FOREWORD

Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

In recent years Internet of Things (IoT) and AI are found to offer beneficial advantages in health-care applications by virtue of improved power efficiency including energy harvesting from the environment and of local AI inferences. Edge computing to process part of big data at each edge device becomes important technique to reduce data traffic in the limited communication bandwidth and to save energy dissipation. Many aspects of these innovative movements essentially owe basic motive force to solid-state circuit and system designs.

It is my great honor to announce the publication of this special section on solid-state circuit design. This section contains 6 regular papers including 1 invited paper, devoted to the distinctive exploration of new circuit techniques on integrated circuits, covering VLSI architecture, digital/analog/memory circuits, and low power technology/circuit, intended for IoT, AI, connectivity, high-reliability, and ultra-low power applications.

The first paper (invited) presents an extensive review on on-chip biomedical signal processing for wearable health-care SoC, with insightful views on future trend in saving data communication bandwidth by data compression and neural network techniques for leading IoT applications. This is followed by a paper proposing a configurable approximate adder considering the accuracy-power trade-off for approximate computing which is now focus of efficient computations in IoT and AI processing. Next, two circuit techniques for low power timer and VCO are presented: the 3rd paper designs a differential gate leakage timer circuitry for small footprint and low power, while the 4th paper focuses on specialty VCO design by ultra-low power and low phase noise design for chip-scale atomic clock. The next paper proposes a novel 1T-4MTJ (Magnetic Tunneling Junction) memory cell structure for field-switching MRAM with a voltage offset self-reference sensing scheme. The last paper evaluates and analyzes the contribution of neuron-induced soft error on SRAM, flip-flop, and combinational circuit in chip-level soft error rate (SER), based on irradiation test results at low voltage.

On behalf of the editorial committee, I would like to express my sincere appreciation to all the authors for their contributions and to all the reviewers for their critical inputs. In addition, I would like to thank the editorial committee for their works on this special section.

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Hideto Hidaka *(Member)* received the B.E., M.E. and Ph. D degrees from the University of Tokyo, Japan respectively. He has been with Mitsubishi Electric Corp., Renesas Technology Corp., and Renesas Electric Corp. for R&D of high-density memory, embedded memory and MCU product platform. At Renesas Electronics he has been engaged in corporate technical management. He is an IEEE Fellow.