INVITED PAPER *Special Section on Opto-electronics and Communications for Future Optical Network*

High-Speed-Operation of All-Silicon Lumped-Electrode Modulator Integrated with Passive Equalizer

Yohei SOBU[†a)], **Shinsuke TANAKA**[†], ***and*** **Yu TANAKA**[†], ***Members***

SUMMARY Silicon photonics technology is a promising candidate for small form factor transceivers that can be used in data-center applications. This technology has a small footprint, a low fabrication cost, and good temperature immunity. However, its main challenge is due to the high baud rate operation for optical modulators with a low power consumption. This paper investigates an all-Silicon Mach-Zehnder modulator based on the lumped-electrode optical phase shifters. These phase shifters are driven by a complementary metal oxide semiconductor (CMOS) inverter driver to achieve a low power optical transmitter. This architecture improves the power efficiency because an electrical digital-to-analog converter (DAC) and a linear driver are not required. In addition, the current only flows at the time of data transition. For this purpose, we use a PIN-diode phase shifter. These phase shifters have a large capacitance so the driving voltage can be reduced while maintaining an optical phase shift. On the other hand, this study integrates a passive resistance-capacitance (RC) equalizer with a PIN-phase shifter to expand the electro-optic (EO) bandwidth of a modulator. Therefore, the modulation efficiency and the EO bandwidth can be optimized by designing the capacitor of the RC equalizer. This paper reviews the recent progress for the high-speed operation of an all-Si PIN-RC modulator. This study introduces a metal-insulator-metal (MIM) structure for a capacitor with a passive RC equalizer to obtain a wider EO bandwidth. As a result, this investigation achieves an EO bandwidth of 35.7–37 GHz and a 70 Gbaud NRZ operation is confirmed.

key words: *photonic integrated circuit, silicon photonics, optical modulator, passive equalizer*

1. Introduction

A rapid increase of the global data traffic in an optical network represents the Compound Annual Growth Rate (CAGR) over 25% for both intensity-modulation direct-detection (IM-DD) and coherent detection scheme in the Global Cloud Index (GCI) report [1]. Due to the strong demands from the optical network application (e.g. data centers), a large transmission capacity and a low power consumption are necessary for compact transceivers such as Quad Small Form-factor Pluggable Double Density (QSFP-DD) or Octal Small Form-factor Pluggable (OSFP) modules [2]. Silicon (Si) photonics is one of the most promising platforms for these applications. They can achieve a highly dense photonics integrated circuit (PIC) due to its high index contrast with the Si/SiO_2 waveguide. To date, some Si PICs have successfully demonstrated their large-capacity and highly-dense data transmission [3], [4]. A further increase in the transmission bandwidth is required for the next-generation standard of 400 Gbps and beyond while maintaining a low cost and a low power consumption. However, the main challenge remains with a higher baud rate operation with a low power consumption for the optical modulator.

To date, several types of Si modulators have been developed for high-speed modulation, high modulation efficiency, and low power consumption [5]. When considering the coherent transmission, the Mach-Zehnder-type modulator (MZM) is suitable in terms of the required range for an operating wavelength and the modulation scheme. The current trend in the development of a Si modulator is for a wide bandwidth demonstration by introducing heterogeneous integration with other materials. A Si-organic hybrid modulator and a plasmonic modulator are promising candidates for the next-generation high-speed optical modulators beyond the 100 Gbaud in the Si photonics platform [6]–[8]. These modulators have not demonstrated their usability in terms of the foundry process compatibility for mass production and long-term reliability. In contrast, all-Si-based optical modulators are attractive candidates because of their compatibility in the foundry process, their highly dense assembly with an electrical driver, high reliability, and small temperature dependency [9]. However, all-Si modulators have some concerns in order to achieve high performance. The carrier plasma effect that is used in all-Si modulators has a relatively weak effect for the refractive index change. They also have a trade-off between the operation bandwidth and the modulation efficiency. This can be attributed to the capacitance of the phase shifter, which is linked to the modulation efficiency. Therefore, high-speed all-Si modulators have been developed while addressing these concerns. In particular, high-speed traveling-wave (TW) type modulators have PN depletion mode that have been investigated [5], [10]. They are mostly driven with an electrical digital-to-analog converter (DAC) and a large-swing linear driver. However, as the symbol rate of the system increases, it is difficult to maintain a large swing due to the trade-off relationship between the modulation depth and the power consumption. Therefore, the current trend of high-speed all-Si modulators are to compensate the high-speed modulators by a strong digital signal processing (DSP) equalizer. Although an 80 Gbaud PAM8 and an 80 Gbaud to 100 Gbaud QAM operation have been demonstrated with offline DSP technology, there is a concern about the power consumption [11]–[14]. From these backgrounds, a new approach for the Si photonics modulator to obtain a high-speed modulation and a

Manuscript received December 27, 2019.
Manuscript revised April 16, 2020.
Manuscript publicized May 15, 2020.

[†]The authors are with Fujitsu Limited, Kawasaki-Shi, 212–8510 Japan.
a) E-mail: sobu.yohei@fujitsu.com

DOI: 10.1587/transele.2019OCP0006

low power consumption is the optical time division multiplexing scheme [15], [16]. They use a mode locked laser, an optical serializer, and limited (quarter rate) electronics to achieve a 104 Gbaud operation, or a 1.5pJ/bit. However, they have an additional loss of 6 dB due to the optical serializer.

From this overview, Si modulators have not been demonstrated for high-speed multi-level operations and a low power consumption for the same device under the same conditions [17]. To reduce power consumption, it is effective to combine an efficient lumped-electrode phase shifter and a CMOS inverter driver. However, it cannot support multi-level modulation format, as this architecture is limited to a binary operation. Then, an optical DAC architecture is a good solution. The binary signals are multiplexed at the optical domain by using a segmented modulator [18], [19]. In fact, a low power operation in higher-order modulation signals such as pulse amplitude modulation (PAM) and quadrature amplitude modulation (QAM) has been demonstrated by using optical DAC technology [20]–[23]. For this architecture, an electrical DAC and a large swing linear driver are not required. To achieve this architecture more effectively, this study introduces a forward-biased PIN phase shifter that is integrated with a passive RC equalizer (PIN-RC). In our previous study, we reported a very low VπL of 0.31 Vcm for a 25 Gbps modulator [24]. This concept can optimize the trade-off between the electro-optic (EO) bandwidth and the modulation efficiency since the capacitance of PIN-RC modulator can be controlled. Then, we demonstrated a very-low-power operation (1.59 mW/Gbps) of a 56-Gbps PAM4 oDAC transmitter by combining the CMOS inverter driver and the segmented modulator [23]. However, the modulation speed was limited by the RC constant of the optical phase shifter. We also demonstrated the feasibility of high-speed modulation by using a lumped electrode PIN-RC modulator, which improves the design of the all-Si PIN-RC phase shifters [25]. This investigation reviews the design controllability and the measurement results of the PIN-RC modulator by introducing a metal-insulator-metal (MIM) structure into the capacitor of a passive RC equalizer. This is achieved with a 3-dB bandwidth (f_{3dB}) of 35.7–37 GHz. This confirms the 70 Gbaud NRZ operation with a clear optical eye opening.

The rest of this paper is organized as follows. Section 2 describes the design of the PIN-RC modulator by using an equivalent circuit of the PIN phase shifter and the RC equalizer. The parameters of the PIN-RC modulator for the high-speed-operation are listed in this section. The fabrication and the measurement results of the PIN-RC modulator are verified in Sect. 3. The results of the DC characteristics, the electro-optic (EO) response, and the high-speed-large signal test are also mentioned. Section 4 discusses the estimated performances when applying the CMOS inverter driver (i.e., removing the limitation of the 50 Ω systems). Finally, a brief summery is provided in Sect. 5.

2. Design and Fabrication of the PIN-RC Modulator

2.1 Lumped Electrode PIN Phase Shifter

This section describes the design and parameters of the lumped electrode PIN-RC modulator. Generally, the free carrier plasma effect is widely used in silicon photonics modulators since the EO effect is small for the silicon phase shifter [5]. The Si phase shifter generates an optical phase shift that corresponds to the amount of the electric charge depleted or injected by the driver circuit. The Si phase shifters, such as the PN and PIN diodes, are commonly used because they are compatible with the foundry process and a small dependence of operating wavelength and temperature. The fundamental efficiency of the Si phase shifter is determined by the overlap of the electrical carrier distribution and the optical field in Si waveguide. In the case of the commonly used Si phase shifter, an electric charge is required to give an optical phase shift equal to π (Q_π), which is approximately 3~6 pC [24], [26]. To achieve a higher power efficiency in this type of situation, the following two viewpoints should be considered.

First, the driving architecture needs to be considered so it supplies an electric charge into the optical phase shifter efficiently. Currently, the traveling-wave (TW) type Si phase shifter with a differential radio frequency (RF) transmission line is commonly used. However, in this architecture, the current is supplied constantly to the differential RF transmission line by the current mode logic (CML) driver. As a result, the power efficiency is low. Afterwards, impedance matching between the CML driver and the optical phase shifter is required. On the other hand, the Si phase shifter can be divided into a short segment and can be treated as a lumped electrode driven by a CMOS inverter driver. In this case, as the current is supplied through data transition, the power efficiency is very high. Also, the lumped electrode architecture enables an easy design of the EO bandwidth.

Second, the types of phase shifters should be properly selected. To obtain a high power efficiency in the case of the lumped electrode architecture, the phase shifter with a large capacitance needs to be applied. Additionally, it is desirable to fabricate the phase shifter with the standard foundry process.

Therefore, for this study, the lumped-electrode forward-biased PIN phase shifter with a large capacitance was chosen. The PIN phase shifter is composed of an un-doped intrinsic layer inside the Si core layer within 480 nm × 220 nm waveguides and p- and n-Si conducting layers on a Si slab layer as shown in Fig. 1. An EO bandwidth of the lumped electrode optical modulators is limited by the RC constant of the phase shifters. Figure 2 illustrates the equivalent circuit of the PIN phase shifter. This consists of a parallel arranged capacitance and resistance (C_F and R_F) for the PIN diode and the series resistance (R_S). The length of the phase shifter to be 250 μm, and the C_F, R_F, and R_S are 13.2 pF, 197 Ω, and 12.2 Ω, respectively. This study

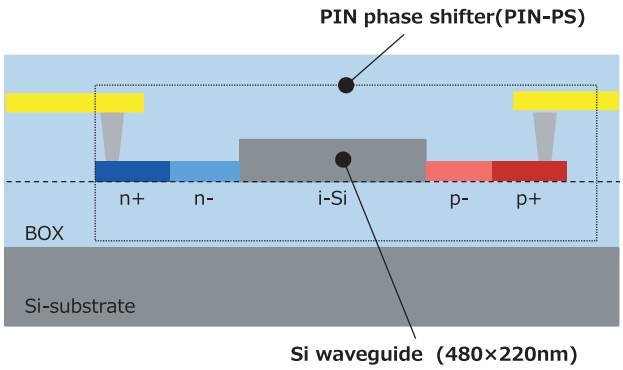


Fig. 1 Cross sectional view of PIN phase shifter.

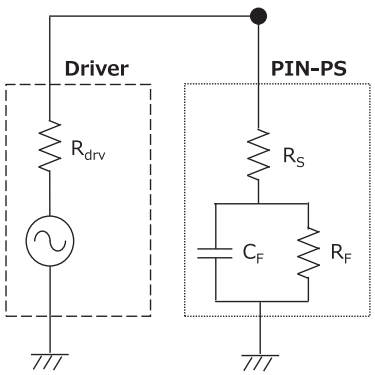


Fig. 2 Equivalent circuit model of PIN phase shifter and driver.

assumes that the driver impedance is 50 Ω when considering the measurement setup of the Si photonics chip. In this case, the EO bandwidth (f_{3dB}) is calculated by the following equation.

$$f_{3dB} = 1/2\pi(R_S + R_{drv})C_F \tag{1}$$

The EO bandwidth of the PIN phase shifter is limited to several hundred MHz mainly due to the large capacitance C_F of the intrinsic region.

2.2 PIN Phase Shifter Integrated with RC Equalizer

To extend the EO bandwidth of the entire system for high-speed operation, this study introduced a passive equalization technique that inserts a simple RC filter between the driver and the PIN phase shifter as presented in the left equivalent circuit in Fig. 3 [23]–[25]. The capacitance C_E and the resistance R_E can be satisfied with the following equation.

$$C_E = C_F/\eta, \quad R_E = RF \times \eta, \quad \eta \gg 1 \tag{2}$$

From this, the capacitance C_E enhances the EO bandwidth by reducing the effective capacitance of the PIN phase shifter by applying Eq. (3).

$$(1/C_E + 1/C_F)^{-1} \sim C_E = C_F/\eta \tag{3}$$

In addition, a resistance R_E for the equalizer is inserted to obtain a flat EO response over the entire signal frequency.

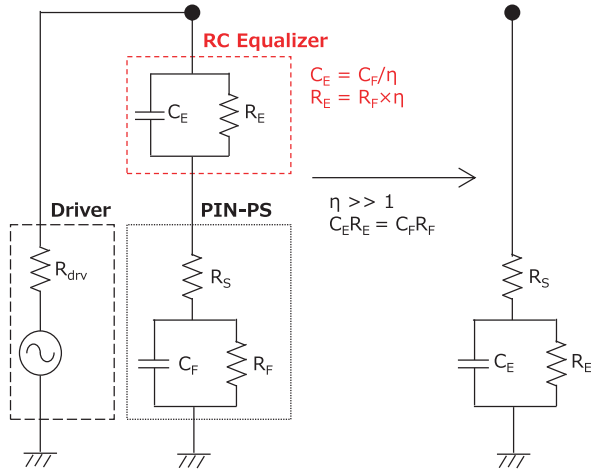


Fig. 3 Equivalent circuit model of PIN phase shifter that is integrated with passive RC equalizer.

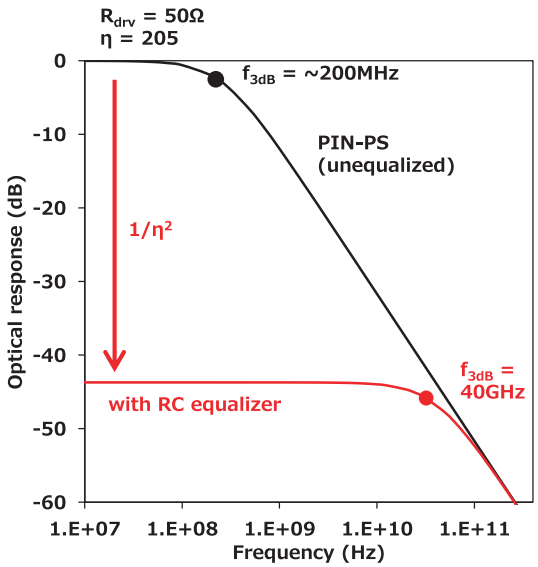


Fig. 4 Calculated optical responses of PIN phase shifter (black line) and PIN phase shifter with passive RC equalizer (red line).

As a result, the equivalent circuit become a simple RC circuit in the right side of Fig. 3. This means that the EO bandwidth of the entire system is extended by a factor of η. In this time, η, C_E, and R_E is set to be 205, 64.4 fF, and 40.5 kΩ, respectively, to achieve 3dB EO bandwidth of 40 GHz, by using Eqs. (2) and (4).

$$f_{3dB} = 1/2\pi(R_S + R_{drv})C_E \tag{4}$$

Figure 4 displays the calculated small-signal EO responses of the entire system. The black and red line show the EO responses with the un-equalized and equalized PIN phase shifter. The un-equalized PIN-PS exhibits too large of an EO response ($\propto 20\log(1/V\pi)$) at a low frequency regime. The RC filter de-emphasis the excess EO response by a factor of $1/\eta^2$. As a result, the EO response of the equalized PIN phase shifter exhibits a flat response up to the designed EO bandwidth of 40 GHz. In this scheme, the relationship

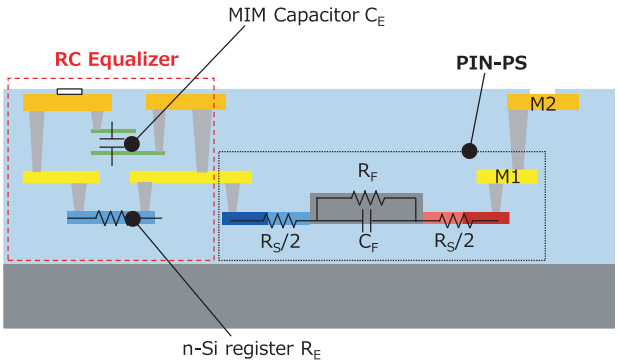


Fig. 5 Cross-sectional view of Si-MZM involving PIN phase shifter that is integrated with RC equalizer.

of the trade-off between the required EO bandwidth and the modulation efficiency can be optimized by designing the RC equalizer. This equalization technique requires no additional power because it consists of only a passive component. The EO response of this system is also strongly affected by the driver impedance R_{drv}. Therefore, in the case of using the CMOS inverter driver with R_{drv} of several Ω, the expansion of the EO response or the improvement of the power efficiency can be achieved. Namely, the lumped electrode PIN-RC modulator is suitable with a high-speed and a high-power efficiency modulation.

In this design scheme, the high accuracy and the controllability of the capacitance C_E and the suppression of the parasitic capacitance are important to enable the stable broadband operation of the modulator. Therefore, this investigation introduced the metal insulator metal (MIM) capacitor to precisely define the C_E. The thinner the insulation layer is between the metal layers, the greater the reduction of the area of the MIM structure. As a result, a smaller parasitic capacitance can be obtained. In addition, a thinner insulation layer enables the precise control of the C_E. Figure 5 depicts the cross-sectional view of the PIN-RC modulator. The resistance of the RC equalizer was fabricated by the n-type Si doped layer.

2.3 Design Parameters of PIN-RC Modulator

This section discusses the design parameters of the PIN-RC modulator. Two types of modulators were fabricated with the EO bandwidth of 30 GHz (design (a)) and 40 GHz (design (b)). The length of the PIN phase shifter was 250 μm. The parameters of the passive RC equalizer were optimized to obtain the required EO bandwidth of the modular as displayed in Table 1.

2.4 Fabricated PIN-RC Modulator

The PIN-RC modulators were fabricated by using a standard Si photonics process at a commercial CMOS foundry. An example of the fabricated device is featured in Fig. 6. It has an asymmetric Si MZM. The device has GSG pads for differential driving. The passive RC equalizer had a very

Table 1 Design parameters and values of PIN RC modulator. Design (a) and design (b) are for EO bandwidth of 30 GHz and 40 GHz respectively.

Parameter		Design Value
Driver impedance	Rdrv	50 Ω
PIN capacitor	C_F	13.2 pF
PIN resistor	R_F	197 Ω
Series resistance	R_S	12.2 Ω
Design (a) RC Equalizer for 30 GHz	C_{E_30GHz}	86.2 fF
	R_{E_30GHz}	30.4 kΩ
	η_{30GHz}	154
Design (b) RC Equalizer For 40 GHz	C_{E_40GHz}	64.4 fF
	R_{E_40GHz}	40.5 kΩ
	η_{40GHz}	205

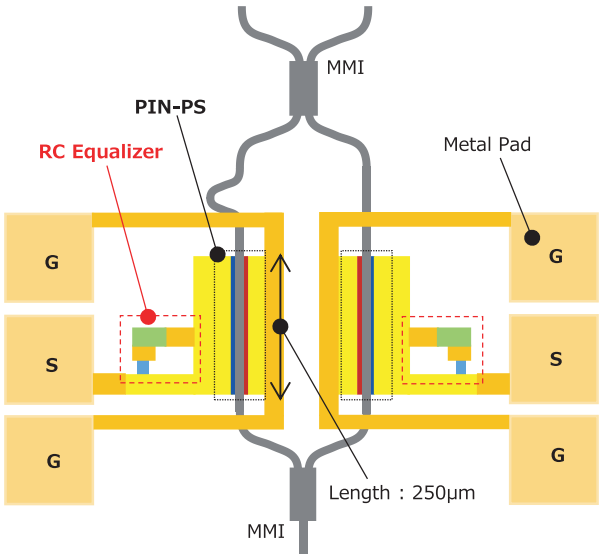


Fig. 6 Fabricated device of Si-PIN-MZM.

compact footprint of < 50 x 60 μm^2 and it can be placed near the PIN phase shifters. The total footprint of the fabricated modulator was only < 400 x 500 μm^2, which includes the GSG probe pads. Thus, these structures are suitable for future optical DAC architecture designs. This is because the densely segmented MZM layout can be combined by employing U-shaped-phase shifters and highly dense metal pads for flipchip bonding.

3. Measurement Results of PIN-RC Modulator

3.1 Experiment Setup

Figure 7 illustrates the experimental setup of the DC characteristics, the EO response, and the high-speed large signal operation. The black and red lines correspond to the electrical cable and the optical single mode fiber, respectively. First, this investigation confirmed the IV characteristics of the PIN-diode with the passive RC equalizer. Second, the modulation efficiency (VπL) was calculated by using the measured bias voltage dependence of the optical interference spectrum shift from the optical spectrum analyzer (YOKOGAWA, AQ6370). Third, the EO response of the PIN-RC modulator was measured with a lightwave

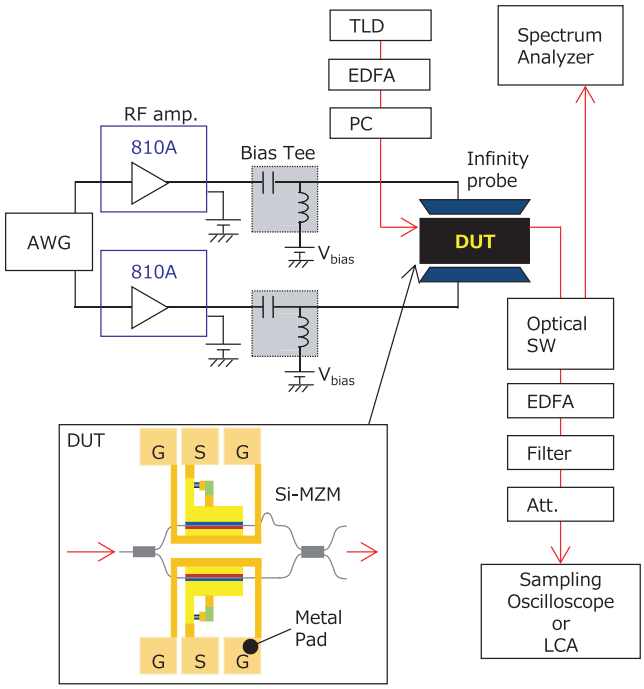


Fig. 7 Measurement setup of IV characteristics, modulation efficiency, EO response, and high-speed large signal test.

component analyzer (LCA) (Keysight, N4373D). For this study, the EO bandwidth was measured to confirm the consistency between the design value of the capacitance (C_E) of the RC equalizer and the measurement results.

Finally, the high-speed large signal test was measured. The details of this test are mentioned in Sect. 3.3. The measurement conditions are in the C-band at room temperature.

3.2 Measured Results of DC Characteristics and EO Response

This section discusses the measurement results of the I-V characteristics, VπL, and the EO response of the PIN-RC modulator. As described in the design section, this study compared the measured results between the two types of designs. The I-V characteristics exhibited the forward-biased diode response with a resistance R_E as shown in Fig. 8. The resistance R_E was measured to be 27.1 kΩ and 36.1 kΩ for design (a) and design (b) respectively. The bias current (I_{bias}) was measured to be 0.145 and 0.193 mA at a forward bias voltage of 6V. Then, the partial bias on PIN-diode can be calculated by subtracting the voltage drop at the resistance R_E from 6V. Each partial bias on PIN-diode was 0.75 and 0.77 V in design (a) and design (b) respectively. Figure 9 corresponds to the forward bias dependencies of VπL, which is calculated by the optical phase shift for both designs with both arms respectively. An optical phase shift is derived from the transmission spectrum shift, which follows the applied DC bias voltage. The VπL was obtained to be approximately 1.7 Vcm and 2 Vcm at a forward bias voltage of 6 V. From these results, the π-phase shift charge (Qπ) can

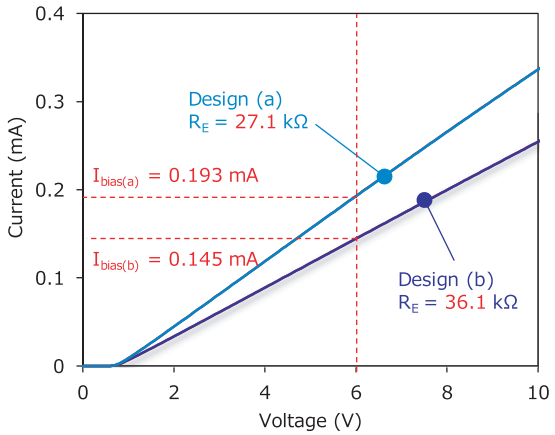


Fig. 8 Measured IV characteristics for design (a) and design (b)

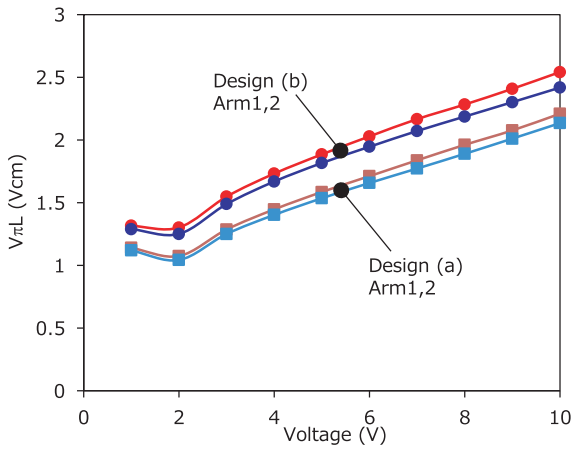


Fig. 9 Measured VπL for design (a) and design (b)

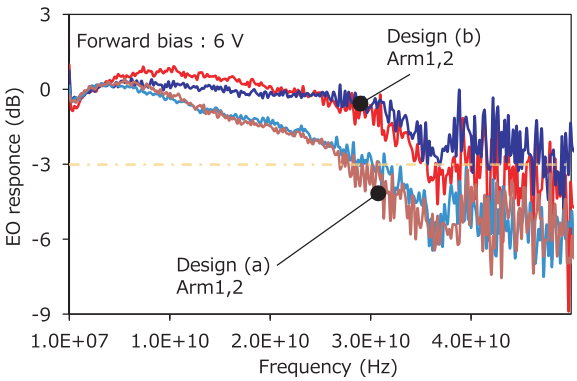


Fig. 10 Measured EO response for design (a) and design (b)

be calculated to be 5.1~5.8 pC which is almost common for various types of Si PS [24], [26]. The optical propagation loss of the phase shifter was measured to be 27.8 dB/cm, which corresponds to a modulator insertion loss of 0.7 dB.

Figure 10 demonstrates the measured small-signal EO responses for both designs with both arms of the fabricated modulator with forward bias of 6V, respectively. The EO responses were normalized in the low frequency range. This

Table 2 Measured values of EO bandwidth and modulation efficiency of PIN-RC modulators for design (a) and design (b).

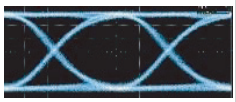
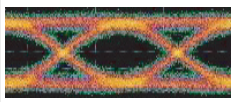
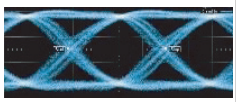
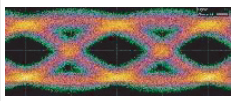
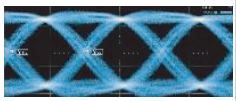
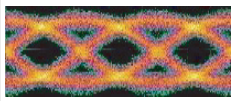
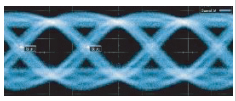
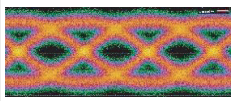
Design / Arm	Measured f_{3dB} [GHz]	Measured VπL [Vcm]
(a) / arm1	27.5	1.71
(a) / arm2	29.0	1.66
(b) / arm1	35.7	2.03
(b) / arm2	37.0	1.95

study obtained wide and flat EO responses because of the optimized RC equalizer setting. The f_{3dB} was measured to be 27.5-29 GHz for design (a) and 35.7–37 GHz for design (b), respectively. The measured values of the VπL and f_{3dB} were summarized in Table 2. The measured characteristics were almost consistent with the design value. Design (a) has a higher modulation efficiency and a smaller EO bandwidth because it has a larger capacitance, C_E. From these measurement results, the optimization of the trade-off between the modulation efficiency and the expanded EO bandwidth of the PIN-RC modulator was successfully demonstrated with good controllability by introducing MIM-type capacitor into the RC passive equalizer.

3.3 Measured Characteristics of High-Speed Large Signal Operation

This section begins by discussing the experimental setup and the conditions for the measurement. For the large signal measurement, this investigation used an arbitrary waveform generator (AWG, Keysight, M8196A), RF phase matching cables, RF amplifiers (SHF, L810), bias-tees, and RF probes (Form Factor, Infinity probe) in a push-pull manner. The total frequency response of these RF components except for the RF probes was compensated by the AWG. The modulator was driven with a pseudorandom binary sequence NRZ signal of $2^{11} - 1$ generated from the AWG with a raised cosine filter of $\alpha = 0.1{\sim}0.5$. The baud rate of the NRZ signal was varied from 40 Gbaud to 70 Gbaud. The peak-to-peak amplitude (V_{pps}) in the drive signal was measured to be 2.3–4.8 V for each modulation speed shown. The values of V_{pps} decreased with the increased baud rate because of the influence of the limited bandwidth and nonlinearity of the AWG and RF amplifier. The input wavelength was set to the quadrature point while using the asymmetric MZI. In the experiment, the bias voltage was fixed at 6 V to maintain the same bias condition for the small-signal measurement. The measured device in design (b) demonstrates the high-speed large signal operation. The modulated signal was amplified by an Erbium Doped Fiber Amplifier (EDFA) and recorded with a sampling oscilloscope (Keysight, 86100D) that has an optical plugin module with a bandwidth of 65 GHz. The input electrical waveform and the output optical waveforms for 40 Gbaud to 70 Gbaud NRZ operations are described in Table 3. The measured V_{pps} and the extinction ration (ER) of the measured optical waveform were also summarized. The clear eye opening for each data rate was confirmed. The measured extinction ratio (ER) was 3.4 dB at 40 Gbaud, 3.2 dB at 50 Gbaud, 2.4 dB at 60 Gbaud, and 1.6 dB at 70 Gbaud. For each modulation speed, this investigation observed that the optical waveforms were similar to the electrical eye waveforms of the drive signal. This finding indicates that the large-signal bandwidth was not mainly limited by the bandwidth of the Si modulator for these operation speeds. Therefore, high-speed operations over 70 Gbaud can be achieved by the optimization of the measurement setup of the RF signals.

Table 3 40-70 Gbaud electrical input waveform with peak-to-peak amplitude in NRZ drive signal and measured optical eye diagram. This includes extinction ratio of PIN-RC modulator in case of design (b).

Baudrate [Gbaud]	Electrical Input Waveform V_{pps}	Optical Output Waveform Extinction Ratio
40	 4.8 V	 3.4 dB
50	 4.6 V	 3.2 dB
60	 3.8 V	 2.4 dB
70	 2.3 V	 1.6 dB

4. Discussion

Overall, this investigation demonstrates the feasibility of the high-speed operation of an all-Si PIN-RC MZM. In this study, the modulation efficiency was limited to a small value of VπL (2 Vcm) because the EO response and modulation efficiency are affected by the limitation of the output impedance of the driver ($R_{drv} = 50\ \Omega$). In the case where the CMOS inverter driver is combined with the PIN-RC modulator [23], this can significantly enhance the modulation efficiency because of the small output impedance (several Ω) for the CMOS inverters. Figure 11 corresponds to the estimated EO response when applying the CMOS inverter driver. The dashed line shows the optical response of R_{drv} at 50 Ω which is the same as demonstrated in Fig. 4. The bold line shows the case of R_{drv} at 0 Ω. In the case of $R_{drv} = 0$, we can improve the modulation efficiency (C_E) with maintaining f_{3dB} in the Eq. (4). Namely, η can be reduced from 205 to 38.3 to obtain the same EO bandwidth of 40 GHz. In this case, we assumed to control the forward bias voltage to maintain the partial bias on the PIN-diode (~0.77 V in design (b)).

As a result, the PIN-RC modulator exhibits a 12.3 dB

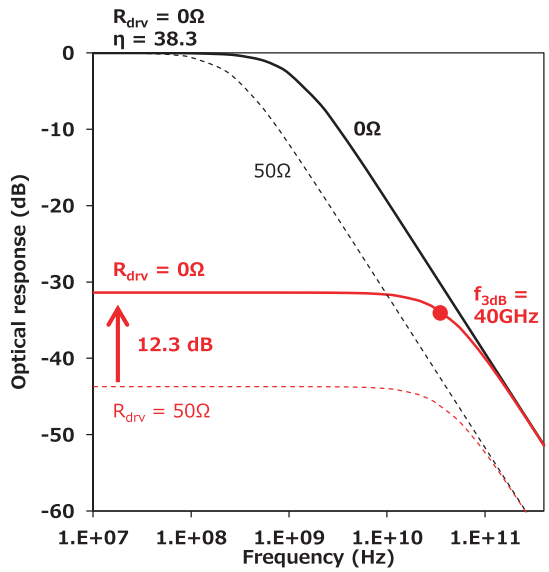


Fig. 11 Estimated EO response in case of applying CMOS inverter driver with PIN-RC modulator.

higher EO response than the 50 Ω system. This corresponds to a small VπL of 0.4 Vcm at DC and small DC bias under 2V. These calculations predict that a CMOS inverter driver which has a small output impedance at its saturated region is preferable. For this bandwidth equalization technique, the capacitance C_E should be carefully optimized due to the trade-off between the power efficiency and the EO bandwidth.

5. Conclusion

This paper describes the optimization technique between the power efficiency and the EO bandwidth of an all-Si MZM by using a PIN-RC structure. This investigation describes a broadband operation for the PIN-RC modulator to achieve a higher EO bandwidth. The equalizer was composed of a simple n-doped Si register and a MIM capacitor, which are compatible with the standard CMOS process. The fabricated modulator exhibited a wide bandwidth of f_{3dB} = 35.7–37 GHz for a 50 Ω system. The VπL was measured to be 2 Vcm. In the large-signal experiment, a clear eye opening of up to 70 Gbaud NRZ signals was obtained with an ER of 1.4 dB. These results clearly indicate the feasibility of the all-Si modulator for use in a high-speed and low-power-consumption transmitter. Finally, this study shows the architecture of enhancing the power efficiency by using CMOS inverter driver. In addition, higher-order modulation schemes, such as PAM4 or QAM, can be achieved by combining the CMOS inverter driver with the segmented PIN-RC modulator.

Acknowledgments

The authors would like to thank the colleagues in Fujitsu Limited.

References

[1] Cisco Global Cloud Index: Forecast and Methodology, 2016-2021 White Paper.
[2] M. Bohn, P. Magill, M. Hochberg, D. Scordo, A. Novack, and M. Streshinsky, "Next-Generation Silicon Photonic Interconnect Solutions," OSA OFC2019, paper M3J.3, 2019.
[3] T. Aoki, S. Sekiguchi, T. Simoyama, S. Tanaka, M. Nishizawa, N. Hatori, Y. Sobu, A. Sugama, T. Akiyama, A. Hayakawa, H. Muranaka, T. Mori, Y. Chen, S.-H. Jeong, Y. Tanaka, and K. Morito, "Low crosstalk simultaneous 12 ch × 25 Gb/s operation of high-density silicon photonics multichannel receiver," J. of Lightwave Technol., vol.36, no.5, pp.1262–1267, 2018.
[4] P.D. Dobbelaere, G. Armijo, J. Balardeta, B. Chase, Y. Chi, A. Dahl, Y.D. Koninck, S. Denton, M. Eker, S. Fathpour, D. Foltz, F. Gholami, S. Gloeckner, K.Y. Hon, S. Hovey, S. Jackson, W. Li, Y. Liang, M. Mack, G. Masini, G. McGee, A. Mekis, S. Pang, M. Peterson, T. Pinguet, L. Planchon, K. Roberson, S. Sahni, J. Schramm, M. Sharp, C. Sohn, K. Stechschulte, P. Sun, G. Vastola, S. Wang, B. Weber, G. Wong, K. Yokoyama, S. Yu, and R. Zhou, "Silicon-photonics-based optical transceivers for high-speed interconnect applications," SPIE, vol.9775, 977503 pp.1–5, 2016. DOI:10.1117/12.2218140
[5] J. Witzens, "High-Speed Silicon Photonics Modulators," Proc. IEEE, vol.106, no.12, pp.2158–2182, 2018. DOI:10.1109/JPROC.2018.2877636
[6] L. Alloatti, R. Palmer, S. Diebold, K.P. Pahl, B. Chen, R. Dinu, M. Fournier, J.-M. Fedeli, T. Zwick, W. Freude, C. Koos, and J. Leuthold, "100 GHz silicon–organic hybrid modulator," Light: Sci. & Appl. 2014, vol.3, no.5, e173, pp.1–4, 2014. DOI:10.1038/lsa.2014.54
[7] H. Zwickel, S. Wolf, C. Kieninger, Y. Kutuvantavida, M. Lauermann, T.D. Keulenaer, A. Vyncke, R. Vaernewyck, J. Luo, A.K.-Y. Jen, W. Freude, J. Bauwelinck, S. Randel, and C. Koos, "Silicon–organic hybrid (SOH) modulators for intensity-modulation / direct-detection links with line rates of up to 120Gbit/s," Opt. Express, vol.25, no.20, pp.23784–23800, 2017. DOI:10.1364/OE.25.023784
[8] U. Koch, C. Uhl, H. Hettrich, Y. Fedoryshyn, C. Hoessbacher, W. Heni, B. Baeuerle, B. Bitachon, A. Josten, M. Ayata, H. Xu, D.L. Elder, L.R. Dalton, E. Mentovich, D. Tsiokos, N. Pleros, M. Möller, and J. Leuthold, "Monolithic high-speed transmitter enabled by BiCMOS-plasmonic platform," ECOC2019, paper PD.1.4, 2019.
[9] K. Goi, N. Ishikura, H. Ishihara, S. Sakamoto, K. Ogawa, T.-Y. Liow, X. Tu, G.-Q. Lo, and D.-L. Kwong, "Low-Voltage Silicon Mach-Zehnder Modulator Operating at High Temperatures without Thermo-Electric Cooling," OSA OFC2016, paper W2A.23, 2016.
[10] M. Li, L. Wang, X. Li, X. Xiao, and S. Yu, "Silicon intensity Mach–Zehnder modulator for single lane 100 Gb/s applications," Photonics Research, vol.6, no.2, pp.109–116, 2018. DOI:10.1364/PRJ.6.000109
[11] M. Jacques, Z. Xing, A. Samani, E. E.-Fiky, X. Li, S. Lessard, and D.V. Plant, "200Gbit/s Net Rate Transmission over 2 km with a Silicon Photonic Segmented MZM," ECOC2019, paper PD.1.6, 2019.
[12] S. Zhalehpour, J. Lin, M. Guo, H. Sepehrian, Z. Zhang, L.A. Rusch, and W. Shi, "All-Silicon IQ Modulator for 100Gbaud 32QAM Transmissions," Proc. OFC2019, paper Th4A.5, 2019.
[13] J. Zhou, J. Wang, L. Zhu, Q. Zhang, and J. Hong, "Silicon Photonics Carrier Depletion Modulators Capable of 85Gbaud 16QAM and 64Gbaud 64QAM," OSA OFC2019, paper Tu2H.2, 2019.
[14] F. Zhang, Y. Zhu, F. Yang, L. Zhang, X. Ruan, Y. Li, and Z. Chen, "Up to Single Lane 200G Optical Interconnects with Silicon Photonic Modulator," OSA OFC2019, paper Th4A.6, 2019.
[15] J. Verbist, M. Lillieholm, J.V. Kerrebrouck, S.A. Srinivasan, P.D. Heyn, J.V. Campenhout, M. Galili, L.K. Oxenløwe, X. Yin, J. Bauwelinck, and G. Roelkens, "104 Gbaud OOK and PAM-4

Transmission over 1km of SMF using a Silicon Photonics Transmitter with Quarter-Rate Electronics," OSA OFC2019, paper Tu2l.2, 2019.

[16] J. Lambrecht, J. Verbist, H. Ramon, M. Vanhoecke, J. Bauwelinck, X. Yin, and G. Roelkens, "Low-Power (1.5 pJ/b) Silicon Integrated 106 Gb/s PAM-4 Optical Transmitter," J. of Lightwave Technol., vol.38, no.2, pp.432–438, 2020. DOI:10.1109/JLT.2019.2933286

[17] M.C. Larson, J. Sonkoly, A. Mizrahi, M. Ayliffe, and J. Kemp, "InP vs Si Photonic Integrated Circuit Platforms for Coherent Data Center Interconnects," ECOC 2018, paper Mo3I.5, 2018.

[18] T. Yamase, M. Sato, H. Noguchi, K. Sato, and T. Kato, "Low-Power Multi-level Modulation of InP MZM with In-line Centipede Structure Directly Driven by CMOS IC," OECCPSC2013, paper WK2-3, 2013.

[19] B. Milivojevic, S. Wiese, S. Anderson, T. Brenner, M. Webster, and B. Dama, "Demonstration of Optical Transmission at Bit Rates of Up to 321.4 Gb/s Using Compact Silicon Based Modulator and Linear BiCMOS MZM Driver," J. of Lightwave Technol., vol.35, no.4, pp.768–774, 2017. DOI:10.1109/JLT.2016.2592618

[20] M. Webster, K. Lakshmikumar, C. Appel, C. Muzio, B. Dama, and K. Shastri, "Low-Power MOS-Capacitor Based Silicon Photonic Modulators and CMOS Drivers," OSA OFC2015, paper W4H.3, 2015.

[21] T.N. Huynh, N. Dupuis, R. R.-Donadio, J.E. Proesel, D.M. Gill, C.W. Baks, A.V. Rylyakov, C.L. Schow, W.M.J. Green, and B.G. Lee, "Flexible Transmitter Employing Silicon-Segmented Mach–Zehnder Modulator With 32-nm CMOS Distributed Driver," J. of Lightwave Technol., vol.34, no.22, pp.5129–5136, 2016. DOI:10.1109/JLT.2016.2606558

[22] I.G. López, A. Aimone, P. Rito, S. Alreesh, T. Brast, V. Höhns, G. Fiol, M. Gruner, J.K. Fischer, J. Honecker, A.G. Steffan, M. Schell, A. Awny, A.C. Ulusoy, and D. Kissinger, "High-Speed Ultralow-Power Hybrid Optical Transmitter Module With InP I/Q-SEMZM and BiCMOS Drivers With 4-b Integrated DAC," IEEE Trans. Microw. Theory Techn., vol.64, no.12, pp.4598–4610, 2016. DOI:10.1109/TMTT.2016.2622701

[23] S. Tanaka, T. Simoyama, T. Aoki, T. Mori, S. Sekiguchi, S.-H. Jeong, T. Usuki, Y. Tanaka, and K. Morito, "Ultralow-Power (1.9 mW/Gbps), 56-G PAM4 Operation of Si Photonic Transmitter Integrating Segmented PIN Mach-Zehnder Modulator and 28-nm CMOS Driver," J. of Lightwave Technol., vol.36, no.5, pp.1275–1280, 2018. DOI:10.1109/JLT.2018.2799965

[24] T. Baba, S. Akiyama, M. Imai, and T. Usuki, "25-Gb/s broadband silicon modulator with 0.31 Vcm VπL based on forward-biased PIN diodes embedded with passive equalizer," Opt. Express, vol.23, no.26, pp.32950–32960, 2015. DOI:10.1364/OE.23.032950

[25] Y. Sobu, T. Simoyama, S. Tanaka, Y. Tanaka, and K. Morito, "70 Gbaud Operation of All-Silicon Mach-Zehnder Modulator based on Forward-Biased PIN Diodes and Passive Equalizer," OECCPSC2019, paper MD2-2, 2019.

[26] D. Petousi, L. Zimmermann, K. Voigt, and K. Petermann, "Performance Limits of Depletion-Type Silicon Mach-Zehnder Modulators for Telecom Applications," J. Lightw. Technol., vol.31, no.22, pp.3556–3562, 2013. DOI:10.1109/JLT.2013.2284969

Yohei Sobu received his B.E. and M.E. degrees in electrical and electronic engineering from the Tokyo Institute of Technology in Tokyo, Japan in 2011 and 2013, respectively. He joined Fujitsu Laboratories, Ltd., in Atsugi, Japan and the Photonics Electronics Technology Research Association (PETRA) in Tsukuba, Japan. He has been working on the development of silicon photonics devices. He is currently a researcher with Fujitsu Limited, Shinkawasaki, Japan. His current research focuses on the development of integrated photonics.

Shinsuke Tanaka received his B.E., M.E., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 2000, 2002, and 2013, respectively. In 2002, he joined Fujitsu Laboratories Ltd. in Kanagawa, Japan, where he has been involved in the research and development of wavelength tunable lasers and semiconductor optical amplifier (SOA). He has been a member of the Photonics Electronics Technology Research Association (PETRA) from 2012 to 2019. He currently conducts research on silicon hybrid lasers and silicon integrated modulators. He is presently a research manager for Fujitsu Limited for integrated photonics.

Yu Tanaka received his Ph.D. degree in material science from the Tokyo Institute of Technology in Tokyo, Japan in 2000. In 2002, he joined Fujitsu Laboratories, Ltd. in Atsugi, Japan. Since then, he has been involved in the development of optical devices that includes quantum dot lasers and photonic-crystals-based optical switches. In 2012, he joined the Photonics Electronics Technology Research Association, where he is currently a Senior Researcher. He is currently engaged in the development and industrialization of integrated silicon-photonics-based optical transceivers.