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# A Noise-Canceling Charge Pump for Area Efficient PLL Design

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**SUMMARY**    In general, since the in-band noise of phase-locked loops (PLLs) is mainly caused by charge pumps (CPs), large-size transistors that occupy a large area are used to improve in-band noise of CPs. With the high demand for low phase noise in recent high-performance communication systems, the issue of the trade-off between occupied area and noise in conventional CPs has become significant. A noise-canceling CP circuit is presented in this paper to mitigate the trade-off between occupied area and noise. The proposed CP can achieve lower noise performance than conventional CPs by performing additional noise cancelation. According to the simulation results, the proposed CP can reduce the current noise to 57% with the same occupied area, or can reduce the occupied area to 22% compared with that of the conventional CPs at the same noise performance. We fabricated a prototype of the proposed CP embedded in a 28-GHz LC-PLL using a 16-nm FinFET process, and 1.2-dB improvement in single sideband integrated phase noise is achieved.
*key words:* *PLL, frequency synthesizer, phase-locked loop, charge pump, noise-cancel, phase noise, jitter, in-band noise, occupied area*

## 1.    Introduction

Phase-locked loops (PLLs) are often used as frequency synthesizers in most wireless and wireline communication systems. The phase noise of PLLs limits the signal-to-noise ratio of transmitters and receivers. Recent high-performance communication systems with multi-level modulation, such as quadrature amplitude modulation and pulse amplitude modulation, strongly require lower phase noise to improve communication quality [1]–[9].

In recent years, digital PLLs have been widely used because of their benefits, such as portability, small area, and noise tolerance. However, analog PLLs are still an attractive option for clock generation when lower noise is required or when designing in older processes [32]. The in-band phase noise of digital PLLs is usually determined by the resolution of the time-to-digital converters (TDCs) and digitally controlled oscillators (DCOs). High-resolution TDCs and DCOs can result in large circuits that consume a lot of power and area. Therefore, digital PLLs have higher cost and worse performance compared with analog PLLs when targeting lower phase noise [33].

Typical analog PLLs consist of a feedback loop with several blocks as shown in Fig. 1. Table 1 shows the transfer
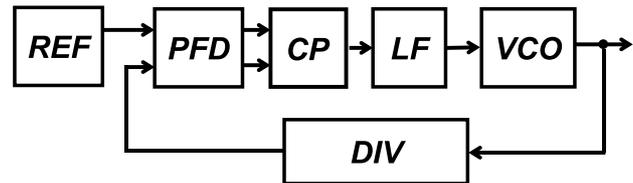
**Fig. 1**    PLL block diagram.

**Table 1**    Closed loop transfer functions for PLL blocks (©2020 IEEE [31]).

| Block | Transfer function | Frequency response | Block | Transfer function | Frequency response |
|---|---|---|---|---|---|
| REF / DIV | $\dfrac{N}{1+\frac{s}{KF(s)}}$ | LPF | LF | $\dfrac{K_o}{s+KF(s)}$ | BPF |
| PFD-CP | $\dfrac{1}{K_{PD}}\cdot\dfrac{N}{1+\frac{s}{KF(s)}}$ | LPF | VCO | $\dfrac{s}{s+KF(s)s}$ | HPF |
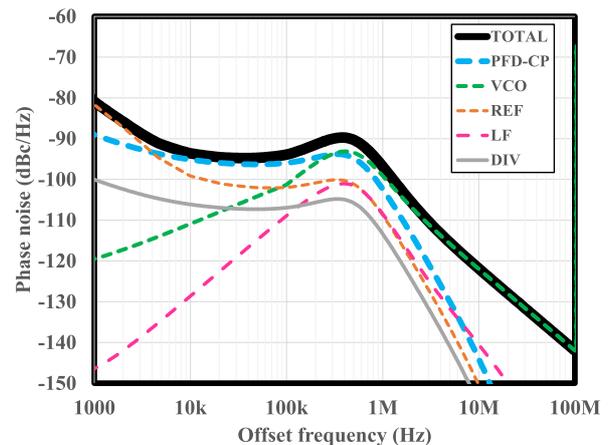


**Fig. 2**    Example of phase noise with contribution of each block.

functions and frequency response of the phase noise in each block. The transfer functions are obtained from the linear PLL model [10]–[12], and these transfer functions have different types of frequency response, including low-pass filter (LPF), band-pass filter (BPF), and high-pass filter (HPF). Figure 2 shows an example of the frequency response of the phase noise in each block. The dominant components of phase noise differ depending on the frequency region because the frequency response of the noise transfer functions differ between blocks. For example, inside the loop bandwidth, the phase noise of voltage-controlled oscillators

(VCOs) is not dominant since VCOs have an HPF transfer characteristic, the in-band phase noise of VCOs is suppressed. In contrast, the phase noise of PFD-CPs is dominant inside the bandwidth, as shown in Fig. 2 [13], [14], owing to their LPF transfer characteristic.

There are methods for reducing in-band phase noise from each block in a PLL. Reference clock noise generally appears within several kilohertz-offset frequency, and can be reduced by using low-noise crystal oscillators with high-Q and enhancing the driving capability of the output buffers. The noise of dividers can be suppressed by achieving high slew rate using high-speed devices in advanced technologies like the FinFET process. The noise of the loop filters is predominantly thermal noise from resistors, which can be mitigated by adjusting the loop parameters to reduce the resistances that comprise the loop filters [16]. The noise of CPs can be reduced by increasing transistor sizes because noise in devices such as MOSFETs can be suppressed by using larger size devices. However, larger devices require a larger occupied area, resulting in a higher fabrication cost of low-noise CPs. This becomes a very serious issue when using advanced technologies such as the FinFET process.

We propose a noise-canceling CP that suppresses the in-band noise and reduces occupied area. This paper is organized as follows. The trade-off issues of conventional CPs are described in Sect. 2. Section 3 introduces the design of the proposed CP that solves the trade-off. Section 4 presents experimental results. Finally, Sect. 5 provides our conclusions.

## 2. Low-Noise Design Issues for Conventional CPs

### 2.1 General Issues of Conventional Low-Noise CPs

In the linear PLL model, the in-band phase noise associated with the CPs can be expressed as

$$\mathcal{L}_{CP} \propto \frac{N^2}{(I_{CP}/2\pi)^2}, \qquad (1)$$

where N is the number of divisions of the PLL, and $I_{CP}$ is the CP output current value [15]. This shows that the in-band phase noise associated with CPs can be adjusted using the loop parameters. Specifically, although the in-band noise can be reduced by using smaller N and larger $I_{CP}$, this creates undesirable requirements for other blocks. For example, increasing $I_{CP}$ causes larger capacitors to be required in the loop filters, which increases the occupied area. Similarly, reducing N results in the need for a higher-frequency reference clock since the output frequency of the PLL is determined by the reference frequency multiplied by N, and this results in increased power consumption. Thus, adjusting loop parameters such as N or $I_{CP}$ to improve the in-band phase noise results in larger occupied area or power consumption. Hence, the only practical method for reducing the in-band phase noise is to adopt large-size transistors for CPs.

Recently, the FinFET process has been widely used to
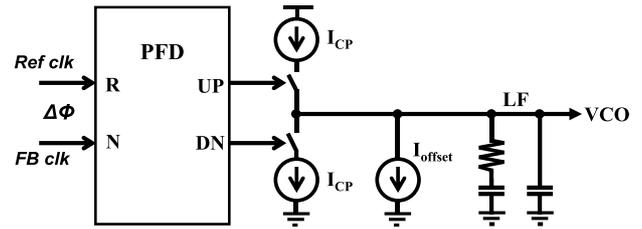


**Fig. 3** Conventional architecture of CP.
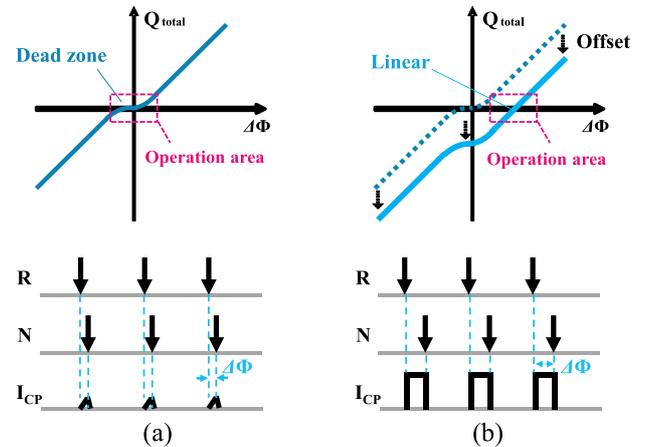


**Fig. 4** Images of PFD-CP transfer curve and waveform (a) without offset current and (b) with offset current.

design advanced transceivers for wireline and wireless communication systems. When FinFETs are used, the noise performance of CPs tends to be degraded compared with planer MOSFETs [17]. FinFET gates are limited to short lengths owing to the process integration of the high-permittivity gate dielectric and metal gate [17]. One typical method for imitating a long-gate-length transistor is to use stacked short-gate-length transistors [18]. However, the number of transistors in the stack is limited due to the voltage drops from the large source resistance of the transistors [17]. As a result, there are limits to increasing the gate length in each transistor in CPs for low-noise performance, and low-noise design techniques for CPs are becoming more and more important in advanced FinFET processes.

### 2.2 Trade-Off between Area and Noise in Conventional CPs with Phase Offset Generator

Figure 3 shows a conventional architecture for CPs using a linearization method. In the linearized CP, it is common to use an offset CP current as a phase-offset generator [19]–[22]. Figure 4 shows the injected charge versus input phase error characteristic, and waveforms of the reference (R) and feedback (N) clocks in the PFD and the output current $I_{CP}$ of the CP. When there is almost no phase offset between the two clocks, the PFD and CP operate in a region around the zero-phase error called the dead zone, as shown in Fig. 4.

This dead-zone is primarily derived from the delayed
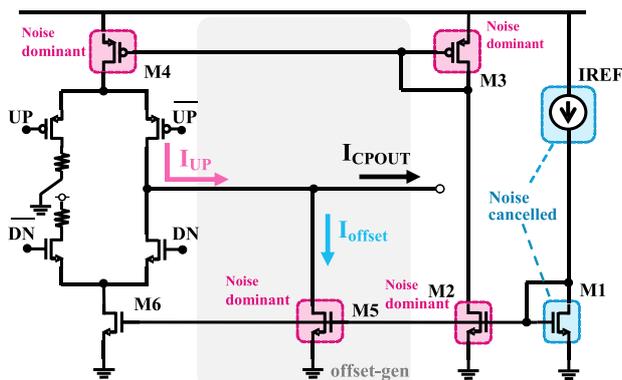
**Fig. 5** Circuit diagram of conventional CP (©2020 IEEE [31]).



**Fig. 6** Current waveforms: (a) Current pulse of main CP; (b) Offset current; (c) CP output current.

response of the "UP" or "DN" switches and current sources to fine phase errors. As shown in the waveforms in Fig. 4 (a), $I_{CP}$ is not output properly because CP cannot adequately follow the fine phase error between the reference and feedback clocks. Consequently, PLL performances such as phase noise and spurs are degraded because the behavior of the PLL differs from the ideal operation due to the dead zone.

The phase-offset generator $I_{offset}$ is used to deal with above mentioned dead-zone issue. As shown in Fig. 4 (b), by using the phase-offset generator, the loop is locked with a constant phase offset between the reference and feedback clocks depending on the offset current value. Therefore, the PFD and CP can operate in a linear region, which means that the PFD and CP can follow fine phase errors, and the PLL with phase-offset generator can avoid performance degradation due to the dead zone. Moreover, the phase offset generator eliminates the need to consider the current mismatch between the up and down currents which often causes trouble when the PFD and CP operate in the region around the zero-phase error [23]–[30].

Figure 5 shows the circuit diagram of a conventional CP with phase-offset generator. The CP has two current sources M4 and M6 that are controlled by "UP" and "DN" signals from the PFD, IREF is a constant current source, and M1, M2, and M3 are current mirrors. In this circuit, a current source M5 is added to the CP output as a phase offset generator. Figure 6 (a), (b), and (c) show the current waveforms of the current pulse $I_{UP}$, the constant current $I_{offset}$, and the CP output current $I_{CPOUT}$, respectively. The pulse width of $I_{UP}$ is automatically controlled by the PFD so that the area "A" equals "B" in Fig. 6. This is because the total charge injected into the loop filter in one period is zero when the PLL is locked [15]. The phase offset in the conventional CP is realized by the offset current generator M5 in this way. The noise generated in M1 and IREF in Fig. 5 are copied to both M4 and M5 and included in $I_{UP}$ and $I_{offset}$, respectively. These noise elements in $I_{UP}$ and $I_{offset}$ can be canceled, since the output charge accumulated by $I_{UP}$ is discharged by $I_{offset}$ every cycle while the PLL is locked [15]. In contrast to IREF and M1, the noise of M2, M3, M4, and M5 cannot be canceled, and are dominant noise elements in
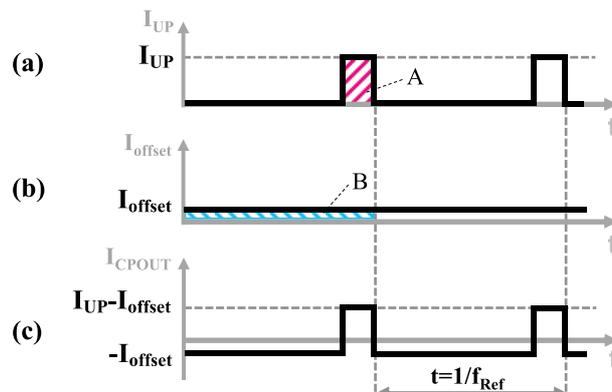
the conventional CP circuit. Incidentally, M6 is not a dominant noise element because it has almost no operation while the loop is locked with the phase offset.

In order to reduce the CP noise, the size of each transistor is determined as follows based on the above relations. The sizes of M2, M3, M4, and M5 need to be large since they are dominant noise sources. The size of M4 becomes very large depending on the mirror ratio from M3, which is usually more than 5 times, because the current value of M3 cannot be designed so large to prevent extra power consumption. Since the size of M5 is large even though it has a small current value, the size of M6 also needs to be large. This is because the size of M6 is more than 10 times that of M5 depending on the current mirror ratio, because the current value of M6 is usually designed to be more than 10 times the offset current of M5. Moreover, the current value of M1 is usually designed to be close to M2 and M5, and therefore, the size of M1 automatically increases to match the size due to the mirror relation. In this way, although M1 and M6 are not dominant noise elements in the conventional CP, their size needs to be large.

To achieve low-noise performance in conventional CPs with a phase offset generator as shown in Fig. 5, large transistors are needed for M1, M2, M3, M4, M5, and M6. Since many large transistors are used, a large occupied area is needed for low noise performance, creating a trade-off between noise performance and occupied area in conventional CPs with a phase-offset generator.

## 3. Circuit Design of Proposed Noise-Canceling CP

### 3.1 Principle of Offset Current Generation and Noise Cancellation in Proposed CP

We propose a novel CP circuit as shown in Fig. 7 that mitigates the trade-off between noise performance and occupied area. By using the proposed CP, the noise of M2 and M3 in addition to IREF and M1 can be cancelled as described later. A phase-offset generator using a capacitor $C_S$ is used to flow the offset current instead of the offset current source that is used in conventional CPs. It is necessary to repeatedly

**Fig. 7** Circuit diagram of proposed CP (©2020 IEEE [31]).



**Fig. 8** Parts related to generating a phase offset.



**Fig. 9** Current waveforms: (a) Current pulse of main CP; (b) Offset current; (c) CP output current.



**Fig. 10** Proposed CP with parts related to discharging method highlighted.

charge and discharge for every period of the phase comparison because current cannot flow continuously to a capacitor. We use the current source M7, voltage-follower A1, and some switches for the charge and discharge operations. The upper- and lower-electrode voltage of $C_S$, and the CP-output voltage are defined as $V_U$, $V_L$, and $V_{CP}$, respectively.

Similar to the conventional CP, the following-stage LF is charged by the CP current $I_{up}$. After that, $C_S$ is charged by $I_{CHG}$ in the proposed CP to realize the phase offset operation. Figure 8 shows the circuit diagram of the proposed CP during a charging operation. In order to generate the phase offset, switches S1 and S2 are turned on, and $I_{CHG}$ flows to $C_S$ as shown in Fig. 8. At this time, $I_{UP}$ does not flow and $I_{CHG}$ comes from the following-stage LF as $I_{CPOUT}$. Note that $I_{CHG}$ is strongly correlated with $I_{UP}$ because the LF is previously charged by $I_{UP}$. Figure 9 (a), (b), and (c) show the current waveforms of the current pulse $I_{UP}$ in Fig. 7, the offset current $I_{CHG}$, and CP-output current $I_{CPOUT}$ in Fig. 8, respectively. The offset current $I_{CHG}$ flows and the charge corresponding to area "B" is stored in $C_S$ as shown in Fig. 9 (b).

Once the PLL is locked, the areas "A" and "B" in Fig. 9 are exactly the same, because the output charge accumulated by $I_{UP}$ is exactly discharged by $I_{CHG}$ every cycle while the PLL is locked. In other words, the time over which $I_{UP}$ flows is controlled so that the areas "A" and "B" are the same by the locked PLL. Therefore, the noise elements of IREF, M1,

M2, and M3 in $I_{UP}$ are pulled out by $I_{CHG}$, and this is the principle of the noise cancellation in the proposed CP.

Discharging the capacitor $C_S$ is required in order to achieve sufficient phase offset. If $C_S$ is not discharged sufficiently, the offset current is small and the phase offset is also small. The development of the discharge method is the most significant part of the proposed CP because noise performance greatly depends on the discharging method.

Figure 10 shows the proposed CP circuit during the discharge operation. Figure 12 (b), (c), and (d) show the waveforms of $I_{CPOUT}$, $Q_S$, and $V_{Cs}$, respectively, where $Q_S$ is the charge stored in $C_S$, and $V_{Cs}$ represents the voltage difference between $V_U$ and $V_L$. It is crucial to prevent charge from leaking from $C_S$ during this time because any leak is uncorrelated with the current mirrors and degrades the noise-canceling effect. Therefore, the capacitor $C_S$ is controlled to be disconnected from CPOUT except while being charged, and the voltage follower A1 and switch S3 are used to keep $V_U$ the same as $V_{CP}$ while S1 is turned off. After that, S4 is turned on to discharge $C_S$, and the current flows to the lower electrode of $C_S$ from M7. As a result, $V_L$ is pulled up by this current and $Q_S$ is discharged as shown in Fig. 12 (c) and (d).

**Fig. 11** Transistor sizes in the proposed CP.



**Fig. 12** Timing diagram of the operation of the proposed circuit.

Note that the charge and discharge currents of $C_S$ originate from current sources M4 and M7, respectively, and both current sources copy the current of M3. The common noise elements included in the charge and discharge currents (i.e. the noise of IREF, M1, M2, and M3) can be canceled in the proposed CP. Thus, additional noise-canceling effects are obtained, and the noise performance of the proposed CP is further improved compared with conventional CPs.

### 3.2 Device Size Considerations of the Proposed CP

Figure 11 shows a circuit diagram of the proposed noise-

cancelling CP including the example of the transistor sizes. First, M1, M2, and M6 can be designed small because they are not dominant noise sources. Next, the size of M3 can be reduced because of the additional noise-canceling effect of the proposed CP. Finally, it is necessary to determine the sizes of M4 and M7 carefully to be large enough depending on the target noise specifications. Thus, although many large MOSFETs are needed in a conventional CP, the proposed CP needs only two large MOSFETs and offers an area efficient design.

In actual implementation, incomplete cancellation occurs for the correlated noise contained in $I_{UP}$ and $I_{DCHG}$. Therefore, when this incomplete cancellation is taken into account, extremely small transistors need to be avoided.

### 3.3 Detailed Circuit Operation of the Proposed CP

Figure 12 shows detailed waveforms for the proposed CP. First, S1 and S2 are turned on and charge is drawn into $C_S$ generating the offset current $I_{CHG}$. $V_U$ rises to $V_{CP}$ and $Q_S$ becomes charged, as shown in Fig. 12 (c) and (d). At the same time, S5 is also turned on and the current generated in M7 flows to ground. Next, S1 and S3 are turned off and on, respectively, and $C_S$ is disconnected from the node CPOUT and connected to the voltage follower A1 to keep $V_U$ the same as $V_{CP}$ before the phase comparison. After this, the current pulse $I_{UP}$ is output from M4 to compensate the offset charge. After $I_{UP}$ stops, S5 is turned off and switches S2 and S4 are turned on to discharge $C_S$ by M7. $V_L$ is pulled up by the current of M7 and $Q_S$ is discharged as shown in Fig. 12.

The design consideration when controlling these switches is to prevent unnecessary leaks from $C_S$. Therefore, it is necessary to control the on and off timings of the switches so that the voltage across $C_S$ does not change. For example, in order to maintain $V_U$ when Cs is disconnected from CPOUT via S1, S3 needs to be turned on in conjunction with S1 being turned off. In the same way, S4 needs to be turned on in conjunction with S2 and S5 being turned off the moment Cs is disconnected from ground via S2 to maintain $V_L$ to ground.

These operations are repeated every period of the phase comparison; that is, the operation frequency of S1–S5 is the same as the frequency of the phase comparison. Therefore, S1–S5 need to be designed properly considering whether they can operate at the target reference frequency, since they may become one of the factors that limits the CP operating speed. Although the operation speed using the proposed CP is lower than that using the conventional CP, the proposed CP can operate up to 500 MHz in our simulation, which is sufficient for 100 MHz used in this work.

### 3.4 Simulated Results of Proposed CP

Figure 13 shows simulation results of the CP current noise for conventional and proposed CPs. The simulation results indicate that the in-band noise can be improved because of the additional noise-canceling effect of the proposed CP.
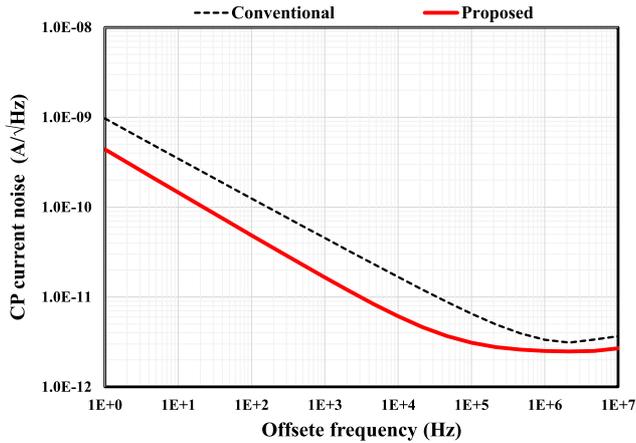
**Fig. 13**   Simulated CP current noise (©2020 IEEE [31]).

**Table 2**   Comparison of noise contributions (©2020 IEEE [31]).

| Noise contributor | Noise contribution (%) | |
|---|---|---|
| | Conventional | Proposed |
| IREF | 9.7 | 14.0 |
| M1 | 0.3 | 0.1 |
| M2 | 7.1 | 2.8 |
| M3 | 16.0 | 2.5 |
| M4 | 23.3 | 31.4 |
| M5 | 39.0 | - |
| M6 | 1.2 | 1.8 |
| M7 | - | 36.5 |
| A1 | - | 4.8 |
| Switches | 3.4 | 6.2 |

These simulations were executed using periodic noise analysis under conditions equivalent to the loop being locked, which means that the input phase error of the PFD between the reference clock and feedback clock are set so that the output charge equals zero. The sizes of IREF, M1, M2, M3, M4, and M6 are the same in each CP with only the offset generator differing for easy comparison.

Table 2 shows the noise-contribution ratio for the simulation results for the conventional and proposed CPs shown in Fig. 13. In the conventional CP, the contribution of M5 is the highest and the contributions of M4, M3, and M2 are higher, as we expected. In the proposed CP, the contribution of M7 is the highest, and the contribution of M4 is the second, that is, M7 and M4 are the dominant noise sources in the proposed CP as expected. In these simulation circuits, IREF was designed with the approximately minimum size of PMOSFET because the noise of IREF can be canceled. However, IREF cannot be cancelled completely in actual simulations and represents a slightly high contribution in both CPs.

It is necessary to consider the noise contributions of the additional switches and the voltage follower in the proposed CP. However, these components can be designed using smaller transistors compared with the current-source

transistors in the conventional CP because of the relatively small noise contributions of the switches and voltage follower as shown in Table 2.

Figure 14 shows simulation results for the relation between occupied area and integrated current noise for the proposed and conventional CPs. These data were plotted by sweeping the transistor sizes of the current sources in CP and simulating the CP current noise. It can be clearly seen that lower-noise performance can be realized with smaller occupied areas by using the proposed CP. The proposed CP can reduce the value of the current noise to 57% for the same occupied area. When the same noise performance is required, the occupied area of the proposed CP can be reduced to 22% compared with the conventional CP. Moreover, although the lower limit of current noise of the conventional CP is about 9.18 nArms, a noise current value of 8.05 nArms can be achieved using the proposed CP with small occupied area.



**Fig. 14**   Simulation results for relation between CP area and CP noise (©2020 IEEE [31]).

## 4.   Experimental Results

We fabricated a prototype of the proposed CP embedded in a 28-GHz LC-PLL using a 16-nm FinFET process. Both conventional and proposed CPs were implemented and selectable by changing the mode to evaluate the effectiveness of the proposed CP. The frequency of the reference clock is 100 MHz. It was generated by doubling the 50-MHz fundamental frequency of the crystal oscillator considering the suitability for mass production in terms of its cost and availability. The power-supply voltage of the PLL is 0.9 V. The die micrograph is shown in Fig. 15. The fully integrated PLL occupied an area of $280\,\mu m \times 340\,\mu m$, and the area occupied by the CP is only $140\,\mu m \times 45\,\mu m$. In order to achieve the same noise performance using the conventional CP, a CP area of at least 4.5 times is required according to estimates in Fig. 14. This difference in area occupied by the CPs has a large impact on the area occupied by the whole PLL.

The measured output phase noise of the PLL is shown in Fig. 16. The red line shows the phase noise using the pro-
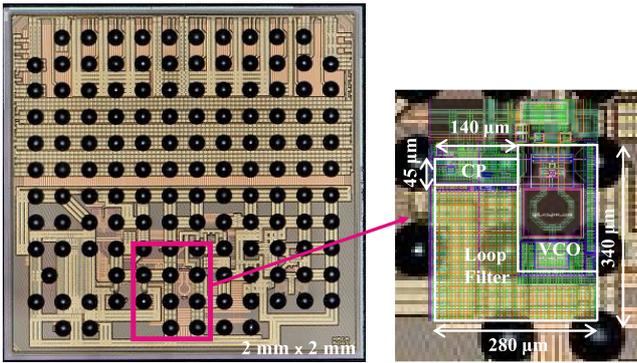
**Fig. 15**     Die micrograph (©2020 IEEE [31]).



**Fig. 17**     Simulated phase noise profile with breakdown of each block.



**Fig. 16**     Measured PLL phase noise (©2020 IEEE [31]).
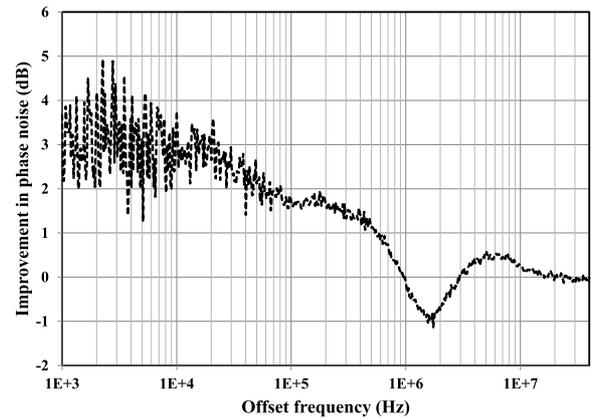


**Fig. 18**     Improvements in phase noise.

posed CP showing that in-band phase noise is suppressed compared with that using the conventional CP. Single sideband integrated phase noise from 1-kHz to 40-MHz offset frequency is improved by 1.2 dB. The dashed line in Fig. 16 shows the simulated phase noise of the PLL using the proposed CP. The measured phase noise of the proposed PLL is close to the simulation result. Figure 17 shows the simulation results, including the breakdown of noise in the PLLs with proposed and conventional CPs. Except for the CPs, the other blocks are common to both PLLs. It is clear that the improvement in the in-band phase noise is due to the improvement in the CP noise owing to the additional noise-canceling effect of the proposed CP. These measurements were made by evaluating the PLL output signal after division by four using a Keysight E5052A signal source analyzer.

Figure 18 shows the calculation results for the difference between the two phase noise curves in Fig. 16 in each offset frequency. It can be seen that the phase noise is improved in all regions inside the loop bandwidth (1.0 MHz) with a maximum improvement value of 4.9 dB at 2.2-kHz offset. The phase noise of the PLL using the proposed CP is degraded in the region from 1-MHz to 3-MHz offset, it is due to the slight difference in the loop bandwidth. The effective gain of the PFD with the conventional CP was smaller than the proposed one because the $I_{UP}$ is reduced by $I_{offset}$



**Fig. 19**     Comparison of measured spurs.

during phase comparison in the conventional CP as shown in Fig. 6 (c), but $I_{UP}$ is not reduced during phase comparison in the proposed CP as shown in Fig. 9 (c). Therefore, the loop bandwidth was a little wider in the PLL with the proposed CP and phase noise is slightly degraded compared to the PLL with the conventional CP in the region from 1-MHz to 3-MHz offset.

We measured the spurs in order to check the effects of the additional operations of switches in the proposed CP. Figure 19 shows measured reference spurs of the PLL using

**Table 3** Performance summary

| CP mode | Conventional | Proposed |
|---|---|---|
| Process | 16nm FinFET | |
| Reference frequency | 100 MHz | |
| VCO oscillation frequency | 28 GHz | |
| Power-supply voltage (PLL) | 0.9 V | |
| Chip area | 2.0 mm x 2.0 mm | |
| PLL area | 280 um x 340 um | |
| CP area | 140 um x 45 um | |
| Total power consumption of PLL | 10.0 mW | 11.2 mW |
| Reference spur (100 MHz offset) | -56.9 dBc | -56.5 dBc |
| Phase noise (1 kHz offset) | -78.5 dBc/Hz | -82.2 dBc/Hz |
| Phase noise (10 kHz offset) | -88.2 dBc/Hz | -91.6 dBc/Hz |
| Phase noise (100 kHz offset) | -91.0 dBc/Hz | -92.7 dBc/Hz |
| Phase noise (1 MHz offset) | -97.1 dBc/Hz | -97.0 dBc/Hz |
| Integrated jitter (1 kHz - 40 MHz offset) | 848 fs | 735 fs |
| FoM* | -231.4 dB | -232.2 dB |

*FOM = $10\log_{10}(\sigma_{jijtter}^2 * \text{Power}/1\text{mW})$

the conventional and proposed CPs. Since there was almost no difference between the two lines in Fig. 19, the spurs using the proposed CP were virtually not degraded owing to the additional switching operations. It is assumed that the additional operations of the switches have less effect on the spurs because the number of switches directly connected to CPOUT is only one (S1) as shown in Fig. 7 and the current flowing through the switch is small enough. The spurs were caused by sharing the power supplies of the VCO, crystal oscillator, and other PLL blocks in the prototype. The spur at 50-MHz offset was due to the fundamental frequency of the crystal oscillator, and other spurs such as 200-MHz, 300-MHz, and 400-MHz offsets were primarily due to harmonic frequencies. These measurements were made by evaluating the PLL output signal after division by four using a Keysight N9020A signal analyzer.

Finally, the implementation and measurement results are summarized in Table 3. At 28-GHz output and 0.9-V supply, the measured RMS integrated jitter of the PLL using the conventional and proposed CPs was 848 fs at 10.0 mW and 735 fs at 11.2 mW, respectively. The power consumption of the CP increased by 1.20 mW from 0.48 mW to 1.68 mW, and the 98% of the increase was due to the voltage-follower A1 in Fig. 7. Consequently, the FoM of −232.2 dB was achieved with the proposed CP compared to −231.4 dB with the conventional CP.

## 5. Conclusion

We proposed a noise-canceling CP circuit in this paper that employs a capacitor $C_S$ instead of a current source to realize offset phase operation in a low-noise CP. By careful designing the charge and discharge methods of the $C_S$ taking correlations into account, additional noise cancelation was achieved, and the trade-off between occupied area and noise performance was mitigated. The simulated and measured results indicated the effectiveness of the proposed CP. The proposed noise-canceling CP can be applied to re-

cent high-performance communication systems which require low-noise PLLs with small occupied area. In particular, it is effective when high-cost advanced technologies such as FinFET process are used.

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