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Fabrication Process for Superconducting Digital Circuits

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SUMMARY This review provides a current overview of the fabrication processes for superconducting digital circuits at CRAVITY (clean room for analog and digital superconductivity) at the National Institute of Advanced Industrial Science and Technology (AIST), Japan. CRAVITY routinely fabricates superconducting digital circuits using three types of fabrication processes and supplies several thousand chips to its collaborators each year. Researchers at CRAVITY have focused on improving the controllability and uniformity of device parameters and the reliability, which means reducing defects. These three aspects are important for the correct operation of large-scale digital circuits. The current technologies used at CRAVITY permit ±10% controllability over the critical current density (J_c) of Josephson junctions (JJs) with respect to the design values, while the critical current (I_c) uniformity is within $1\sigma = 2\%$ for JJs with areas exceeding 1.0 μm^2 and the defect density is on the order of one defect for every 100,000 JJs.

key words: *superconducting integrated circuits, Josephson junction, fabrication process, controllability, uniformity, defect density*

1. Introduction

The National Institute of Advanced Industrial Science and Technology (AIST) is equipped with a clean room for fabricating devices based on metal superconductors, particularly Nb, which is named CRAVITY (clean room for analog and digital superconductivity) [1]. We are developing and fabricating various types of superconducting devices at CRAVITY, such as superconducting detectors [2], [3], detector readout circuits [4], [5], SQUID (superconducting quantum interference device sensors) [6], quantum annealing machines [7], and digital circuits [8]–[16]. The fabricated devices are supplied to CRAVITY's collaborators both in Japan and abroad. Among our fabricated devices, digital circuits have the longest history and the highest level of integration.

Integrated digital circuits are composed of numerous circuit elements and the parameters of each element must be controlled within certain operating margins. If the value of only one parameter for one element exceeds its tolerance, it can result in fatal error for the circuit. In our experience, important aspects of the digital circuit fabrication process include controllability for achieving the required device parameters, intra- and interchip parameter uniformity, and reliability in terms of minimizing the number of defects to the greatest extent possible.

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In this paper, we focus on the digital circuit fabrication process employed at CRAVITY and our current status with respect to controllability, uniformity, and reliability.

2. Digital Circuit Fabrication Process

We routinely fabricate superconducting digital devices using three types of processes [17]. Figure 1 depicts the device structures fabricated using each type of process. A device structure obtained from the most traditional process, referred to as STP2 [18], is shown in Fig. 1 (a). This structure contains four Nb superconducting layers, including a Nb/Al-AlO$_x$/Nb Josephson junction (JJ) [19], and one Mo resistor layer on a surface-oxidized 3-inch Si wafer. inter-

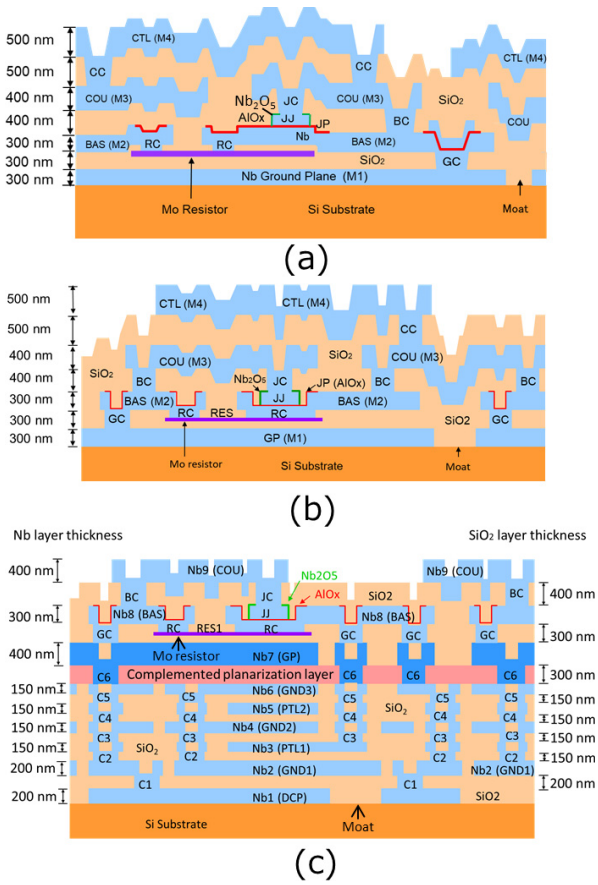

Fig. 1 Schematic device structures fabricated at CRAVITY using three digital circuit fabrication processes: (a) STP2, (b) HSTP, and (c) ADP2. Reprinted with permission from Ref. [17]. © 2017 CSSJ.

layer dielectric is composed of SiO_2. The critical current density (J_c) of the JJ is set to 2.5 kA/cm^2 and the sheet resistance ($R_\square$) is 1.2 Ω. The minimum JJ dimensions and line width are 2 μm × 2 μm and 1.5 μm, respectively.

Figure 1 (b) presents a device structure fabricated using HSTP [20], which is an advanced version of STP2. The layer structure is the same as in STP2, but J_c, $R_\square$, and the minimum JJ dimensions and line width are 10 kA/cm^2, 2.4 Ω, 1 μm × 1 μm, and 1.0 μm, respectively. These parameter values are set to realize higher operation speed. Another difference is that the JJs are positioned on contact holes between the resistor layer and JJ in HSTP, whereas they are placed on the resistor layer in STP2. This placement was adopted to reduce the influence of stress relaxation of the Nb film by generating steps beneath the JJ area [21].

The most complicated process employed at CRAVITY is ADP2, which affords the device structure shown in Fig. 1 (c) [22]. ADP2 devices have nine Nb layers. In ADP2, the Nb layers from the bottom to the seventh layer are planarized using our unique caldera planarization method [23]. The upper two layers, including the JJ layer, are not planarized and these devices have the same structure as HSTP devices except for the absence of a top layer. J_c, $R_\square$, and the minimum sizes are identical to those in HSTP.

CRAVITY supplies several thousand digital chips fabricated using these three processes to its collaborators each year.

3. Process Flow and Evaluation

Figure 2 presents a general process flow diagram for the superconducting integrated circuits with the fabrication machines used in each process [22]. Essentially, the process comprises repeated cycles of film deposition, patterning, etching, washing (photoresist removal), and inspection. We use DC magnetron sputtering for metal deposition and plasma-enhanced chemical vapor deposition (PECVD) for SiO_2 deposition. An i-line stepper is used for the patterning, the performance of which limits the minimum JJ size and line width. Etching is conducted by reactive-ion etching (RIE) using fluorine-based gases such as SF_6 and CHF_3. Cleaning to remove the photoresist following RIE is

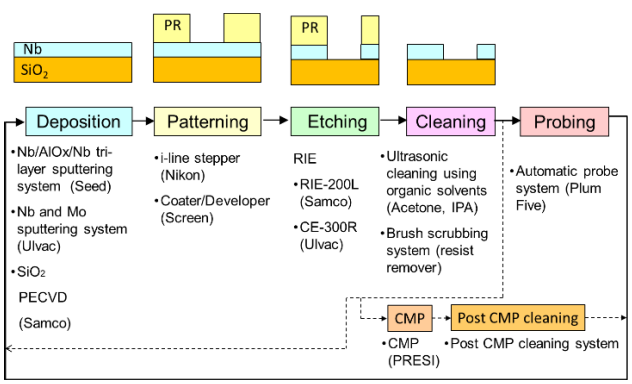

Fig. 2 Fabrication process flow diagram and equipment.

rather important for improving the process reliability. An automatic washing machine involving high-pressure jet injection of 1-methyl-2-pyrrolidone (the photoresist removal solvent), a brush pen, and ultrasonic water is used in the cleaning process. After fabricating the Nb layers at the bottom to the seventh layer in the ADP2 process, Nb patterns are planarized by the caldera planarization method. A chemical mechanical polishing (CMP) machine and a post-CMP cleaning machine are used in the planarization.

Every fabricated wafer includes several process evaluation chips containing various inspection circuits [22]. The room-temperature resistance values of these inspection circuits are measured using an automatic prober system after the formation of each metal layer. The maximum number of probing points is 316 per chip and we can measure nine chips per wafer. Thus, the total number of measurement sites is 2,844 per wafer. The inspection items include defect evaluation such as intra- and interlayer short circuits, JJ resistance, and wiring shrinkage. The evaluation chips also contain circuits for measurements at 4 K, including the critical current (I_c) of the JJ and the resistance (R), inductance (L), and I_c of the superconducting contacts.

4. Controllability of Circuit Parameters

Important circuit parameters in superconducting digital circuits such as single-flux-quantum (SFQ) circuits [24] include I_c, R, and L. These parameters are determined by J_c, JJ area (A), $R_\square$, sheet inductance ($L_\square$), and line width. I_c is the product of J_c and A. R (resp. L) is the product of $R_\square$ (resp. $L_\square$) and the ratio of line length to width. The line length is determined by the design. The operating margin of SFQ circuits depends on the type of circuit and/or the operating frequency. We assume that an operating margin of ±20% should be maintained [25]. Shifts in the fabricated parameters from their design values cause the operating margins to become even narrower. Our target J_c and $R_\square$ values are within ±10% of the design values.

The most difficult parameter to control in the process is J_c, because it is exponentially dependent on the AlO_x tunnel barrier thickness. AlO_x is formed by the thermal oxidation of Al, which is deposited on the Nb base electrode, and the thickness is 10 nm in our process. We use Ar/O_2 (99:1) gas for the oxidation to improve the controllability of the O_2 partial pressure [26]. J_c is determined by controlling the product of the O_2 partial pressure and oxidation time while maintaining the wafer stage temperature at 20°C by flowing temperature-controlled water. As the controllability of J_c is highly sensitive to the process conditions, oxidation pressure is finely tuned by feedback from the latest data. Figure 3 shows the variation of J_c in ADP2 over 18 months, revealing that the J_c values remained within ±10% of the design value (J_c = 10 kA/cm^2). The deviation of the JJ area (A) from its design value was evaluated from the shrinkage caused during patterning and RIE. The shrinkage was extrapolated using several I_c values for JJs that have different A values. As shown in Fig. 3, the shrinkage in ADP2 is

approximately 0.2 μm, which is accounted for in the design values in advance; for example, a 1.0 μm × 1.0 μm JJ is designed as a 1.2 μm × 1.2 μm square [13].

Figure 4 shows the variation of $R_\square$ over 18 months. In general, $R_\square$ remained close to its design value of 2.4 Ω, although it deviated by up to 25% for some of the observation period owing to instrument problems. Figure 5 presents a plot of the shrinkage of the lines in every wiring layer including the resistor layer. We measured these values by extrapolating from the room-temperature resistance values of wiring with various line widths. The greater shrinkage values of the BAS layer, which is the base electrode of the JJs, originated from the Al/Nb layer structure, which differs from the structure of the other wiring layers. We thus consider the shrinkage to be well controlled. To obtain the correct R and L values, this shrinkage is accounted for in the design by using line widths that are 0.2 and 0.1 μm larger than the desired values for the BAS layer and other layers, respectively. Nb in the BAS layer and Nb in other layers are deposited using different sputtering systems. The film quality differs slightly, such as RRR = 5.9 for the BAS sputtering system and RRR = 7.2 for the other system. We suppose that differences in film quality cause the difference in shrinkage.

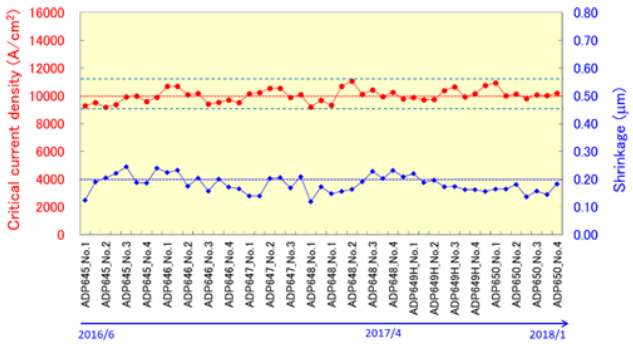

Fig. 3 Variation of J_c and JJ shrinkage in ADP2 over 18 months.

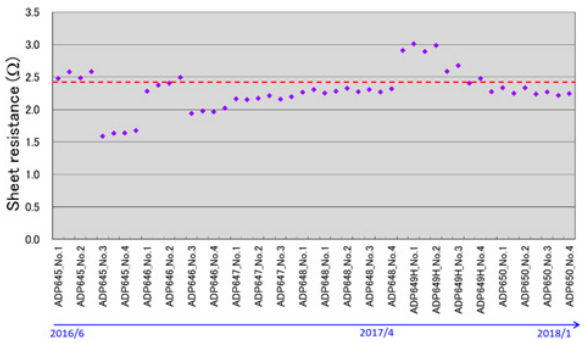

Fig. 4 Variation of $R_\square$ in ADP2 over 18 months.

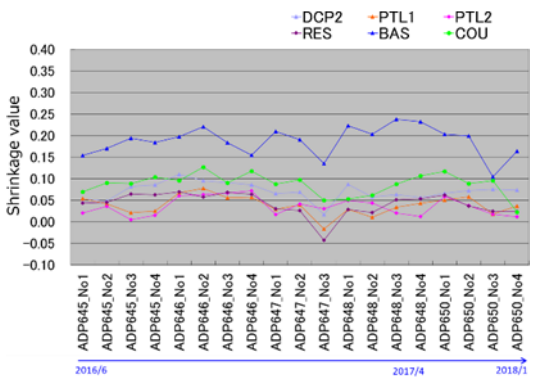

Fig. 5 Variation of shrinkage values for the DCP2, PTL1, PTL2, RES, BAS, and COU layers in ADP2 over 18 months.

5. Parameter Uniformity

Circuit parameter uniformity throughout a wafer and chip is also important for correct circuit operation. Figure 6 shows the variation of experimentally measured J_c values throughout a 3-inch wafer. Here, the same JJ area of 20 μm × 20 μm is assumed in the J_c calculation, regardless of the chip location on the wafer. To confirm the validity of assuming the same JJ area over a 3-inch wafer, we checked the pattern size after the junction etching process with a microscope. Figure 7 shows the evaluation results of the pattern size at position 64 (center) and position 22 (periphery) in Fig. 6. JJ shrinkage does not significantly differ between the center and peripheral chips, as shown in Fig. 7. However, the JJ corners are rounded and the degree is not uniform within a wafer. Therefore, we used large JJs of 20 μm × 20 μm to eliminate almost all A fluctuation due to corner rounding in this experiment. When the JJ was a 1 μm × 1 μm square, all corners were rounded to a circle, resulting in a 21.5%

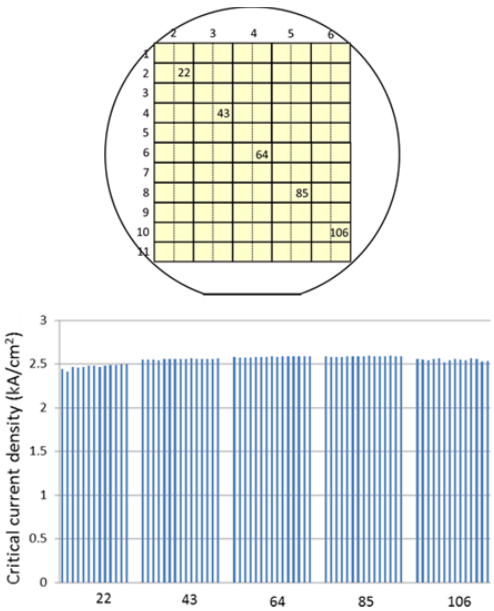

Fig. 6 Variation of J_c throughout a 3-inch wafer. Each bar shows the central J_c value of 100 series-connected 20 μm × 20 μm JJs. The J_c variation of the 100 series-connected JJs was very low. The J_c variation of the central three chips was less than 1%, and the maximum J_c deviation was 5% for the upper-left chip. Reprinted with permission from Ref. [17].

area reduction. For a 20 μm × 20 μm square JJ, on the other hand, the area reduction due to corner rounding was only 0.05%. We estimate that the Josephson penetration depth at J_c of 2.5 kA/cm^2 JJ is 7.6 μm assuming a London penetration depth of 90 nm. The current distribution in the 20 μm × 20 μm JJs was considered to be nearly uniform based on the Josephson penetration depth value [27]. Variation of the J_c values within the 5 mm square chip remained within 1%. The maximum variation throughout the 3-inch wafer was 5%, although the deviation in the J_c values between the central three chips was less than 1% [17].

The I_c uniformity in a chip is predominantly dependent on the variation of A, because J_c remains almost constant throughout a chip as shown in Fig. 6. Figure 8 presents the best results obtained at CRAVITY. This plot shows 1σ of I_c variation for smaller JJs that have areas of less than 1.5 μm^2.

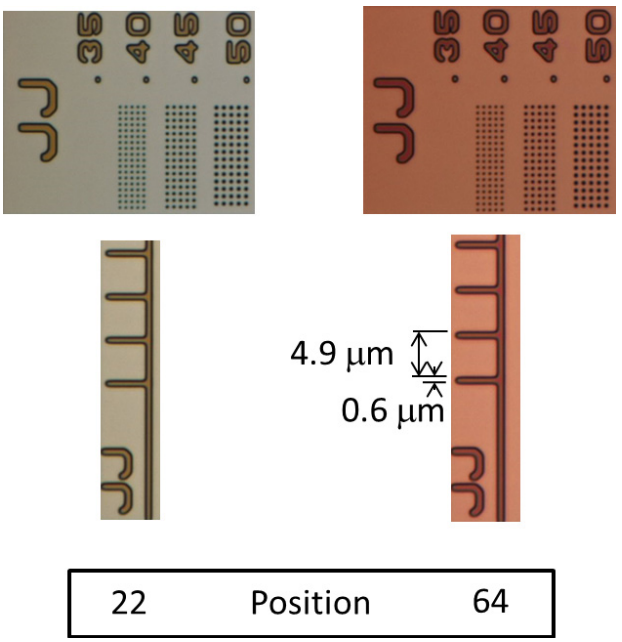

Fig. 7 Microscopic photographs of size evaluation patterns at positions 64 and 22 in Fig. 6. No significant difference was observed in these figures.

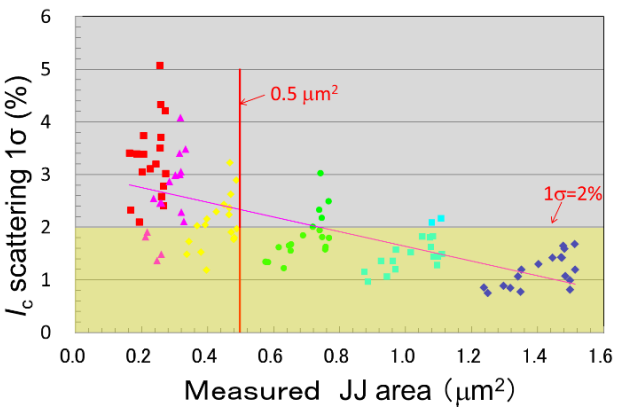

Fig. 8 Dependence of I_c variation on JJ area A. Reprinted with permission from Ref. [17]. © 2017 CSSJ.

The I_c uniformity deteriorated further for smaller A values. This uniformity was measured from the I_c slopes of the I–V curves of 1,000 series-connected JJs fabricated in several runs. The I_c variation for the JJs with areas exceeding 1.0 μm^2 remained less than 2%. If we apply the criterion that 1σ must be less than 2% for large-scale digital circuits, A = 0.5 μm^2 is the lowest limit for obtaining such circuits [28], [29].

The uniformities of R and L were hardly affected by the patterning and etching processes, because R and L are sufficiently wide compared with their shrinkage values. As the Mo thickness is almost uniform throughout the 3-inch wafer used in our process, $R_\square$ remains constant within 1σ = 1%. This is confirmed by room-temperature measurements of nine process evaluation chips in each wafer. The L values depend on the SiO_2 thickness, which is controlled to less than 1σ = 2% in a wafer. Thus, the L uniformity is also excellent.

6. Process Reliability

We estimate the process reliability using the process evaluation chips. The defects are intra- and interlayer short and open circuits. When certain specific defects are detected during this evaluation, we take measures to repair them. The number of defects detected using the nine process evaluation chips in a wafer is less than 10 in the better cases and approximately 20 in the worst cases. These values demonstrate the high reliability of the processes used at CRAVITY; as the total number of detection points is 2,110, the process evaluation chips can include multiple patterns that are more difficult to fabricate than those used in real circuits, and the defects are typically detected in the peripheral area of wafers [22].

Shift register chips for process evaluation are also mounted in every fabrication wafer. In ADP2, the shift register chips contain 16 shift register circuits consisting of six types of shift registers with different bit numbers from 16 to 2,560 bits, and the total number of JJs in the chip is 68,990 [22]. We observed a dramatic improvement in the process reliability upon changing the SiO_2 deposition method from bias sputtering to PECVD. Figure 9 presents the yields of the shift register circuits in six chips in each of two wafers prepared using the two deposition methods. The yields were superior for the wafer in which SiO_2 was deposited by PECVD. We have demonstrated that this yield improvement mainly originates from reduction of the num-

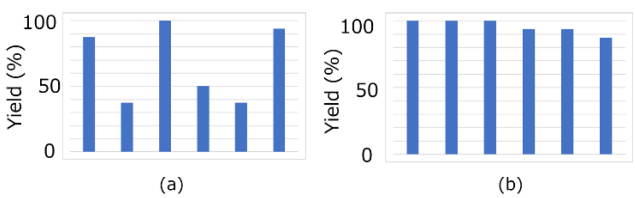

Fig. 9 Shift register yields of six chips in each of two wafers, in which the SiO_2 was deposited by (a) bias sputtering and (b) PECVD.

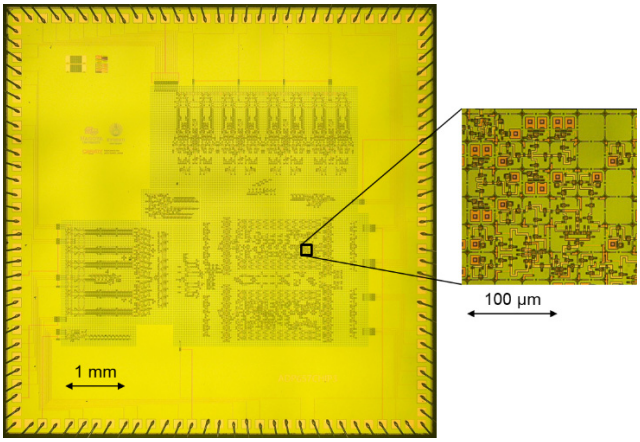

Fig. 10 SFQ gate-level-pipelined processor consisting of 25,477 JJs fabricated using ADP2. This circuit can be operated at up to 32 GHz.

ber of small particles beneath the JJs [30]. The small particles cause an increase in I_c to beyond the operating margin and cause malfunctions in the shift resistor circuits. The I_c increase due to small particles is also regarded as a process defect. We have also determined that the defect rate in CRAVITY digital circuits is approximately one defect in every 100,000 JJs on the basis of the detection of four defects across six chips containing 413,940 JJs in total [22].

We have fabricated numerous superconducting digital circuits, such as the SFQ gate-level-pipelined 4-bit processor designed by researchers at Kyushu University and Nagoya University (Fig. 10), which was prepared using ADP2 and was confirmed to operate correctly at 32 GHz [31]. This processor consists of 25,477 JJs and multiple circuit elements. This result demonstrates that all of the parameters of the superconducting digital circuit, such as I_c, R, and L, fall within the designed operating margin and that no defects such as open circuits or short circuits are present in the chip.

7. Conclusion

CRAVITY at AIST is used to fabricate superconducting integrated circuits with improved parameter controllability, uniformity, and process reliability. These aspects are routinely monitored throughout every fabrication step using the process evaluation chips and measurements conducted at 4 K with liquid He. At present, the process parameters can generally be controlled to within ±10% of the target values, the parameter uniformities are sufficient for digital circuit operation, the number of defects is on the order of one defect in every 100,000 JJs, and SFQ circuits containing tens of thousands of JJs operate correctly at clock frequencies up to several tens of gigahertz. To further improve the CRAVITY process and realize more advanced superconducting digital circuits, upgrading the process environment and fabrication machines will be necessary.

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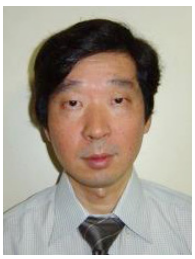

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