

4-Cycle-Start-Up Reference-Clock-Less Digital CDR Utilizing TDC-Based Initial Frequency Error Detection with Frequency Tracking Loop

Tetsuya IIZUKA^{†,††a)}, Senior Member, Meikan CHIN^{††}, Nonmember, Toru NAKURA^{†††b)}, Member, and Kunihiro ASADA^{††}, Senior Member

SUMMARY This paper proposes a reference-clock-less quick-start-up CDR that resumes from a stand-by state only with a 4-bit preamble utilizing a phase generator with an embedded Time-to-Digital Converter (TDC). The phase generator detects 1-UI time interval by using its internal TDC and works as a self-tunable digitally-controlled delay line. Once the phase generator coarsely tunes the recovered clock period, then the residual time difference is finely tuned by a fine Digital-to-Time Converter (DTC). Since the tuning resolution of the fine DTC is matched by design with the time resolution of the TDC that is used as a phase detector, the fine tuning completes instantaneously. After the initial coarse and fine delay tuning, the feedback loop for frequency tracking is activated in order to improve Consecutive Identical Digits (CID) tolerance of the CDR. By applying the frequency tracking architecture, the proposed CDR achieves more than 100 bits of CID tolerance. A prototype implemented in a 65 nm bulk CMOS process operates at a 0.9–2.15 Gbps continuous rate. It consumes 5.1–8.4 mA in its active state and 42 μ A leakage current in its stand-by state from a 1.0 V supply.

key words: clock-and-data recovery (CDR), time-to-digital converter (TDC), serial communication, quick start-up, internet-of-things

1. Introduction

A Clock-and-Data Recovery (CDR) circuit, which recovers the clock signal from the incoming random data sequences to retime the data, is one of the crucial building blocks in data communication devices [1], [2]. Though a Phase-Locked Loop (PLL) based architecture is often used for CDR [3]–[11], it usually requires long settling time to recover the target clock signal. In the applications that keep communicating for a long period of time, the performance overhead in this start-up is not of critical concern. However, in some applications that work intermittently such as mobile and Internet-of-Things (IoT) sensor node applications [12], [13], the effective usage of a low-power stand-by state is important as well as a dynamic power efficiency in

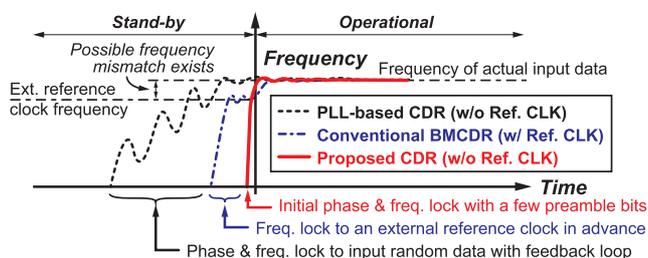


Fig. 1 Conceptual comparison of frequency-locking behavior among three CDR architectures.

an active state. Thus, in such cases, the data link has to resume its communication immediately after it is activated not to waste power for state transitions.

To realize quick start-up, several different CDR architectures have been proposed [14]–[20]. Among them a burst-mode CDR (BMCDR) has been used in point-to-multipoint fiber serial communications such as passive optical networks (PON), in which a quick phase locking is crucial [20]–[26]. As a BMCDR can effectively utilize a low-power stand-by state thanks to its quick start-up feature, it can be considered as a useful choice to realize energy-efficient serial communication systems. Figure 1 conceptually compares start-up features of the CDR techniques. The conventional reference-less PLL-based CDR precisely but slowly locks to the input signal, while the BMCDR can reduce the wait time for phase locking and saves power during the start-up. However, most of the conventional BMCDRs use an external reference clock and need to lock to a predetermined frequency prior to the actual random data input. Thus, these BMCDR techniques still require some dynamic power consumption even in the stand-by state. In order to eliminate the external reference and *a priori* frequency locking, a reference-clock-less BMCDR scheme utilizing a time-to-digital converter (TDC) based architecture has been proposed [27]. Based on the recent progress in CMOS process scaling, time resolution is becoming more and more superior to a voltage resolution due to the high-speed transistors and the reduced supply voltage [28]–[32]. By fully utilizing the time-domain information, a power-efficient CDR architecture could be realized. This scheme uses a Cycle-Lock Gated ring Oscillator (CLGO) that quickly locks to the input frequency by detecting 1-UI cycle time of the incom-

Manuscript received October 29, 2021.

Manuscript revised February 1, 2022.

Manuscript publicized April 11, 2022.

[†]The author is with Systems Design Lab., School of Engineering, The University of Tokyo, Tokyo, 113–0032 Japan.

^{††}The authors are with The Department of Electrical Engineering and Information Systems, the University of Tokyo, Tokyo, 113–0032 Japan.

^{†††}The author is with Graduate School of Engineering, Fukuoka University, Fukuoka-shi, 814–0180 Japan.

a) E-mail: iizuka@vdec.u-tokyo.ac.jp

b) E-mail: nakura@fukuoka-u.ac.jp

DOI: 10.1587/transle.2021CTP0001

ing data stream utilizing Self-Tunable Digitally-Controlled Delay Lines (ST-DCDLs). By employing coarse-fine hierarchical architecture, it can recover the continuous-rate clock from a stand-by state from 1.40 to 2.06 Gb/s only with a 4-bit preamble. Thus it enables us to quickly capture the incoming data immediately after start-up as shown in Fig. 1. By combining an additional feedback loop for frequency tracking as well as incorporating the fractional delay control scheme, its tolerance to Consecutive Identical Digits (CID) is significantly improved in [33].

These techniques are useful to eliminate dynamic power consumption during the stand-by state while realizing immediate start-up without an external reference clock. In these techniques, however, the dynamic power consumption during the actual data communication is relatively large because fine resolution TDCs with resistive interpolation is required for the fine ST-DCDL. In this paper, we propose a new architecture of the reference-clock-less CDR based on a ST-DCDL with a fine Digital-to-Time Converter (DTC). With the proposed architecture we can reduce the dynamic power consumption during the active state while inheriting the advantage of the quick start-up and frequency tracking features in [33].

The rest of this paper is organized as follows. Section 2 explains the architecture of the proposed CDR and the operating principles of the quick start-up. Then in Sect. 3 the chip fabrication and measurement results are summarized. Finally Sect. 4 concludes this paper.

2. Architecture of the Proposed CDR

A block diagram of the proposed CDR is illustrated in Fig. 2, which is similar to the one in [33]. It consists of a gating circuit, a Vernier Phase Detector (PD), a digital controller and a ST-DCDL with a fine DTC. This CDR recovers a half-rate clock, then the incoming data are latched by both the rising and falling edges of the recovered clock. Thus the serial input data will appear at DATAOUT1 and DATAOUT2 alternately. A detailed block diagram of the CDR circuit is shown in Fig. 3 (a). Though the actual circuit is implemented with a differential configuration, this figure shows a single-ended version for simplicity. The coarse-fine hierarchical structure is chosen for wide frequency tuning range as well as fine resolution. The gating circuit in Fig. 2 is composed of an edge detector and a polarity adaptor that find the data transition then align its rise/fall polarity to the present transition of the recovered clock [19], [27].

The proposed CDR has two operation phases as in [33], *i.e.*, quick start-up and frequency tracking. Figures 3 (b) and (c) respectively highlight the active blocks in these two operation phases. During the initial quick start-up phase, by using “1010” 4-bit preamble, 1-UI cycle time is detected with the coarse ST-DCDL and the Vernier TDC. Then in the frequency tracking phase, the Vernier PD and the digital controller are activated to enable the feedback loop.

A schematic diagram of the trigger generator is illustrated in Fig. 4. During the quick start-up phase, the trigger

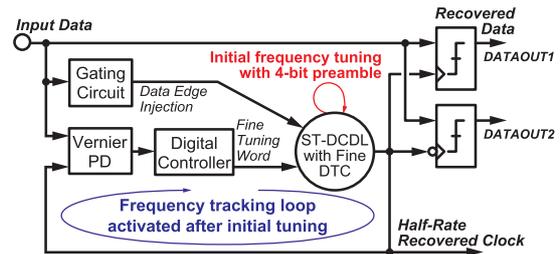
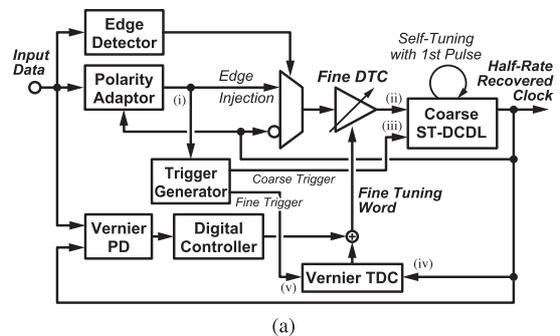
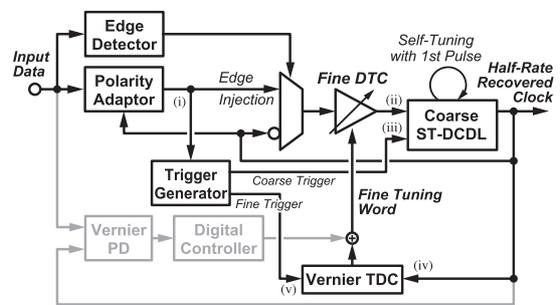


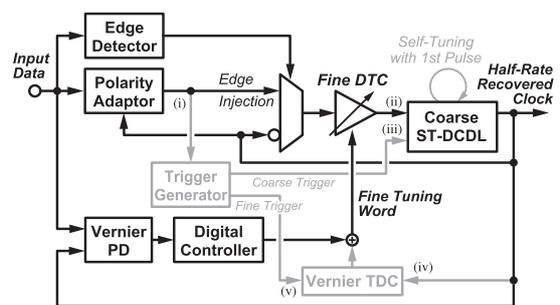
Fig. 2 The proposed CDR architecture based on cycle-lock gated-oscillator (CLGO) with frequency tracking loop.



(a)



(b)



(c)

Fig. 3 (a) A detailed block diagram of the CDR circuit. Gray-colored blocks in (b) and (c) are disabled during quick start-up and frequency tracking phases, respectively.

generator sends trigger signals to the coarse ST-DCDL and the Vernier TDC by detecting the 1st and 2nd falling transitions in “1010” 4-bit preamble signal, respectively. Simulated waveforms during the quick start-up phase are shown in Fig. 5. The coarse trigger signal rises at the first falling edge of the positive input (red line of the top waveform).

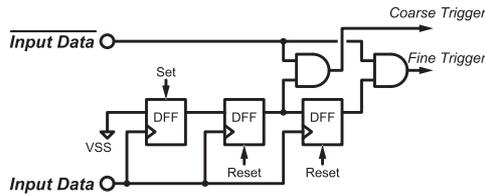


Fig. 4 A block diagram of the trigger generator.

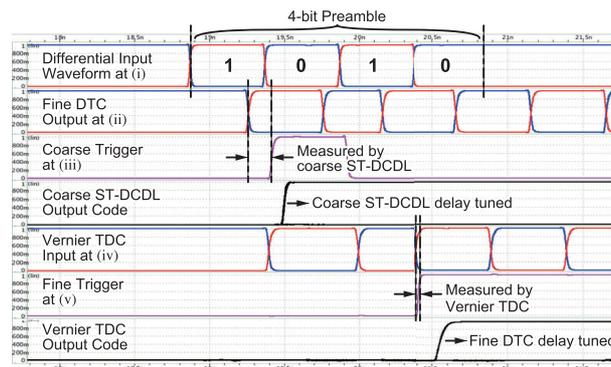


Fig. 5 Simulated waveforms during the quick start-up phase. The node names from (i) to (v) correspond to those in Fig. 3.

The time difference between the fine DTC output and the coarse trigger is measured by the ST-DCDL, so that the total delay through the MUX, the fine DTC and the coarse ST-DCDL in Fig. 3 is coarsely tuned to be 1-UI time interval. After that, at the second falling edge of the positive input, the fine trigger signal rises to measure the residual time difference between the output of the coarse ST-DCDL and the fine trigger by using the Vernier TDC. Then the fine DTC tunes the delay according to the code from the Vernier TDC to generate a finely-tuned half-rate recovered clock waveform.

To make this circuit recover the half-rate clock, the signal path delays must be designed properly so that the internal TDCs can detect the correct delays. But the process, voltage and temperature (PVT) variations would cause the delay mismatch between different signal paths that may lead to erroneous TDC outputs. Thus the circuits need to be delay-matched and are designed with large-enough transistor sizes using the same circuit structures as much as possible in order to mitigate the impact of the PVT variations within the range that can be taken care by the frequency tracking feedback loop, which will be activated after the quick start-up phase.

Figure 6(a) shows a block diagram of the ST-DCDL, which is simply composed of a delay-line-based TDC. Its input-to-output delay is tunable by selecting one of the outputs of the delay line through the internal MUX. As it shares the single delay line to measure and generate the delay, the ST-DCDL tunes the delay by itself by utilizing the output code from the internal TDC. As shown in Fig. 6(b) the buffer circuit for the coarse delay line is implemented with a pseudo differential buffer with switches to disable the out-

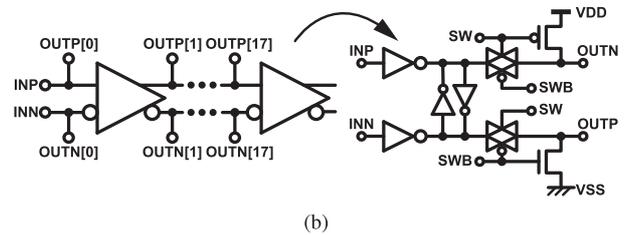
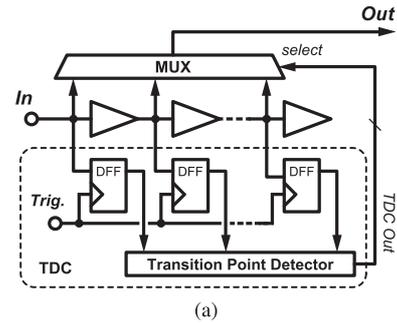


Fig. 6 (a) A schematic diagram of the ST-DCDL and (b) a detailed schematic diagram of the coarse delay buffer.

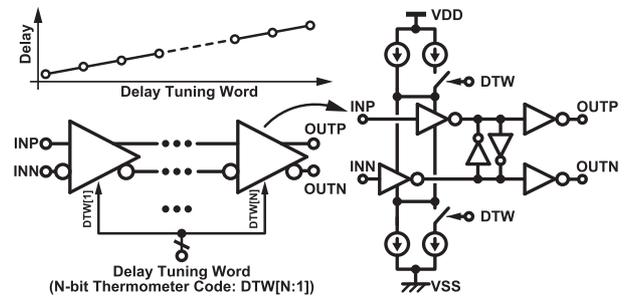


Fig. 7 Schematic diagrams of the fine DTC.

puts. Once the coarse 1-UI time interval detection is finished and the ST-DCDL selects the proper output, the buffers for more delay will be disabled by turning off these switches to save power.

Figure 7 illustrates the schematic diagrams of the fine DTC, which is composed of a series connection of pseudo differential buffers with 1-bit delay tunability. By turning on and off one of the two current source/sink, each buffer stage can finely change its delay between fast and slow settings. With N stages of this buffer tuned with a thermometer coded delay tuning word as shown in Fig. 7, we can achieve a digitally tunable delay with fine resolution while its monotonicity is guaranteed.

A schematic diagram of the Vernier TDC used to detect the residual time difference after coarse tuning is illustrated in Fig. 8. In a Vernier TDC, two delay lines with delay difference of Δt is used to achieve a fine time resolution of Δt [29]. Here in this implementation, the same buffer circuit used in the fine DTC in Fig. 7 is employed to realize two different delays. The slower delay line (the upper one in Fig. 8) uses the slow setting by turning off the internal current sources, while the faster delay line (the lower one)

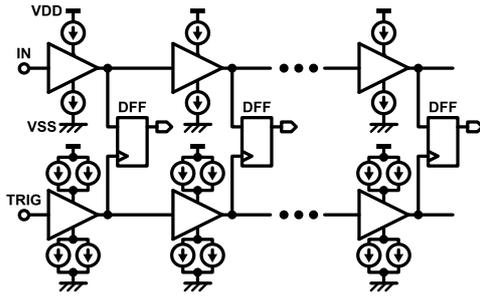


Fig. 8 A schematic diagram of the Vernier TDC.

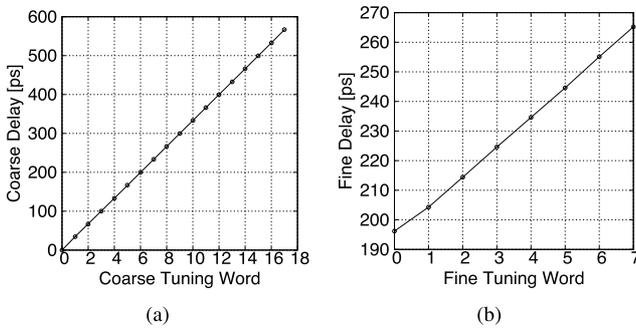


Fig. 9 Delay step simulation results of (a) coarse and (b) fine delay lines.

uses the fast setting by turning on the current sources. By sharing the same 1-bit tunable delay buffer, the time resolution of the Vernier TDC Δt matches by design with the tuning resolution of the fine DTC. In other words, the digital output code from the Vernier TDC, as a result of measuring the residual time difference, can be directly used in the fine DTC to reproduce the same delay to tune the clock frequency. By realizing the same time resolution with the shared buffer circuit, the proposed CDR tunes the fine delay instantaneously without any processing delay in the quick start-up phase. Thus we can maintain the benefit of 4-cycle start-up as in [27], [33] also with the proposed CDR architecture. Of course, due to PVT variations, the actual delay resolution of the Vernier TDC and the fine DTC may be slightly different that leads to tiny delay error in the recovered clock. This remaining error will be taken care by the frequency tracking loop activated after the initial lock, which will be explained later in this section.

Figure 9 shows the simulation results of the delay resolutions of the coarse and fine delay tuning. The ST-DCDL achieves ~ 33 ps/step delay resolution while the fine DTC realizes ~ 10 ps/step.

To tune these coarse and fine delays, the proposed CDR requires a 4-bit “1010” preamble at the start-up. As shown in Fig. 10, at the 1st falling edge in the preamble the coarse trigger is asserted and the ST-DCDL coarsely tunes itself by measuring the 1-UI pulse width using its internal TDC. Then at the 2nd falling edge, the fine trigger is asserted to measure the residual delay difference with the Vernier TDC. In the quick start-up phase, the output code from the Vernier TDC is directly fed to the fine DTC to tune the delay in-

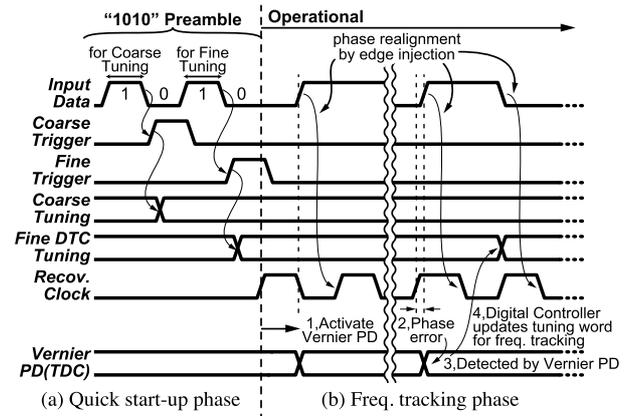


Fig. 10 Conceptual waveforms of the proposed CDR operation.

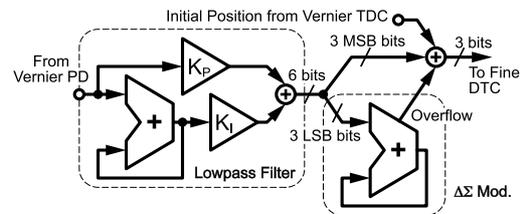


Fig. 11 A block diagram of the digital controller.

stantaneously thanks to the shared buffer structure with the same time resolution. Now we can have a finely tuned recovered clock. However, this initially-tuned delays might contain certain amount of error due to PVT variations and jitter, as well as the input frequency drift. This frequency error accumulates as phase error and results in poor CID tolerance. Thus, as in [33], a feedback loop for frequency tracking shown in Figs. 2 and 3 is activated after the initial clock recovery process. After activating the feedback loop, the Vernier PD, which uses the same Vernier TDCs, detects the phase error between the incoming data and the recovered clock as illustrated in Fig. 10 (b). The PD output is processed by the digital controller whose block diagram is shown in Fig. 11. The digital controller realizes a lowpass characteristic with output dithering by the $\Delta\Sigma$ modulator to effectively improve the frequency resolution. The output of the digital controller is fed to the fine DTC to achieve frequency tracking.

3. Chip Implementation and Measurement Results

The prototype of the proposed CDR is fabricated in a 65 nm bulk CMOS process, whose chip micrograph and layout image are shown in Fig. 12. The proposed CDR occupies $98 \times 157 \mu\text{m}^2$ area. The CDR operation is verified from 0.90 to 2.15 Gb/s continuous rate while it consumes 5.1–8.4 mA current from 1.0 V supply. The measured leakage current during the stand-by state is $42 \mu\text{A}$.

Firstly, the 4-cycle start-up behavior of the proposed CDR is verified as shown in Fig. 13. After “1010” 4-bit preamble input, it successfully recovers the clock and data.

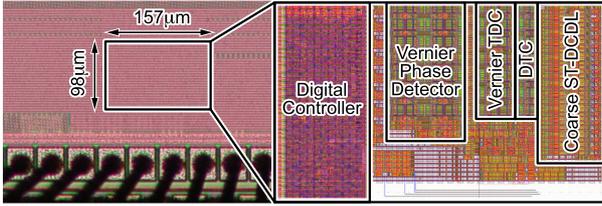


Fig. 12 Chip micrograph and layout of the proposed CDR.

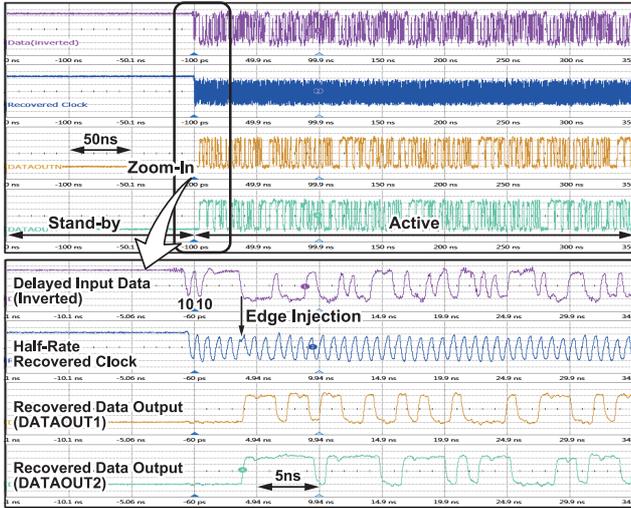


Fig. 13 Measured waveforms of the 4-cycle start-up behavior at 2.15 Gb/s input.

As shown in Fig. 2, the incoming data are latched by both the rising and falling edges of the half-rate recovered clock. Thus the serial input data will appear at DATAOUT1 and DATAOUT2 alternately. We can also observe that the transition edge in the incoming data is injected to realign the phase of the recovered clock. Figure 14 shows the measured eye diagrams of the input data and the half-rate recovered clock signals in the cases of without and with the dithering in the digital controller. The clock jitter is $\sim 19.3 \text{ ps}_{\text{rms}}$ and $\sim 17.4 \text{ ps}_{\text{rms}}$ for the cases without and with the dithering, respectively. Figure 15 compares the CID tolerance measurement results between the cases without and with the dithering. Before and after the intentional consecutive 0 and 1 input at the middle of the waveforms, PRBS data sequence is injected to the circuit. The CID tolerance improves from 44 bits to 102 bits by enabling the dithering in the digital controller. These results demonstrates that the dithering effectively improves the frequency tuning resolution, which leads to better frequency tracking capability. Figure 16 shows the jitter tolerance measurement result. Especially for high-frequency jitter, the proposed CDR has relatively poor jitter tolerance. This is mainly because the frequency characteristic of the digital LPF is not well optimized and the authors expect that it can be improved by carefully tuning the parameters in the digital controller. It would also be possible to gather more insight to improve the CDR performance by investigating in detail on the loop dynamics.

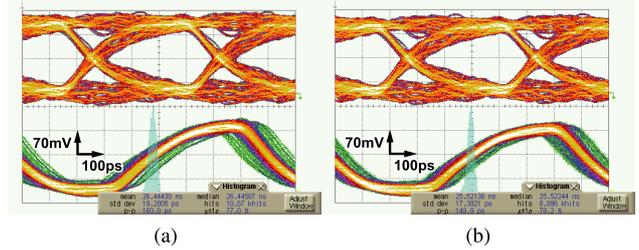


Fig. 14 Measured waveforms of the input data and recovered clocks for 2.15Gb/s inputs (a) without and (b) with dithering in the digital controller.

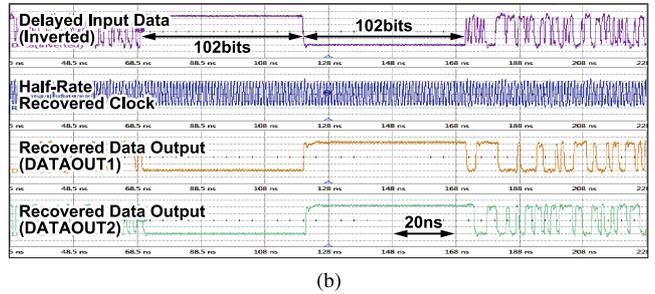
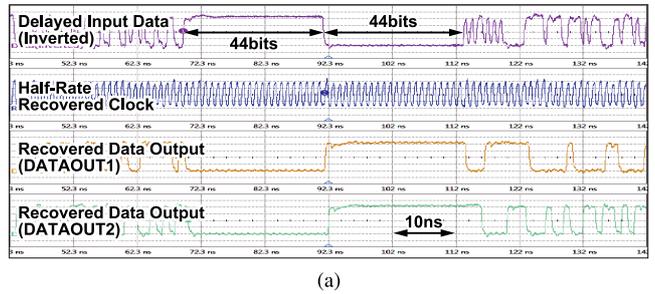


Fig. 15 CID tolerance measurement results at 2.0 Gb/s input (a) without and (b) with dithering.

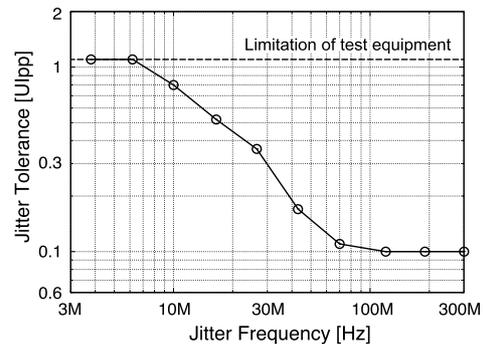


Fig. 16 Jitter tolerance measurement result with 2.0 Gb/s PRBS7 input. Bit error rate of 10^{-9} is used as a criterion of pass/fail.

These are included in our future works.

Finally, Table 1 compares the proposed work with similar prior works. The proposed CDR does not require an external reference clock and the frequency lock prior to the data input, which leads to the immediate start-up with no dynamic power consumption during the stand-by state. Especially compared with [33], the proposed CDR reduces the

Table 1 Performance comparison with prior works.

Ref.	[17]	[18]	[27]	[33]	This Work
CDR Scheme	GVCOW/ FLL	GDCOW/ FLL&PLL	ST-DCDL	ST-DCDL w/ FLL	ST-DCDL w/ Fine DTC&FLL
Tech. [nm]	55	90	65	65 (FD-SOI)	65
Supply [V]	3.3/1.2	N/A	1.4	1.2	1.0
Rate [Gb/s]	2.5	2.2	1.40–2.06	1.2–2.3	0.90–2.15
Power [mW]	13.68	6.1	9.5	13.2–24.6	5.1–8.4
Area [mm ²]	0.04	0.44	0.0064	0.019	0.015
CID Tol.	253bits	128bits	13bits	292bits	102bits
Freq. Lock	Prior to data	Prior to data	4bit	4bit	4bit
Phase Lock	<1bit	<1bit	<1bit	<1bit	<1bit
Ref. Clock	Required	Required	No	No	No
Stand-by Power	Yes	Yes	No	No	No

dynamic power consumption during the active state about $3\times$ while maintaining the same benefits of the 4-cycle quick start-up as well as the wide-range continuous-rate frequency tracking features. Although the maximum CID tolerance is reduced to 102 bits, this number is large enough because we may be able to choose proper coding schemes such as 64b/66b to have enough transitions by accepting some overhead in the data rate.

4. Conclusion

This paper proposed a reference-clock-less quick-start-up CDR that resumes from a stand-by state only with a 4-bit preamble utilizing the ST-DCDL and the fine DTC whose tuning resolution is matched by design with the internal Vernier TDC. The feedback loop for frequency tracking activated after the initial coarse and fine delay tuning works to achieve more than 100 bits of CID tolerance. A prototype implemented in a 65 nm bulk CMOS process operates at 0.9–2.15 Gbps continuous rate. It consumes 5.1–8.4 mA in its active state and 42 μ A leakage current in its stand-by state from a 1.0 V supply. Since the proposed CDR does not need an external reference clock thus consumes no dynamic power in its stand-by state, it can improve the total power efficiency of serial communication systems that work intermittently such as mobile and IoT sensor node applications.

Acknowledgements

This work is supported in part by a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO) and in part by JSPS KAKENHI Grant Number 21H03406. The LSI chip fabricated in this work has been supported through the activities of VDEC, the University of Tokyo in collaboration with Cadence Design Systems Inc., Synopsys, Inc., and Mentor Graphics, Inc.

References

[1] B. Razavi, "Challenges in the design high-speed clock and data recovery circuits," *IEEE Communications Magazine*, vol.40, no.8, pp.94–101, 2002.

[2] B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw Hill, Chicago, 2002.

[3] M.-t. Hsieh and G.E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," *IEEE Circuits and Systems Magazine*, vol.8, no.4, pp.45–57, 2008.

[4] J.L. Sonntag and J. Stonick, "A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid-State Circuits*, vol.41, no.8, pp.1867–1875, 2006.

[5] J. Poulton, R. Palmer, A.M. Fuller, T. Greer, J. Eyles, W.J. Dally, and M. Horowitz, "A 14-mW 6.25-Gb/s transceiver in 90-nm cmos," *IEEE Journal of Solid-State Circuits*, vol.42, no.12, pp.2745–2757, 2007.

[6] P.K. Hanumolu, G.-Y. Wei, and U.-K. Moon, "A Wide-Tracking Range Clock and Data Recovery Circuit," *IEEE Journal of Solid-State Circuits*, vol.43, no.2, pp.425–439, 2008.

[7] M.H. Perrott, Y. Huang, R.T. Baird, B.W. Garlepp, D. Pastorello, E.T. King, Q. Yu, D.B. Kasha, P. Steiner, L. Zhang, J. Hein, and B. Del Signore, "A 2.5-Gb/s Multi-Rate 0.25- μ m CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition," *IEEE Journal of Solid-State Circuits*, vol.41, no.12, pp.2930–2944, 2006.

[8] D. Dalton, K. Chai, E. Evans, M. Ferriss, D. Hitchcox, P. Murray, S. Selvanayagam, P. Shepherd, and L. DeVito, "A 12.5-mb/s to 2.7-Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback," *IEEE Journal of Solid-State Circuits*, vol.40, no.12, pp.2713–2725, 2005.

[9] R.-J. Yang, K.-H. Chao, S.-C. Hwu, C.-K. Liang, and S.-I. Liu, "A 155.52 Mbps-3.125 Gbps continuous-rate clock and data recovery circuit," *IEEE Journal of Solid-State Circuits*, vol.41, no.6, pp.1380–1390, 2006.

[10] G. Shu, S. Saxena, W.-S. Choi, M. Talegaonkar, R. Inti, A. Elshazly, B. Young, and P.K. Hanumolu, "A Reference-Less Clock and Data Recovery Circuit Using Phase-Rotating Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol.49, no.4, pp.1036–1047, 2014.

[11] G. Shu, W.-S. Choi, S. Saxena, M. Talegaonkar, T. Anand, A. Elkholly, A. Elshazly, and P.K. Hanumolu, "A 4-to-10.5 Gb/s Continuous-Rate Digital Clock and Data Recovery With Automatic Frequency Acquisition," *IEEE Journal of Solid-State Circuits*, vol.51, no.2, pp.428–439, 2016.

[12] Y. Yano, S. Yoshida, S. Izumi, H. Kawaguchi, T. Hirose, M. Miyahara, T. Someya, K. Okada, I. Akita, Y. Kurui, H. Tomizawa, and M. Yoshimoto, "An IoT Sensor Node SoC with Dynamic Power Scheduling for Sustainable Operation in Energy Harvesting Environment," *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp.267–270, 2019.

[13] D. Bol, J. De Vos, C. Hocquet, F. Botman, F. Durvaux, S. Boyd, D. Flandre, and J.D. Legat, "SleepWalker: A 25-MHz 0.4-V Sub-mm² 7- μ W/MHz Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits*,

- vol.48, no.1, pp.20–32, 2013.
- [14] B. Leibowitz, R. Palmer, J. Poulton, Y. Frans, S. Li, J. Wilson, M. Bucher, A.M. Fuller, J. Eyles, M. Aleksic, T. Greer, and N.M. Nguyen, “A 4.3 GB/s Mobile Memory Interface With Power-Efficient Bandwidth Scaling,” *IEEE Journal of Solid-State Circuits*, vol.45, no.4, pp.889–898, 2010.
- [15] K. Maruko, T. Sugioka, H. Hayashi, Z. Zhou, Y. Tsukuda, Y. Yagishita, H. Konishi, T. Ogata, H. Owa, T. Niki, K. Konda, M. Sato, H. Shiroshita, T. Ogura, T. Aoki, H. Kihara, and S. Tanaka, “A 1.296-to-5.184 Gb/s Transceiver with 2.4 mW/(Gb/s) Burst-mode CDR using Dual-Edge Injection-Locked Oscillator,” 2010 IEEE International Solid-State Circuits Conference - (ISSCC), pp.364–365, 2010.
- [16] J. Terada, K. Nishimura, S. Kimura, H. Katsurai, N. Yoshimoto, and Y. Ohtomo, “A 10.3125 Gb/s Burst-Mode CDR Circuit using a $\delta\sigma$ DAC,” 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pp.226–609, 2008.
- [17] C.F. Liang, S.C. Hwu, Y.H. Tu, Y.L. Yang, and H.S. Li, “A reference-free, digital background calibration technique for gated-oscillator-based CDR/PLL,” 2009 Symposium on VLSI Circuits, pp.14–15, 2009.
- [18] W.-S. Choi, T. Anand, G. Shu, and P.K. Hanumolu, “A fast power-on 2.2 Gb/s burst-mode digital CDR with programmable input jitter filtering,” 2013 Symposium on VLSI Circuits, pp.C280–C281, 2013.
- [19] S. Kaeriyama and M. Mizuno, “A 10 Gb/s/ch 50 mW $120 \times 130 \mu\text{m}^2$ clock and data recovery circuit,” 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., vol.1, pp.70–478, 2003.
- [20] B. Abiri, R. Shivanaraine, A. Sheikholeslami, H. Tamura, and M. Kibune, “A 1-to-6 Gb/s phase-interpolator-based burst-mode CDR in 65 nm CMOS,” 2011 IEEE International Solid-State Circuits Conference, pp.154–156, 2011.
- [21] A. Li, J. Faucher, and D. Plant, “Burst-mode clock and data recovery in optical multiaccess networks using broad-band PLLs,” *IEEE Photonics Technology Letters*, vol.18, no.1, pp.73–75, 2006.
- [22] B.J. Shastri and D.V. Plant, “5/10-Gb/s burst-mode clock and data recovery based on semiblind oversampling for pons: Theoretical and experimental,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol.16, no.5, pp.1298–1320, 2010.
- [23] C.-F. Liang and S.-I. Liu, “A 20/10/5/2.5 Gb/s power-scaling burst-mode cdr circuit using GVCO/DIV2/DFF tri-mode cells,” 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pp.224–608, 2008.
- [24] J.M. Lin, C.Y. Yang, and H.M. Wu, “A 2.5-Gb/s dll-based burst-mode clock and data recovery circuit with $4 \times$ oversampling,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.23, no.4, pp.791–795, 2015.
- [25] M.-C. Su, W.-Z. Chen, P.-S. Wu, Y.-H. Chen, C.-C. Lee, and S.-J. Jou, “A 10-Gb/s, 1.24 pJ/bit, burst-mode clock and data recovery with jitter suppression,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.62, no.3, pp.743–751, 2015.
- [26] J. Lee and M. Liu, “A 20-Gb/s Burst-Mode Clock and Data Recovery Circuit Using Injection-Locking Technique,” *IEEE Journal of Solid-State Circuits*, vol.43, no.3, pp.619–630, 2008.
- [27] T. Iizuka, S. Miura, Y. Ishizone, Y. Murakami, and K. Asada, “A true 4-cycle lock reference-less all-digital burst-mode CDR utilizing coarse-fine phase generator with embedded TDC,” *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, pp.1–4, 2013.
- [28] R.B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J.L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I.Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O.E. Eliezer, E. de Obaldia, and P.T. Balsara, “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol.39, no.12, pp.2278–2291, Dec. 2004.
- [29] S. Henzler, *Time-to-Digital Converters*, Springer, Netherlands, 2010.
- [30] K. Asada, T. Nakura, T. Iizuka, and M. Ikeda, “Time-Domain Approach for Analog Circuits in Deep Sub-Micron LSI,” *IEICE Electronics Express*, vol.15, no.6, pp.1–21, March 2018.
- [31] R. Enomoto, T. Iizuka, T. Koga, T. Nakura, and K. Asada, “A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18 μm CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.27, no.1, pp.11–19, 2019.
- [32] T. Iizuka and K. Asada, “Time-Domain Approach for Analog Circuits: Fine-Resolution TDC and Quick-Start CDR Circuits,” 2018 International Conference on Advanced Technologies for Communications (ATC), pp.376–381, 2018.
- [33] T. Iizuka, N. Tohge, S. Miura, Y. Murakami, T. Nakura, and K. Asada, “A 4-cycle-start-up reference-clock-less all-digital burst-mode CDR based on cycle-lock gated-oscillator with frequency tracking,” *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, pp.301–304, 2016.



Tetsuya Iizuka received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2002, 2004, and 2007, respectively. From 2007 to 2009, he was with THine Electronics Inc., Tokyo, Japan, as a high-speed serial interface circuit engineer. He joined the University of Tokyo in 2009, where he is currently an Associate Professor with Systems Design Lab., School of Engineering. From 2013 to 2015, he was a Visiting Scholar with the University of

California, Los Angeles, CA, USA. His current research interests include data conversion techniques, high-speed analog integrated circuits, digitally-assisted analog circuits and VLSI computer-aided design. Dr. Iizuka is a member of the Institute of Electrical and Electronics Engineers (IEEE). He was a member of the IEEE International Solid-State Circuits Conference (ISSCC) Technical Program Committee from 2013 to 2017 and a member of the IEEE Custom Integrated Circuits Conference (CICC) Technical Program Committee from 2014 to 2019. From 2016 to 2018, he served as the Editor of *IEICE Electronics Express (ELEX)*. He is currently serving as a member of the IEEE Asian Solid-State Circuits Conference (A-SSCC) and IEEE VLSI Symposium on Circuits Technical Program Committees. He is a recipient of the 21st Marubun Research Encouragement Commendation from Marubun Research Promotion Foundation in 2018, the 13th Wakashachi Encouragement Award First Prize in 2019 and the 18th Funai Academic Prize from Funai Foundation for Information Technology in 2019. He is a co-recipient of the IEEE International Test Conference Ned Kornfield Best Paper Award in 2016.

Meikan Chin received the B.S. and M.S. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2016 and 2019, respectively. His research interests include design and architecture of wire-line communication circuits.



Toru Nakura was born in Fukuoka, Japan in 1972. He received the B. S., and M. S. degree in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995 and 1997 respectively. Then he worked as a circuit designer of high-speed communication using SOI devices for two years, and worked as a EDA tool developer for three years. He joined the University of Tokyo again as a Ph.D student in 2002, and received the degree in 2005. After two years industrial working period, he is back to academia

as an associate professor at VLSI Design and Education Center (VDEC), and Electrical Engineering and Information Systems, in The University of Tokyo. He is currently working as a full professor in the department of Electronics Engineering and Computer Science in Fukuoka University. His current interest includes signal integrity, reliability, power supply, digitally-assist analog circuits, and fully automated analog circuit synthesis.



Kunihiro Asada was born in Fukui, Japan, in 1952. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1975, 1977, and 1980, respectively. He joined the Faculty of Engineering, University of Tokyo, in 1980, and became a Lecturer, an Associate Professor, and a Professor in 1981, 1985, and 1995, respectively. From 1985 to 1986, he was with the University of Edinburgh, Edinburgh, U.K., as a Visiting Scholar supported by the British Council.

From 1990 to 1992, he served as the first Editor of the English version of IEICE Transactions on Electronics. In 1996, he established the VLSI Design and Education Center (VDEC), with his colleagues in the University of Tokyo, which is the center to promote education and research of VLSI design in all the universities and colleges in Japan. He was in charge of the Director of VDEC until 2018, and is currently a Professor Emeritus at the University of Tokyo. He has authored over 400 technical papers in journals and conference proceedings. His current research interests include design and evaluation of integrated systems and component devices. Dr. Asada is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Institute of Electrical Engineers of Japan (IEEJ). He has received Best Paper Awards from IEEJ, IEICE, and ICMTS1998/IEEE. He also served as the Chair of the IEEE/SSCS Japan Chapter from 2001 to 2002 and the IEEE Japan Chapter Operation Committee from 2007 to 2008.