IEICE TRANS. ELECTRON., VOL.E105–C, NO.5 MAY 2022

PAPER

X-Band GaN Chipsets for Cost-Effective 20 W T/R Modules

Jun KAMIOKA[†a)], **Yoshifumi KAWAMURA**[†], **Ryota KOMARU**[†], ***Members***,
Masatake HANGAI[†], ***Senior Member***, **Yoshitaka KAMO**[††], **Tetsuo KODERA**[†††], ***Nonmembers***,
and **Shintaro SHINJO**[†], ***Senior Member***

SUMMARY This paper reports on X-band Gallium Nitride (GaN) chipsets for cost-effective 20 W transmit-receive (T/R) modules. The chipset components include a GaN-on-Si monolithic microwave integrated circuit (MMIC) driver amplifier (DA), a GaN-on-SiC high power amplifier (HPA) with GaAs matching circuits, a high-gain GaN-on-Si HPA with a GaAs output matching circuit, and a GaN-on-Si MMIC switch (SW). By utilizing either combination of the DA or single high-gain HPA, the configurations of two T/R module types can be realized. The GaN-on-Si MMIC DA demonstrates an output power of 6.4–7.4 W, an associate gain of 22.3–24.6 dB and a power added efficiency (PAE) of 32–36% over 9.0–11.0 GHz. A GaN-on-SiC HPA with GaAs matching circuits exhibited an output power of 20–28 W, associate gain of 7.8–10.7 dB, and a PAE of 40–56% over 9.0–11.0 GHz. The high-gain GaN-on-Si HPA with a GaAs output matching circuit exhibits an output power of 15–30 W, associate gain of 27–30 dB, and PAE of 26–33% over 9.0–11.0 GHz. The GaN-on-Si MMIC switch demonstrates insertion losses of 1.1–1.3 dB and isolation of 10.1–14.7 dB over 8.0–11.5 GHz. By employing cost-effective circuit configurations, the costs of these chipsets are estimated to be about half that of conventional chipsets.

key words: *gallium nitride, high power amplifiers, switches, MMICs*

1. Introduction

Transmit-receive (T/R) modules have been widely utilized in applications such as radar technology and communication systems. Active phased array antennas (APAAs), which enable electrical beam formation, have been applied to radar systems [1] and recently also introduced to communication systems such as fifth-generation mobile communications (5 G) [2]. As APAAs require thousands of T/R modules, the cost of T/R modules accounts for a large portion of the system cost [3]. There is an increasing demand for cost-effective transmit modules with high-performance characteristics. A major contributing factor to the cost of T/R modules is the cost of the monolithic microwave integrated circuits (MMICs) component. As the cost of MMIC is mainly driven by the choice of substrate materials and chip size, cost-effective substrate materials and compact design configurations ought to be considered. To realize high power density outputs and power added efficiency (PAE), GaN-on-SiC high power amplifiers (HPAs) [4]–[10] and switches (SWs) [11], [12] are often utilized. In our previous work [13], measurement results of the GaN-on-Si MMIC DA and the HPA which achieve cost-effective amplifier stages were shown. In addition to the detailed circuit designs of the GaN-on-Si MMIC DA and the HPA, this paper also provides circuit designs and measurement results of the GaN-on-SiC HPA and GaN-on-Si MMIC SW. The concepts of X-band GaN chipsets are proposed, and the design methods and measurement results are shown in Sect. 2 of this paper, with their performance and cost-effectiveness evaluated against advanced MMIC based chipset devices in Sect. 3.

Manuscript received June 1, 2021.
Manuscript revised September 14, 2021.
Manuscript publicized December 10, 2021.

[†]The authors are with Information Technology R & D Center, Mitsubishi Electric Corporation, Kamakura-shi, 247–8501 Japan.
[††]The author is with High Frequency & Optical Device Works, Mitsubishi Electric Corporation, Itami-shi, 664–8641 Japan.
[†††]The author is with Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, 152–8550 Japan.
a) E-mail: Kamioka.Jun@bk.MitsubishiElectric.co.jp

DOI: 10.1587/transele.2021ECP5024

2. GaN Chipsets

2.1 Concepts of GaN Chipsets

A schematic of a targeted T/R module is illustrated in Fig. 1. The chipsets include amplifier stage and SW. The target performance of amplifier stage is an output power of 20 W and gain of 30 dB to configure proper amplifier chain with a typical Si core-chip with the saturate output power of about 15 dBm. The target performances of SW are isolation of 15 dB with high power input up to 20 W considering isolation of a circulator. Transmit modules with such performances are conventionally composed of a GaAs or GaN-on-SiC MMIC DA, a GaN-on-SiC HPA, and a GaN-on-SiC SW [14]–[20]. Another option for an amplifier stage is utilizing a high-gain GaN-on-SiC MMIC HPA [20] instead of the combination of a DA and an HPA. These configurations demonstrate good performance due to high power capability

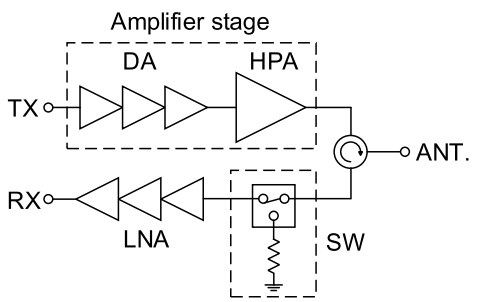

Fig. 1 Schematic of target GaN T/R module with the chipset

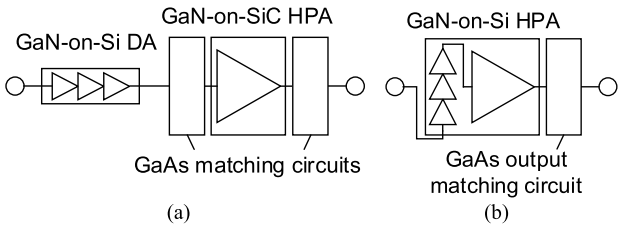

Fig. 2 Schematic of the amplifier stages. (a) Schematic of the proposed case-1 amplifier stage. (b) Schematic of the case-2 amplifier stage.

and high-efficiency characteristic of GaN field effect transistors (FETs). However, the configuration tends to be relatively costly due to the high-cost of GaN-on-SiC substrates. GaAs realizes lower cost to area ratios, but the doubling of sizes is necessary to obtain such a high power of 20 W amplifier because of its lower power density. In this paper, two types of T/R modules are proposed to configure low-cost and high performance. Figure 2 illustrates schematics of proposed amplifier stages wherein one of the proposed amplifier stage is a combination of GaN-on-Si MMIC DA and GaN-on-SiC HPA with GaAs output matching circuit (Case-1) as illustrated in Fig. 2 (a). The power density of GaN-on-Si is as high as that of GaN-on-SiC while the cost to size ratio is comparable with that of GaAs. GaN-on-SiC HPA with GaAs output matching circuit retains the high performance of GaN-on-SiC FETs while matching circuits are realized by GaAs to reduce cost. The other module is composed of a high-gain GaN-on-Si HPA (Case-2) as illustrated in Fig. 2 (b), a DA and an HPA is integrated in a GaN-on-Si chip, and a GaAs output matching circuit is applied. However, the cost of case-2 is lower than that of case-1, whereas, efficiency of case-2 is slightly lower than that of case-1 due to the difference in FET performance. The GaAs output matching circuit is applied to reduce circuit losses compared to those with GaN-on-Si substrate. GaN-on-Si MMIC SW is proposed to reduce the cost and realizes that while retaining high power capability. Circuit design and measurement results of these four devices are shown in detail as follows.

2.2 GaN-on-Si MMIC DA

A GaN-on-Si MMIC DA is designed and fabricated utilizing a 0.25 μm GaN-on-Si process. Figure 3 illustrates a schematic of GaN-on-Si MMIC DA. The DA has three FET stages, with gate peripheries of 0.5 mm for the first stage, 0.7 mm for the second stage, and 1.0 mm × 2 cells for the third stage respectively. R//C stabilization circuits with reduced losses at higher frequencies are utilized to compensate for the gain slope of FETs, which results in the DA with broadband flat gain. As illustrated in Fig. 4 from the dense integration of matching circuits in limited spaces, the DA is carefully designed considering electromagnetic coupling between each matching circuit. Figure 4 illustrates a photograph of GaN-on-Si MMIC DA with a chip size of 3.5 mm × 1.1 mm.

Small and large-signal measurements of the enhanced

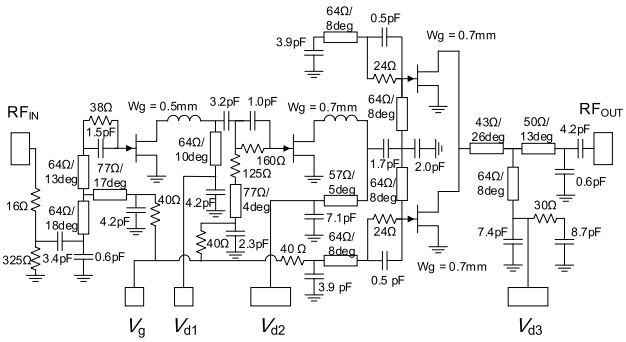

Fig. 3 Schematic of the GaN-on-Si MMIC DA

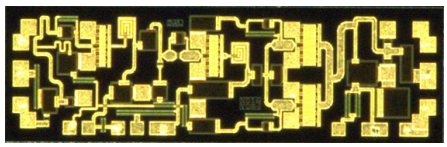

Fig. 4 Photograph of the GaN-on-Si MMIC DA

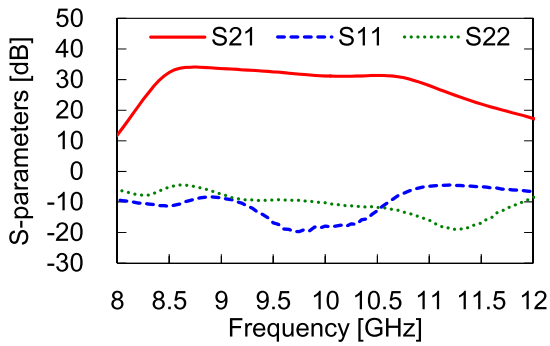

Fig. 5 Measured S-parameters of the developed GaN-on-Si MMIC DA

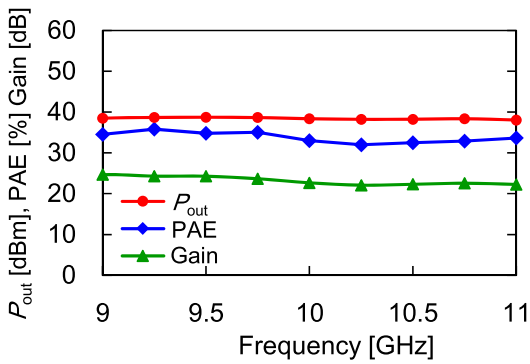

Fig. 6 Measured output power, PAE, and gain of the improved GaN-on-Si MMIC DA.

GaN-on-Si MMIC DA are performed with a drain voltage of 32 V and a quiescent drain current density of 50 mA/mm. Figure 5 illustrates measured S-parameters of the developed GaN-on-Si MMIC DA. A linear gain greater than 28 dB is obtained for frequencies conditions of between 8.5–11.0 GHz. Figure 6 illustrates the improved DA's measured output power, PAE, and gain as a function of frequency. The

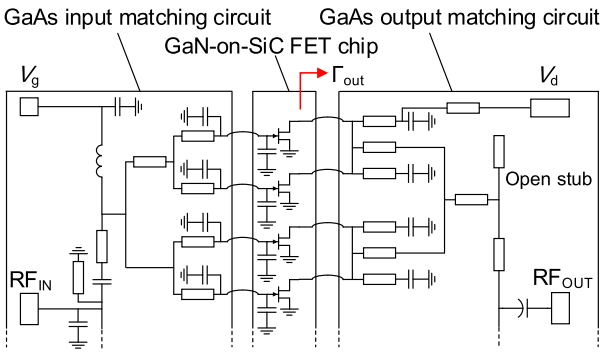

Fig. 7 Schematic of GaN-on-SiC HPA with GaAs matching circuits. Half of the circuit is shown, and the other half is symmetric.

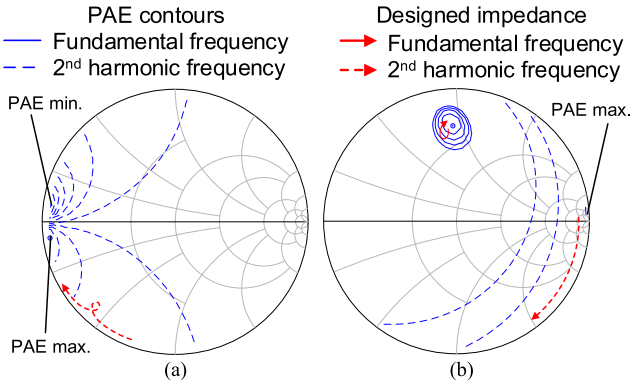

Fig. 8 Simulated targeted and designed impedances of the matching circuits. (a) Impedance of the input matching circuit. (b) Impedance of the output matching circuit.

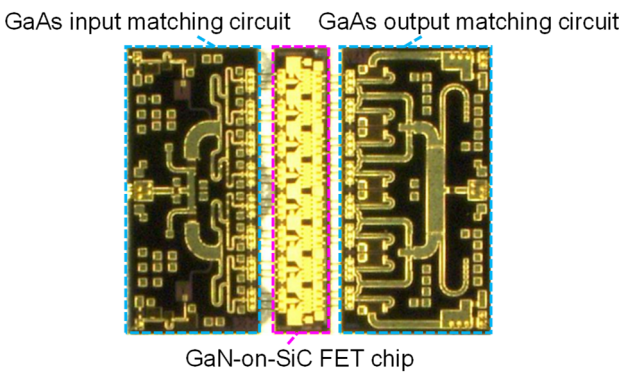

Fig. 9 Photograph of GaN-on-SiC HPA with GaAs matching circuits.

measurement is performed under pulsed operation with a pulse duty-cycle of 10%, and a saturated output power of 38.1–38.7 dBm, associate gain of 22.3–24.6 dB, and PAE of 32–36% over 9.0–11.0 GHz are obtained. The GaN-on-Si MMIC DA achieves high power and high gain with an extremely compact size that is less than half the size of typical GaAs MMIC HPA with similar output power [21].

2.3 GaN-on-SiC HPA with GaAs Input and Output Matching Circuits

GaN-on-SiC HPA with GaAs input and output matching circuits are designed and fabricated utilizing the 0.25 μm GaN-on-SiC MMIC and GaAs passive MMIC process. A schematic of the GaN-on-SiC HPA with GaAs matching circuits is illustrated in Fig. 7. GaAs input and output matching circuits and a GaN-on-SiC FET chip are connected via bonding wires. With HPAs being one of the most power-consuming components in T/R modules, design of the output matching circuit is important to realize high efficiency utilizing harmonic impedance tuning technique [22]–[28]. Impedance matching at the fundamental frequency is mainly based on a quarter-wavelength transmission line and a shunt inductance. In addition, open stubs with an electrical length of $\lambda/4$ at the second harmonic are used to obtain PAE matching at the second harmonic frequency. Figure 8 illustrates the simulated target impedance and impedance of matching circuits seen from the FETs for the fundamental (solid lines) and the second harmonic (dotted lines) frequency. Figure 8 (a) illustrates the source-pull contour and the designed impedance of the input matching circuit seen from the FETs for the second harmonic. The impedance for the maximum PAE and the impedance for the minimum PAE are almost equal. Therefore, the designed impedance is slightly mismatched from the maximum PAE impedance so that the impedance is far from the minimum PAE impedance. Figure 8 (b) illustrates impedances of the output matching circuit seen from the FETs. PAE contours are plotted by 2 pt. step. Designed impedance of the output matching circuit seen from the FETs for the fundamental (9–11 GHz) and the second harmonic (18–22 GHz) frequencies are shown, and the direction of the arrows indicate the low frequency to the high frequency. The HPA behaves like inverse class-F amplifier since only the second harmonic impedance is designed to realize open impedance. It is shown that the fundamental and the second harmonic impedances are well matched to the target impedances. On the input side, impedance matching at the fundamental frequency is achieved by one band-pass and one low-pass configuration. Pre-match small shunt capacitors are incorporated into the GaN-on-SiC FET chip to tune the second harmonic impedance. Figure 9 shows a photograph of the developed GaN-on-SiC HPA. The input matching circuit chip sizes, the FET chip, and the output matching circuit are 1.8 mm × 3.8 mm, 0.8 mm × 3.8 mm and 2.0 mm × 3.8 mm, respectively.

Small and large-signal measurements of the developed GaN-on-SiC HPA are performed with a drain voltage of 30 V and the quiescent drain current density of 50 mA/mm. Figure 10 illustrates the measured S-parameters of the developed GaN-on-SiC HPA. The linear gain of 8.1–11.5 dB is obtained at frequencies of over 9.0–11.0 GHz. The large-signal measurement is performed under the pulsed condition with a pulse duty-cycle of 10%. Figure 11 illustrates the measured output power, PAE, and gain of the developed GaN-on-SiC HPA as a function of frequency. The drain voltage is 30 V and the quiescent drain current density is

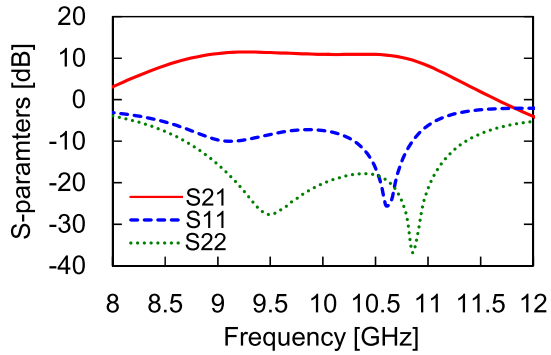

Fig. 10 Measured S-parameters of GaN-on-SiC HPA

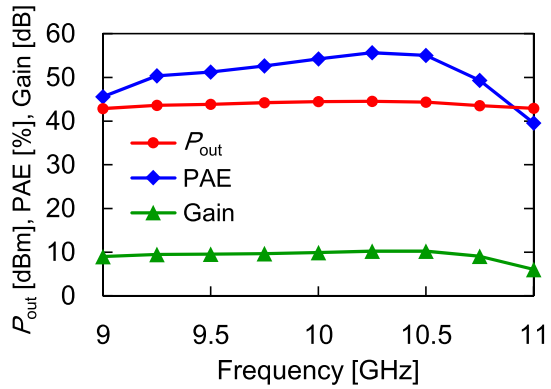

Fig. 11 Measured output power, PAE and gain of the developed GaN-on-SiC HPA

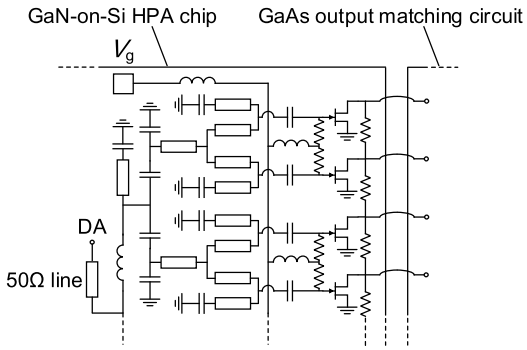

Fig. 12 Schematic of the input matching circuit of GaN-on-Si HPA. Half of the circuit is shown, and the other half is symmetric.

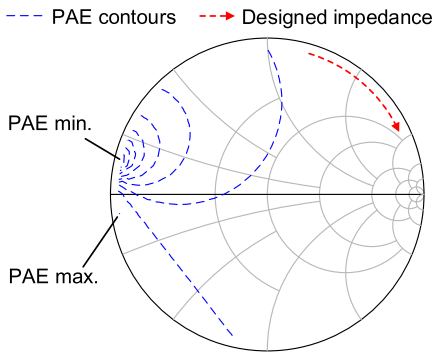

Fig. 13 Simulated target and designed second harmonic impedances of the input matching circuits of the GaN-on-Si HPA.

50 mA/mm. A saturated output power of 42.0–44.5 dBm, associate gain of 7.8–10.7 dB, and PAE of 40–56% for 9.0–11.0 GHz is obtained. These measured results show that the lower cost amplifier exhibits comparable characteristics with all reported advanced amplifiers.

By combining GaN-on-Si MMIC DA and GaN-on-SiC HPA, an output power in excess of 20 W, gain of higher than 30.8 dB, and PAE greater than 37% is estimated for frequencies of over 9.0–11.0 GHz.

2.4 GaN-on-Si HPA with GaAs Output Matching Circuits

The circuit design and measurements of a high-gain GaN-on-Si HPA are shown. A GaAs matching circuit is employed as the output matching circuit of the final stage amplifier to realize lower losses. As illustrated in Fig. 2 (b), the high gain four-stage GaN-on-Si HPA amplifier is composed of the GaN-on-Si amplifier chip and GaAs output matching circuit, which are connected via bonding wires. The aforementioned three-stage GaN-on-Si MMIC DA, an input matching circuit as well as FETs for the final-stage are incorporated into the GaN-on-Si chip. The final stage-gate periphery of the FETs is 1 mm × 8 cells. The DA is placed vertically with respect to the final-stage amplifier to reduce the chip size and connected with HPA via a 50 Ω transmission line. The output matching circuit is the same as the GaN-on-SiC HPA described in Sect. 2.3 as the target impedances are quite similar. Although the cost to area ratio of the GaAs and GaN-on-Si is comparable, GaAs exhibits lower dielectric losses, which enables high power and high-efficiency HPA. Figure 12 illustrates a schematic of the input matching circuit of the final-stage GaN-on-Si HPA, which is newly designed for the HPA. Two high-pass and one low-pass section are utilized. Figure 13 illustrates simulated target and designed second harmonic impedances of the input matching circuits of the GaN-on-Si HPA seen from the final-stage FETs. PAE contours of the second harmonic frequency for 10 GHz are plotted by 2 pt. step. The designed impedance for the second harmonic (18–22 GHz) frequencies are also shown and the direction of the arrows indicates the low frequency to the high frequency. The impedance for the maximum PAE and the impedance for the minimum PAE are close each other. Therefore, the designed impedance is mismatched from the maximum PAE impedance so that the impedance is far from the minimum PAE impedance as in case of the GaN-on-SiC HPA. Figure 14 illustrates a photograph of the GaN-on-Si HPA with a GaAs output matching circuit. The total chip size of the GaN-on-Si chip and the GaAs chip are 3.5 mm × 3.8 mm and 2.0 mm × 3.8 mm, respectively.

Small and large-signal measurements are performed, with a drain voltage is 32 V and the quiescent drain current density of 50 mA/mm being recorded. Figure 15 illustrates the measured S-parameters of the developed GaN-on-Si MMIC HPA. A linear gain of 38.7–41.2 dB is obtained

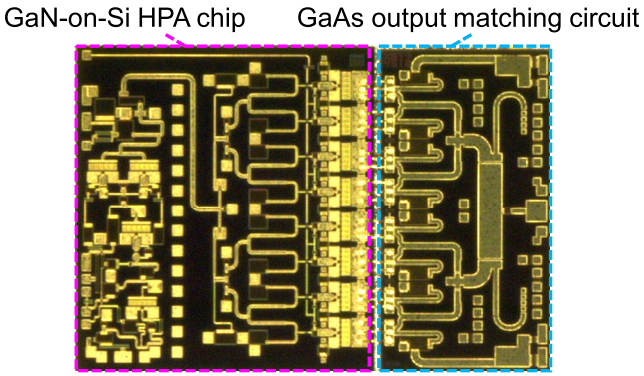

Fig. 14 Photograph of the developed GaN-on-Si HPA

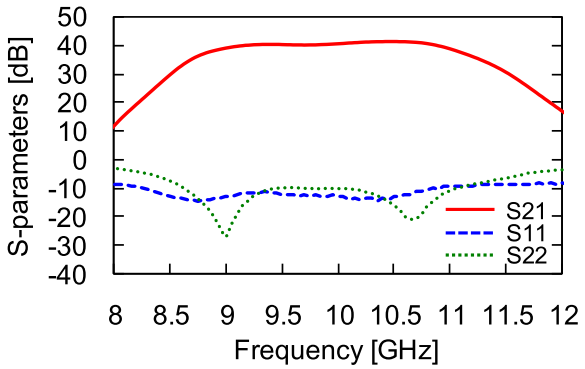

Fig. 15 Measured S-parameters of the GaN-on-Si HPA

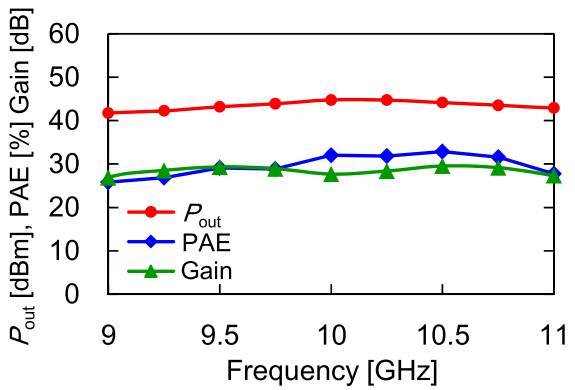

Fig. 16 Measured output power, PAE and gain of the GaN-on-Si HPA.

over frequencies of 9.0–11.0 GHz. Figure 16 illustrates measured output power, gain, and PAE for the improved GaN-on-Si HPA as a function of frequency. The large-signal measurement is operated under a pulse duty-cycle of 10%. And reports a saturated output power in the 41.8–44.8 dBm range, associated gain of 26.9–29.5 dB and PAE of 26–33% for frequencies of 9.0–11.0 GHz. While the efficiency is not as high as that of GaN-on-SiC HPA, these configurations indicate compact and high output power and gain characteristics. The effect of the machining accuracy on the performances is comparable for the two configurations because the deviation of bonding wire length connected to the output matching circuit is dominant on the performance. The configuration of amplifier stage is in a trade-off between the efficiency and the cost.

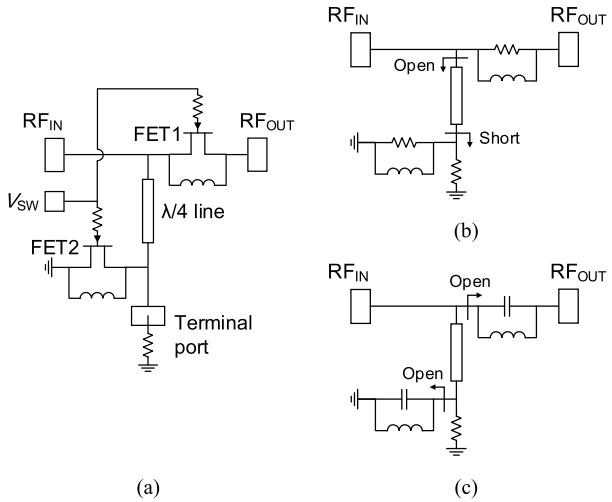

Fig. 17 Schematic of GaN-on-Si MMIC SW. (a) Equivalent circuit of developed GaN-on-Si MMIC SW. (b) Simplified equivalent circuit of SW in receive-mode. (c) Simplified equivalent circuit of SW in transmit-mode.

2.5 GaN-on-Si MMIC High Power SW

A cost-effective GaN-on-Si MMIC SW is designed to protect the receiving devices such as low noise amplifier (LNA) from transmission or reception of unwanted large signals. Figure 17 illustrates schematics of the developed GaN-on-Si MMIC SW. Figure 17 (a) illustrates the equivalent circuit of the developed GaN-on-Si MMIC SW. The SW has an input port and a terminal port which is terminated to 50 Ω. The SW has two FETs, namely FET1 and FET2. FET1 is connected in series between the input and the output ports. A transmission line with the length of $\lambda/4$ at the center frequency followed by shunted FET2 is placed between the input and the terminal ports. A spiral inductor is connected in parallel with each FET. Gate electrodes of the FETs are connected to a common DC voltage supply with high resistance. The operation modes of the SW are controlled by a DC voltage applied to the gates of the FETs, wherein the FET shows off-capacitance when biased at −40 V and on-resistance when biased 0 V. The FETs are biased at 0 V in receive-mode and −40 V in transmit-mode, respectively. Figure 17 (b) and (c) illustrate equivalent circuits of the SW in receive-mode and transmit-mode, respectively. In receive-mode, FETs are biased at 0 V so that they behave as low on-resistance. The equivalent circuit of the receive-mode is illustrated in Fig. 17 (b). FET1 exhibits limited losses and the impedance of the shunt-connected $\lambda/4$ and FET2 exhibits open impedance looking from the input port at the center frequency. Therefore, it has low loss characteristic from the input to the output port. In transmit-mode, isolation between input and output ports must be high to protect receiving devices from high power transmit signal

or noise. FETs are biased at −40 V so that they behave as off-capacitance. The equivalent circuit of the transmit-mode is illustrated in Fig. 17 (c). Each FET and inductance behave like an open circuit, with external signals from input port going to the terminal port. Then, it demonstrates high isolation characteristics between the input and output ports. Design of gate-width of the FETs is explained. Parallel inductors are neglected for simplification. F-matrix between the RF input and output port of the receive-mode is calculated to be

$$F_{\mathrm{RX}} = \begin{pmatrix} 1 & 0 \\ \frac{1}{Z}\frac{Z + jZ_{\mathrm{L}}\tan\theta}{Z_{\mathrm{L}} + jZ\tan\theta} & 1 \end{pmatrix} \begin{pmatrix} 1 & R_{\mathrm{on1}} \\ 0 & 1 \end{pmatrix}, \quad Z_L = Z_0 // R_{\mathrm{on2}} \tag{1}$$

where Z_0 is the port impedance, Z and θ are the characteristic impedance and the electrical length of the $\lambda/4$ line, R_{on1} and R_{on2} are the on-resistance of FET1 and FET2, respectively. By assuming that $\theta = 90$ deg., $R_{\mathrm{on}} \cong R_{\mathrm{on1}}, R_{\mathrm{on2}}$, $Z_{\mathrm{L}} \cong R_{\mathrm{on}}$, $Z \cong Z_0$ and $(R_{\mathrm{on}}/Z_0)^2 \cong 0$, Eq. (1) is transformed to

$$F_{\mathrm{RX}} \cong \begin{pmatrix} 1 & R_{on} \\ R_{on}/Z_0^2 & 1 \end{pmatrix}. \tag{2}$$

Then the insertion loss in receive-mode ($\mathrm{IL_{RX}}$) is derived by calculating $|\mathrm{S_{21}}|$ using Eq. (2) as

$$\mathrm{IL_{RX}} \cong \frac{1}{1 + R_{on}/Z_0} = \frac{1}{1 + R_{on0}/W_g Z_0} \tag{3}$$

where R_{on0} (Ωmm) is the on-resistance of the 1 mm-gate-width FET and W_{g} (mm) is the gate width of the FET. Similarly, F-matrix between the RF input and output port of the transmit-mode is calculated to be

$$F_{\mathrm{TX}} = \begin{pmatrix} 1 & 0 \\ \frac{1}{Z}\frac{Z + jZ_{\mathrm{L}}tan\theta}{Z_{\mathrm{L}} + jZtan\theta} & 1 \end{pmatrix} \begin{pmatrix} 1 & 1/j\omega C_{\mathrm{off1}} \\ 0 & 1 \end{pmatrix}, \quad Z_L = Z_0 // j\omega C_{\mathrm{off2}} \tag{4}$$

where C_{off1} is the off-capacitance of the FET1. By assuming that $Z_{\mathrm{L}} \cong Z \cong Z_0$, Eq. (4) is transformed to

$$F_{\mathrm{TX}} \cong \begin{pmatrix} 1 & 1/j\omega C_{\mathrm{off1}} \\ 1/Z_0 & 1 + 1/j\omega C_{\mathrm{off1}} Z_0 \end{pmatrix}. \tag{5}$$

Then the isolation in transmit-mode ($\mathrm{ISO_{TX}}$) is derived by calculating $|\mathrm{S_{21}}|$ using Eq. (5) as

$$\mathrm{ISO_{TX}} \cong \frac{1}{\sqrt{2.25 + (1/\omega C_{\mathrm{off1}} Z_0)^2}} = \frac{1}{\sqrt{2.25 + (1/\omega C_{\mathrm{off0}} W_{\mathrm{g}} Z_0)^2}} \tag{6}$$

where C_{off0} (F/mm) is the off-capacitance of the 1 mm-gate-width FET. Insertion loss and isolation are in a trade-off relation according to W_{g}. Figure 18 shows the dependence of insertion loss and isolation on the gate width of FET according to Eq. (3) and Eq. (6) ($Z_0 = 50\ \Omega$, $R_{\mathrm{on0}} = 3.7\ \Omega$mm, $C_{\mathrm{off0}} = 0.186$ pF/mm and $f = 10$ GHz). Large W_{g} of 1 mm is employed for loss reduction and the value of the inductors is set so that the resonation frequency of C_{off} and the inductance is equal to the center frequency to improve isolation.

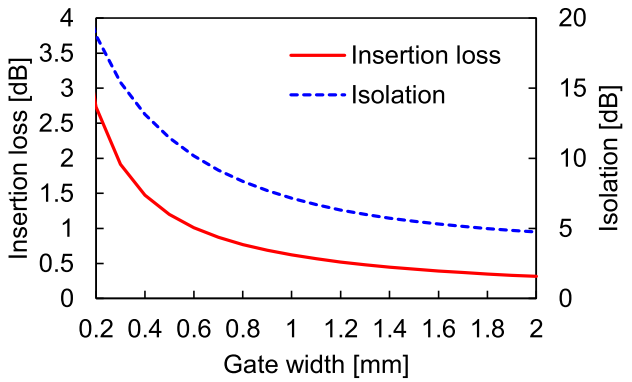

Fig. 18 Dependence of insertion loss and isolation on the total gate width.

Fig. 19 Photograph of the developed GaN-on-Si MMIC SW

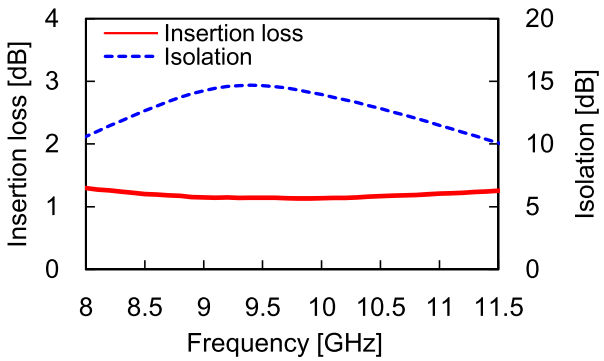

Fig. 20 Measured small-signal characteristics of the developed GaN-on-Si MMIC SW

A photograph of the GaN-on-Si MMIC SW, with a chip size of 1.05 mm × 1.95 mm is illustrated in Fig. 19. Transmission lines between the input port and the output port are designed to be as short as possible to reduce losses. Figure 20 shows a measurement insertion loss and isolation of the developed GaN-on-Si MMIC SW. Insertion losses of 1.1–1.3 dB and isolation of 10.1–14.7 dB are obtained at frequencies of 8.0–11.5 GHz. The measured loss is larger than the calculated loss due to the loss of transmission lines is neglected in the calculation. The measured isolation is larger

Table 1 Comparisons of size and estimated relative cost with other published power amplifiers and a switch for X-band modules.

		DA		HPA		SW		*Normalized cost
		Substrate	Size (mm^2)	Substrate	Size (mm^2)	Substrate	Size (mm^2)	(a.u)
This work	Case 1	GaN-on-Si	3.9	GaN-on-SiC / GaAs	3.0 / 14.4	GaN-on-Si	2	26.3
	Case 2	-	-	GaN-on-Si / GaAs	13.3 / 7.6	GaN-on-Si	2	22.9
Case 3		GaAs [21]	8.8	GaN-on-SiC [4]	18	GaN-on-SiC [11]	1.9	48.6

(*) Assuming cost ratio of GaN-on-Si:GaAs:GaN-on-SiC = 1:1:2

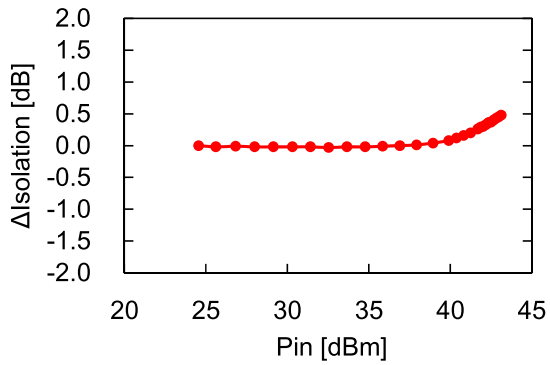

Fig. 21 Measured large-signal characteristic of GaN-on-Si MMIC SW at 9.5 GHz.

than the calculated isolation since the parallel inductor is neglected in the calculation. Figure 21 illustrates the measured large-signal characteristic of GaN-on-Si MMIC SW at 9.5 GHz. Deviation of isolation is less than 0.5 dB, and up to 43.1 dBm input power.

3. Evaluation of Cost-Effectiveness

The cost-efficiency of the developed chipsets is evaluated. Table 1 summarizes comparisons of size and the estimated relative cost with other published power amplifiers and switches for X-band transmit modules. In case-1, the developed GaN-on-Si MMIC DA, the GaN-on-SiC HPA with the GaAs output matching circuit, and the GaN-on-Si MMIC SW are utilized. In case-2, the developed GaN-on-Si high-gain HPA and the GaN-on-Si MMIC SW are utilized. In case-3, conventional transmit modules composed of the GaAs DA [21], the GaN-on-SiC HPA [4] and the GaN-on-SiC SW [11] ever-reported. The cost ratio of GaAs:GaN-on-SiC is typically said to be 1:2 [29], [30]. 50% cost reduction of GaN device fabrication is achieved by using larger wafer [29]. Because large Si wafer is commonly available, cost of GaN-on-Si can be half the cost of GaN-on-SiC. The normalized cost is calculated using a chip size and assumed cost ratio of GaN-on-Si:GaAs:GaN-on-SiC = 1:1:2. By employing the chipset shown in case-1, 46% cost reduction from case-3 is estimated. The cost of case-2 is estimated to be less than half as expensive as case-3. As the output power is comparable between case-1 and case-2, only the efficiency is a trade-off factor with the cost. If power consumption of system specification was not as tight, for example, the system only required short pulse mode operation, case-2 can be the best candidate for the transmit module.

4. Conclusion

GaN chipsets for cost-effective X-band 20 W transmit modules are fabricated and measured. The chipsets include four devices, a GaN-on-Si MMIC DA, a GaN-on-SiC MMIC HPA with a GaAs MMIC input and output matching circuits, a high-gain GaN-on-Si HPA with a GaAs output matching circuit and a GaN-on-Si high power SW. The developed chipsets are estimated to be about half the cost of a conventional chipset while maintaining performances.

References

[1] G.W. Stimson, "Introduction to Airborne Radar," 2nd ed., Mendham, NJ, USA: SciTech, pp.473–491, 1998.

[2] S. Shinjo, K. Nakatani, J. Kamioka, R. Komaru, H. Noto, H. Nakamizo, S. Yamaguchi, S. Uchida, A. Okazaki, and K. Yamanaka, "A 28GHz-band highly integrated GaAs RF frontend Module for Massive MIMO in 5G," 2018 IEEE MTT-S International Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G), Dublin, pp.1–3, 2018. doi: 10.1109/IMWS-5G.2018.8484564

[3] J.S. Herd and M.D. Conway, "The Evolution to Modern Phased Array Architectures," Proceedings of the IEEE, vol.104, no.3, pp.519–529, March 2016. doi: 10.1109/JPROC.2015.2494879

[4] S. Piotrowicz, Z. Ouarch, E. Chartier, R. Aubry, G. Callet, D. Floriot, J. Jacquet, O. Jardel, E. Morvan, T. Reveyrand, N. Sarazin, and S. Delage "43W, 52% PAE X-Band AlGaN/GaN HEMTs MMIC amplifiers," 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, pp.505–508, 2010. doi: 10.1109/MWSYM.2010.5518097

[5] T. Torii, S. Imai, H. Maehara, M. Miyashita, T. Kunii, T. Morimoto, A. Inoue, A. Ohta, H. Katayama, N. Yunoue, K. Yamanaka, and H. Fukumoto, "60% PAE, 30W X-band and 33% PAE, 100W Ku-band PAs utilizing 0.15 μm GaN HEMT technology," 2016 46th European Microwave Conference (EuMC), London, pp.568–571, 2016. doi: 10.1109/EuMC.2016.7824406

[6] D. Sardin, T. Reveyrand, and Z. Popović, "X-band 10W MMIC high-gain power amplifier with up to 60% PAE," 2014 44th European Microwave Conference, Rome, pp.1337–1340, 2014. doi: 10.1109/EuMC.2014.6986691

[7] J. Kang and J.-S. Moon, "Highly efficient wideband X-band MMIC class-F power amplifier with cascode FP GaN HEMT," Electronics Letters, vol.53, no.17, pp.1207–1209, 2017. doi: 10.1049/el.2017.1672

[8] H.-Q. Tao, W. Hong, B. Zhang, and X.-M. Yu, "A Compact 60 W X-Band GaN HEMT Power Amplifier MMIC," IEEE Microwave and Wireless Components Letters, vol.27, no.1, pp.73–75, Jan. 2017. doi: 10.1109/LMWC.2016.2630926

[9] J. Kamioka, E. Kuwata, M. Hangai, K. Nakahara, Y. Kamo, S. Shinjo, M. Shimozawa, "A 26-W X-Band High Efficiency GaN MMIC Power Amplifier with Compact Spurious Suppression Filters," 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, pp.1211–1213, 2018. doi: 10.23919/APMC.2018.8617185

[10] N. Ono, T. Senju, and K. Takagi, "53% PAE 32 W Miniaturized X-Band GaN HEMT Power Amplifier MMICs," 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, pp.557–559, 2018. doi: 10.23919/APMC.2018.8617446
[11] C.F. Campbell and D.C. Dumka, "Wideband high power GaN on SiC SPDT switch MMICs," 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, pp.145–148, 2010. doi: 10.1109/MWSYM.2010.5517940
[12] M. Hangai, R. Komaru, K. Nakahara, Y. Kamo, M. Hieda, and K. Yamanaka, "A high power and low loss GaN HEMT MMIC T/R switch utilizing band-pass/low-pass configuration," 2014 44th European Microwave Conference, Rome, pp.1122–1125, 2014. doi: 10.1109/EuMC.2014.6986637
[13] J. Kamioka, Y. Kawamura, Y. Tarui, K. Nakahara, Y. Kamo, H. Okazaki, M. Hangai, K. Yamanaka, and H. Fukumoto, "A Low-Cost 30-W Class X-Band GaN-on-Si MMIC Power Amplifier with a GaAs MMIC Output Matching Circuit," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, pp.93–96, 2018. doi: 10.23919/EuMIC.2018.8539903
[14] P. Schuh, H. Sledxik, R. Reber, A. Fleckenstein, R. Leberer, M. Oppermann, R. Quay, F. van Raay, M. Seelmann-Eggebert, R. Kiefer, and M. Mikulla, "GaN MMIC based T/R-Module Front-End for X-Band Applications," 2008 European Microwave Integrated Circuit Conference, Amsterdam, pp.274–277, 2008. doi: 10.1109/EMICC.2008.4772282
[15] A. Bettidi, D. Carosi, A. Cetronio, F. Corsaro, C. Costrini, C. Lanzieri, and L. Marescialli, "X-band transmit/receive module MMIC chip-set based on emerging GaN and SiGe technologies," IEEE Int. Symp. On phased array systems and technology Dig. Waltham, MA, US, pp.250–255, Oct. 2010.
[16] J.P.B. Janssen, M. van Heijningen, G. Provenzano, G.C. Visser, E. Morvan, and F.E. van Vliet, "X-Band Robust AlGaN/GaN Receiver MMICs with over 41 dBm Power Handling," 2008 IEEE Compound Semiconductor Integrated Circuits Symposium, Monterey, CA, pp.1–4, 2008. doi: 10.1109/CSICS.2008.23
[17] S. Masuda, M. Yamada, T. Ohki, K. Makiyama, N. Okamoto, Y. Nakasha, K. Imanishi, T. Kikkawa, and H. Shigematsu, "C-Ku band GaN MMIC T/R frontend module using multilayer ceramics technology," 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, pp.1–4, 2011. doi: 10.1109/MWSYM.2011.5972761
[18] A. Bettidi, A. Cetronio, M. Cicolani, C. Costrini, C. Lanzieri, S. Maccaroni, L. Marescialli, M. Peroni, and P. Romanini, "X-band T/R module in state-of-the-art GaN technology," 2009 European Radar Conference (EuRAD), Rome, pp.258–261, 2009.
[19] S. Masuda, M. Yamada, Y. Kamada, T. Ohki, K. Makiyama, N. Okamoto, K. Imanishi, T. Kikkawa, and H. Shigematsu, "GaN single-chip transceiver frontend MMIC for X-band applications," 2012 IEEE/MTT-S International Microwave Symposium Digest, Montreal, QC, pp.1–3, 2012. doi: 10.1109/MWSYM.2012.6259470
[20] S. D'Angelo, A. Biondi, F. Scappaviva, D. Resca, and V.A. Monaco, "A GaN MMIC chipset suitable for integration in future X-band spaceborne radar T/R module Frontends," 2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON), Krakow, pp.1–4, 2016. doi: 10.1109/MIKON.2016.7492014
[21] G. Nikandish and A. Medi, "A Design Procedure for High-Efficiency and Compact-Size 5–10-W MMIC Power Amplifiers in GaAs pHEMT Technology," IEEE Transactions on Microwave Theory and Techniques, vol.61, no.8, pp.2922–2933, Aug. 2013. doi: 10.1109/TMTT.2013.2271997
[22] F.H. Raab, "Class-F power amplifiers with maximally flat waveforms," IEEE Transactions on Microwave Theory and Techniques, vol.45, no.11, pp.2007–2012, Nov. 1997. doi: 10.1109/22.644215
[23] R.A. Beltran, "Class-F and inverse class-F power amplifier loading networks design based upon transmission zeros," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), Tampa, FL, pp.1–4, 2014. doi: 10.1109/MWSYM.2014.6848269
[24] S. Gao, P. Butterworth, S. Ooi, and A. Sambell, "High-efficiency power amplifier design including input harmonic termination," IEEE Microwave and Wireless Components Letters, vol.16, no.2, pp.81–83, Feb. 2006. doi: 10.1109/LMWC.2005.863171
[25] K. Kuroda, R. Ishikawa, and K. Honjo, "Parasitic Compensation Design Technique for a C-Band GaN HEMT Class-F Amplifier," IEEE Transactions on Microwave Theory and Techniques, vol.58, no.11, pp.2741–2750, Nov. 2010. doi: 10.1109/TMTT.2010.2077951
[26] M. Kamiyama, R. Ishikawa, and K. Honjo, "5.65 GHz High-Efficiency GaN HEMT Power Amplifier With Harmonics Treatment up to Fourth Order," IEEE Microwave and Wireless Components Letters, vol.22, no.6, pp.315–317, June 2012. doi: 10.1109/LMWC.2012.2197385
[27] S. Tanaka, S. Koizumi, R. Ishikawa, and K. Honjo, "Class-F GaN HEMT Amplifiers Using Compact CRLH Harmonic Tuning Stubs Designed Based on Negative Order Resonance Modes," IEICE Trans. Electron., vol.E102-C, no.10, pp.691–698, Oct. 2019. doi: 10.1587/transele.2019MMP0001
[28] T. Sugiura, S. Furuta, T. Murakami, K. Tanji, N. Otani, and T. Yoshimasu, "High Efficiency Class-E and Compact Doherty Power Amplifiers with Novel Harmonics Termination for Handset Application," IEICE Trans. Electron., vol.E102-C, no.10, pp.699–706, Oct. 2019.
[29] W. DeMore, Gauging the state of GaN power amplification, http://www.analog.com/media/en/technical-documentation/technical-articles/Gauging-the-State-of-GaN-Power-Amplification.pdf (accessed 2020-03-23)
[30] R.L. Haupt, "Timed arrays: wideband and time varying antenna arrays," New York: Wiley, pp.96–98, 2015.

Jun Kamioka received the B.E. and M.E. degrees in physical electronics engineering from Tokyo Institute of Technology in 2012 and 2014, respectively. In 2014, he joined Information Technology Research and Development Center, Mitsubishi Electric Corporation, where he has been engaged in research and development of microwave amplifiers. He is a member of the Institute of Electronics, Information and Communications on Engeneers (IEICE), Japan.

Yoshifumi Kawamura received the B.E., M.E., and Ph.D. degrees in electronics and information engineering from Hokkaido University in 2008, 2010 and 2013, respectively. In 2013, he joined Information Technology Research and Development Center, Mitsubishi Electric Corporation, where he has been engaged in research and development of microwave power amplifiers. He is a member of the Institute of Electronics, Information and Communications on Engeneers (IEICE), Japan.

Ryota Komaru received the B.E. and M.E. degrees in computer science from Kyushu Institute of Technology in 2005 and 2007, respectively. In 2007, he joined Information Technology Research and Development Center, Mitsubishi Electric Corporation, where he has been engaged in research and development of microwave circuits. He is a member of the Institute of Electronics, Information and Communications on Engeneers (IEICE), Japan.

Masatake Hangai received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tohoku University, Sendai, Japan, in 2000, 2002, and 2012, respectively. In 2002, he joined the Information Technology R&D Center, Mitsubishi Electric Corporation, Kamakura, Japan, where he has been engaged in research and development of microwave control circuits, microwave amplifiers, MMICs, modems, and active phased array antenna systems for satellite applications. He was the recipient of the 2011 IEEE MTT-S Japan Young Engineer Award, and the 2011 Michiyuki Uenohara Memorial Award. Dr. Hangai is a senior member of the Institute of Electronics, Information and Communications on Engeneers (IEICE), Japan.

Yoshitaka Kamo received the B.E. and M.E. degrees in applied physics from Osaka City University in 1995 and 1997, respectively. In 1997, he joined High Frequency & Optical Device Works, Mitsubishi Electric Corporation, where he has been engaged in development of compound semiconductor transistors.

Tetsuo Kodera received the B.S., M.S., and D.S. degrees in physics from the University of Tokyo in 2002, 2004, and 2007, respectively. He worked as a Research Associate at the University of Tokyo, and an Assistant Professor at Tokyo Institute of Technology. He is an Associate Professor at Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, where he has been engaged in research of quantum information devices.

Shintaro Shinjo received the B.S. and M.S. degrees in physics and Ph.D. degree in engineering from Keio University, Tokyo, Japan, in 1996, 1998, and 2011, respectively. In 1998, he joined Mitsubishi Electric Corporation, Kamakura, Japan, where he has been involved in the research and development of microwave monolithic integrated circuits and solid-state power amplifiers. From 2011 to 2012, he was a visiting scholar with the University of California at San Diego, San Diego, CA, USA. He is a senior member of Electrical and Electronics Engineers (IEEE). He was a recipient of the Prize for Science and Technology (Development Category) of the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2009 and the IEICE Electronics Society Award in 2011.