# BRIEF PAPER Special Section on Recent Advances in Simulation Techniques and Their Applications for Electronics

# **Evaluation and Extraction of Equivalent Circuit Parameters for GSG-Type Bonding Wires Using Electromagnetic Simulator**

Takuichi HIRANO<sup>†a)</sup>, Senior Member

SUMMARY In this paper, the author performed an electromagnetic field simulation of a typical bonding wire structure that connects a chip and a package, and evaluated the signal transmission characteristics (Sparameters). In addition, the inductance per unit length was extracted by comparing with the equivalent circuit of the distributed constant line. It turns out that the distributed constant line model is not sufficient because there are frequencies where chip-package resonance occurs. Below the resonance frequency, the conventional low-frequency approximation model was effective, and it was found that the inductance was about 1 nH/mm. key words: bonding wires, extraction, inductance, capacitance, electromagnetic field simulation

#### 1. Introduction

A bonding wire is used to connect the semiconductor chip and the package (or substrate). The bonding wire is crimped by heating a gold wire to the pad on the chip and the package [1], [2]. Semiconductor chips connect power supplies through bonding wires and send and receive signals to and from the outside. When a signal is transmitted through a bonding wire, it becomes a lumped constant line at low frequencies, but at high frequencies, its characteristics cannot be evaluated unless it is analyzed as a distributed constant line and a more rigorous electromagnetic (EM) field problem. Traditionally, the effects of bonding wires have been evaluated using wire inductance per unit length using low frequency approximation [3]-[17]. There are also many documents [18], [19] that investigated the effect of bonding wires using electromagnetic field simulation, but it is different from the connection considering the height of the chip examined in this paper.

In this paper, the author performed an electromagnetic field simulation of a typical bonding wire structure that connects a chip and a package, and evaluated the signal transmission characteristics (S-parameters). In addition, the inductance per unit length was extracted by comparing with the equivalent circuit of the distributed constant line. It turns out that the distributed constant line model is not sufficient because there are frequencies where chip-board resonance occurs. The miniaturization of semiconductors has made it possible to handle millimeter-wave bands [20]-[23], which has become a very important issue in chip-package transmission.

Manuscript received November 1, 2021.

<sup>†</sup>The author is with Tokyo City University, Tokyo, 158–8557 Japan.

a) E-mail: thirano@tcu.ac.jp

DOI: 10.1587/transele.2021ESS0002

#### Analysis Model 2.

Figure 1 shows a model of the bonding wire that connects the chip and the package. The circuit layer of the chip is filled with SiO<sub>2</sub> having a relative permittivity of 4, the height is set to 5 µm. The pads on the chip have a Ground-Signal-Ground (GSG) structure with a thickness of 1 µm, 70 µm square, and 100 µm pitch. The ground pads on both sides of the signal pad are connected to the ground of the chip using vias. The pads on the package have a Ground-Signal-Ground (GSG) structure with a thickness of 18 µm, 200 µm square and 250 µm pitch. The ground pads on both sides of the signal pad are connected to the ground of the package using vias. The radius of the bonding wire is a, extending vertically by  $h_1$  from the pad on the chip, extending horizontally to  $d_1$ , and then connecting to the pad of the package by the shortest straight path.

Figure 2 shows an electromagnetic field simulation model. The electromagnetic field simulator based on the finite element method, COMSOL Multiphysics, was used. The lower surface, which is the ground of the package, was an electric wall (PEC), and the other five peripheral surfaces were an absorbing boundary condition (ABC). Assuming silicon, the chip has a relative permittivity of 11.9, and the package has a relative permittivity of 3.4. The chip and package were lossless. The bonding wire and pad were assumed to be copper and had a conductivity of  $\sigma = 5.8 \times 10^7$  S/m. Lumped ports with a reference





Manuscript publicized May 17, 2022.





impedance of  $50 \Omega$  were set for Ports 1 and Port 2.

### 3. RLGC Parameter Extraction

Calculate the S-parameters or Z-parameters in Fig. 1 by electromagnetic field simulation analysis. The relationship between the Z-parameter and the impedance of the T-type equivalent circuit in Fig. 3 is given by the following equation.

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix}$$
(1)

From Eq. (1), the constant of the T-type circuit can be obtained from the Z-parameter by the following equation.

$$\begin{pmatrix} Z_1 = Z_{11} - Z_3 = Z_{11} - Z_{12} \\ Z_2 = Z_{22} - Z_3 = Z_{22} - Z_{12} \\ Z_3 = Z_{12} = Z_{21} \end{cases}$$
(2)

Figure 4 shows the RLGC parameters of a distributed constant line of length  $\Delta z$ . Comparing Fig. 4 and Fig. 3, the following equation is obtained.

$$\begin{cases} Z_1 + Z_2 = R\Delta z + j\omega L\Delta z \\ 1/Z_3 = G\Delta z + j\omega C\Delta z \end{cases}$$
(3)

From Eq. (3), RLGC can be calculated by the following equation.

$$\begin{cases}
R = \operatorname{Re} [Z_1 + Z_2] / \Delta z \\
L = \operatorname{Im} [Z_1 + Z_2] / (\omega \Delta z) \\
G = \operatorname{Re} [1/Z_3] / \Delta z \\
C = \operatorname{Im} [1/Z_3] / (\omega \Delta z)
\end{cases}$$
(4)



**Fig.4** RLGC parameters for distributed-constants transmission line model.



**Fig. 5** S-parameters ( $a = 10 \,\mu\text{m}$ ,  $s = 100 \,\mu\text{m}$ ,  $w_c = 1 \,\text{mm}$ ).



Fig. 6 Relative intensity of electric field.

## 4. Results

#### 4.1 S-Parameters

Figure 5 shows the frequency characteristics of the Sparameters when  $a = 10 \,\mu\text{m}$  and  $s = 100 \,\mu\text{m}$  in Fig. 1. The transmission coefficient is small up to around 15 GHz, but a resonance phenomenon is observed that sharply decreases around 22 GHz. The reflectance coefficient gradually increases to the vicinity of this resonance. Figure 6 shows the electric field distribution at 10 GHz and 22 GHz. At 22 GHz, resonance due to the substrate, bonding wire, and chip is observed, which is not seen at 10 GHz.

## 4.2 Extracted RLGC Parameters

The S-parameters in Fig. 5 are converted to Z-parameters, and the RLGC component per 1 mm extracted using Eq. (4) is shown in Fig. 7. The conductance G is a negative value because it cannot be expressed by the equivalent circuit. At low frequencies below 20 GHz, the inductance is close to 1 nH/mm. This is in good agreement with the commonly



Fig. 7 RLGC parameters ( $a = 10 \,\mu\text{m}$ ,  $s = 100 \,\mu\text{m}$ ,  $w_c = 1 \,\text{mm}$ ).

**Table 1** Inductance with wire radius *a*. ( $s = 100 \,\mu\text{m}$ ,  $w_c = 1 \,\text{mm}$ , 10 GHz)

<i>a</i> (µm)	Inductance (nH/mm)
5	1.13
10	0.91
20	0.67

used approximation 1.15 nH/mm by the following equation.

$$L = \frac{\mu_0}{\pi} \ln \frac{d}{a} \tag{5}$$

Equation (5) is the inductance per unit length of two parallel lines with radius *a* and spacing *d* ( $a \ll d$ ). However, at high frequencies above 20 GHz, there is a resonance phenomenon that cannot be explained by low frequency approximation. The capacitance per unit length of two parallel lines is 0.0097 pF/mm according to the following equation.

$$C = \frac{\pi \varepsilon_0}{\ln \frac{d}{a}} \tag{6}$$

Using these values, Z-parameters were calculated from Eqs. (1) and (2) and converted to S-parameters. Figure 8 shows the results of comparison with the electromagnetic field simulation values. The difference at low frequencies is not large, but resonance near 22 GHz cannot be obtained with the equivalent circuit model.

#### 4.3 Wire Radius Effects

Table 1 shows the difference in inductance value depending on the wire radius. It was found that the thicker the wire, the smaller the inductance, which is consistent with the tendency in Eq. (5).



**Fig. 8** Comparison between EM simulation and equivalent circuit model  $(a = 10 \,\mu\text{m}, s = 100 \,\mu\text{m}, w_c = 1 \,\text{mm}).$ 

**Table 2** Total lengths of bonding wires with spacing *s*. ( $a = 10 \,\mu\text{m}$ ,  $w_c = 1 \,\text{mm}$ )

	Length (µm)		
s (µm)	Signal-Signal	GND-GND	Average
50	393.7	421.5	407.6
100	428.2	454.8	441.5
200	508.3	531.4	519.9
400	688.9	706.1	697.5



**Fig.9** Variation of  $S_{21}$  with average bonding wire lengths in Table 2. ( $a = 10 \,\mu\text{m}, w_c = 1 \,\text{mm}$ )

#### 4.4 Wire Length Effects

The change in characteristics due to the length of the bonding wire was investigated. The distance *s* between the chip end in Fig. 1 and the pad end on the package was changed. Table 2 shows the length of the bonding wire with respect to *s*. Figure 9 shows the change in the transmission coefficient  $S_{21}$  due to the change in the bonding wire length. It can be seen that the resonance frequency decreases as the wire length increases. It was confirmed that the change in inductance was small in *s*.

#### 4.5 Chip Size Effects

Figure 10 shows the change in the transmission coefficient  $S_{21}$  depending on the chip width. It can be confirmed that the larger the chip, the lower the frequency of resonance.

#### 5. Conclusions

The wire bonding characteristics between the chip and the package were evaluated by electromagnetic field simulation. Resonance at a specific frequency, which cannot be obtained



**Fig. 10** Variation of  $S_{21}$  with chip width  $w_c$ .

with the equivalent circuit model, was confirmed. Since the frequency at which resonance occurs depends on the length of the bonding wire and the width of the chip, it was found that the resonance is caused by the leakage of electromagnetic waves to the lower part of the bonding wire and chip. Below the resonance frequency, the conventional lowfrequency approximation model was effective, and it was found that the inductance was about 1 nH/mm. In the future, it will be necessary to study a structure that does not cause resonance in the frequency band used.

#### Acknowledgments

The author acknowledges KESCO CO., LTD. for their support of COMSOL application builder compiler. This work was supported in part by NICT and Research Center for Biomedical Engineering (Hiroshima Univ.).

#### References

- O.L. Anderson, H. Christensen, and P. Andreatch, "Technique for connecting electrical leads to semiconductors," J. Applied Physics, vol.28, no.8, p.923, 1957. (DOI: 10.1063/1.1722893).
- [2] P.H. Dehkordi and D.W. Bouldin, "Design for packageability-early consideration of packaging from a VLSI designer's viewpoint," Computer, vol.26, no.4, pp.76–81, 1993. (DOI: 10.1109/2.206519).
- [3] C.-T. Tsai, "Package inductance characterization at high frequencies," IEEE Trans. Compon. Packaging Manuf. Technol.: Part B, vol.17, no.2, pp.175–181, 1994. (DOI: 10.1109/96.330432).
- [4] H.-Y. Lee, "Wideband characterization of mutual coupling between high density bonding wires," IEEE Microw. Guided Wave Lett., vol.4, no.8, pp.265–267, 1994. (DOI: 10.1109/75.311493).
- [5] H.-Y. Lee, "Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits," IEEE Trans. Microw. Theory Tech., vol.43, no.1, pp.63–68, 1995. (DOI: 10.1109/22.363006).
- [6] S.-K. Yun and H.-Y. Lee, "Parasitic impedance analysis of double bonding wires for high-frequency integrated circuit packaging," IEEE Microw. Guided Wave Lett., vol.5, no.9, pp.296–298, 1995. (DOI: 10.1109/75.410403).
- [7] H. Patterson, "Analysis of ground bond wire arrays for RFICs," Proc. IEEE MTT-S Int. Microw. Symp. Dig. 2, pp.765–768, 1997.
- [8] K.W. Goossen, "On the design of coplanar bond wires as transmission lines," IEEE Microw. Guided Wave Lett., vol.9, no.12, pp.511–513, 1999. (DOI: 10.1109/75.819415).
- [9] X. Qi, P. Yue, T. Arnborg, H.T. Soh, H. Sakai, Z. Yu, and R.W. Dutton, "A fast 3D modeling approach to electrical parameters extraction of bonding wires for RF circuits," IEEE Trans. Advanced Packaging, vol.23, no.3, pp.480–488, 2000. (DOI: 10.1109/

6040.861564).

- [10] F. Alimenti, P. Mezzanotte, L. Roselli, and R. Sorrentino, "Modeling and characterization of the bonding-wire interconnection," IEEE Trans. Microw. Theory Tech., vol.49, no.1, pp.142–150, 2001. (DOI: 10.1109/22.899975).
- [11] X. Qi, "High frequency characterization and modeling of on-chip interconnects and RF IC wire bonds," Ph.D. Dissertation, Stanford University, 2001.
- [12] A.L. Nazarian, L.F. Tiemeijer, D.L. John, J.A. van Steenwijk, M. de Langen, and R.M.T. Pijper, "A physics-based causal bond-wire model for RF applications," IEEE Trans. Microw. Theory Tech., vol.60, no.12, pp.3683–3692, 2012. (DOI: 10.1109/TMTT. 2012.2217983).
- [13] H. Mirmazhari, A. Taghizadeh, J. Sobhi, and Z.D. Koozehkanani, "A high efficiency DC-DC converter using a new in-package structure of bonding-wire inductor," IEICE ELEX, vol.9, no.11, pp.1005–1011, 2012. (DOI: 10.1587/elex.9.1005).
- [14] I. Ndip, A. Öz, H. Reichl, K.-D.Lang, and H. Henke, "Analytical models for calculating the inductances of bond wires in dependence on their shapes, bonding parameters, and materials," IEEE Trans. Electromag. Compat., vol.57, no.2, pp.241–249, 2015. (DOI: 10.1109/TEMC.2014.2378284).
- [15] T.V. Dinh, J. Pagazani, D. Lesénéchal, D. Pasquet, P. Descamps, G. Lissorgues, and P. Nicole, "Bonding-wire-geometric-profiledependent model for mutual coupling between two bonding wires on a glass substrate," IEEE Trans. Compon. Packaging Manuf. Technol., vol.5, no.1, pp.119–127, 2015. (DOI: 10.1109/TCPMT. 2014.2366730).
- [16] T. Nakura, M. Kano, M. Yoshizawa, A. Hattori, and K. Asada, "Resonant power supply noise reduction by STO capacitors fabricated on interposer," IEICE Trans. Electron., vol.E98-C, no.7, pp.734–740, July 2015. (DOI: 10.1587/transele.E98.C.734).
- [17] C. Wang, J. Zheng, G. Wang, W. Gao, and Q. Hua, "Parasitic effects analysis of bonding wires bonding parameter of intelligent power modules for three-phase motor control applications," J. Phys.: Conf. Ser. 1607 (IOP Pub., 2020) 012036. (DOI: 10.1088/ 1742-6596/1607/1/012036).
- [18] P.C. Cherry and M.F. Iskander, "FDTD analysis of high frequency electronic interconnection effects," IEEE Trans. Microw. Theory Tech., vol.43, no.10, pp.2445–2451, 1995. (DOI: 10.1109/22. 466178).
- [19] C. Schuster, G. Leonhardt, and W. Fichtner, "Electromagnetic simulation of bonding wires and comparison with wide band measurements," IEEE Trans. Adv. Packag., vol.23, no.1, pp.69–79, 2000. (DOI: 10.1109/6040.826764).
- [20] C.H. Doan, S. Emami, D.A. Sobel, A.M. Niknejad, and R.W. Brodersen, "Design considerations for 60 GHz CMOS radios," IEEE Commun. Mag., vol.42, no.12, pp.132–140, 2004. (DOI: 10.1109/ MCOM.2004.1367565).
- [21] B. Razavi, "Design of millimeter-wave CMOS radios: A tutorial," IEEE Trans. Circuits Syst. I Regul. Pap., vol.56, no.1, pp.4–16, 2009. (DOI: 10.1109/TCSI.2008.931648).
- [22] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," IEEE J. Solid-State Circuits, vol.48, no.1, pp.46–65, 2013. (DOI: 10.1109/JSSC.2012.2218066).
- [23] T. Kikkawa, Y. Masui, A. Toya, H. Ito, T. Hirano, T. Maeda, M. Ono, Y. Murasaka, T. Imamura, T. Matsumaru, M. Yamaguchi, M. Sugawara, A. Azhari, H. Song, S. Sasada, and A. Iwata, "CMOS Gaussian monocycle pulse transceiver for radar-based microwave imaging," IEEE Trans. Biomed. Circuits Syst., vol.14, no.6, pp.1333–1345, 2020. (DOI: 10.1109/TBCAS.2020.3029282).