FOREWORD

Special Section on Low-Power and High-Speed Chips

Low-power, high-speed chips (COOL Chips) encompass a broad range of architectures, applications, methodologies, and usage models, and are essential fundamental techniques to realize Green Transformation (GreenX). These technologies are present in AI, IoT, multimedia, digital consumer electronics, mobile, graphics, encryption, robotics, automotive, networking, medical, healthcare, and biometrics. They are based on novel architectures and schemes for single/multi/many-cores, NoC, embedded systems, reconfigurable computing, grid, ubiquitous, dependable computing, GALS, and 3D integration. COOL software, which includes parallel schedulers, embedded real-time operating systems, binary translations and compiler issues and low power application techniques, is also emerging.

These technologies all aim to reduce power consumption and enhance chip performance. Regardless of their goals, all of industry has been challenged with developing optimal solutions—both hardware and software—for power optimization according to the required performance. In general, to migrate decades' worth of legacy approaches to low-power technology, researchers approach these optimal solutions from the perspective of starting from scratch.

With this in mind, we've been organizing annual COOL Chips conferences since 1998. We celebrated COOL Chips 24 in April 2021. COOL Chips, a sister conference to HOT CHIPS, focuses on all aspects of cool technologies. Approximately 150 individuals attend the conference each year. In addition to regular paper presentations, the conference includes keynotes and invited talks, special topic presentations, posters and panel discussions. To attract submissions from engineers working in industry, the program committee bases acceptance on a 3-page extended abstract as well as a 6-page paper. The conference proceedings include the final presentation slides with the abstract or the paper. All program committee members reviewed each of the 14 submissions for COOL Chips 24 and selected the 10 bests on the basis of technical merit and innovation.

It is our great honor to announce the publication of this special section on Low-Power and High-Speed Chips. The section is devoted to variety of techniques for COOL Chips. It contains 3 papers, among 5 submissions, which covers, performance- and energy-efficient CNN Accelerators, a binary translator for deep-learning processing library, and a metadata prefetching mechanism for hybrid memory architecture.

On behalf of the editorial committee, we would like to express our sincere appreciation to all the authors for their contributions and to all the reviewers for their critical reviewing papers. Lastly, We would like to thank the editorial committee for their work on this special section, especially, secretaries: Prof. Wada and Prof. Egawa.

Fumio Arakawa and Makoto Ikeda, Guest Editors

Fumio Arakawa *(Senior Member)* is a designated researcher of d.lab at the University of Tokyo, and an invited professor of Graduate School of Informatics at Nagoya University. His research interests include architecture and micro-architecture of low-power and high-performance processors. He has founded an R&D and consulting company, Famer Systems, Inc. to contribute on industries with his R&D experience of Hitachi and Renesas Electronics. He is an organizing committee co-chair of the COOL Chips conference series, and the chairman of Microprocessor Technical Committee of JEITA. He served as a Guest Editor of IEEE Micro for seven times, and TPC members of conferences including ISSCC, VLSI Circuits Symposium, A-SSCC, and MCSoC. He has a Ph.D. in electrical engineering from the University of Tokyo. He is a member of IEEE and IEICE.

Makoto Ikeda *(Senior Member)* is a professor at Systems Design Lab (d.lab), the University of Tokyo. His research interests include high-performance, low-power, and reliable digital circuit, especially for hardware security and smart image sensor design. He received BE, ME and PhD in Electrical Engineering from the University of Tokyo, in 1991, 1993 and 1996, respectively. He's a program committee co-chair of the COOL Chips conference series and has served program chair of International Solid-State Circuits Conference, VLSI Circuits Symposium, Asian Solid-State Circuits Conference. He is a Senior Member of IEEE, and IEICE, and a member of ACM, and IPSJ.