FOREWORD

Special Section on Analog Circuits and Their Application Technologies

It is my great honor and pleasure to announce the publication of this special section on analog circuits and their application technologies.

The rapid progress of IoT, AI, 5G, quantum computing demands the evolution of integrated circuits in the fields such as wireless/wireline communication, sensing systems, health/biomedicine, signal processing, power management, edge computing, and cryo-CMOS, where analog circuits have been playing a crucial role. In addition to pure analog techniques, the scope of this special section includes fundamental issues such as co-design of analog/digital circuits, analog circuits in SoCs, analog circuit design for manufacturability (DFM) and testability (DFT), device modeling techniques, and hardware security. Analog circuits with high performance and enhanced functionality as well as low power and low cost are challenging to design but strongly demanded for next-generation applications. Thus, this special section aims to advance the state of the art in analog circuits and their application technologies.

This special section has 11 excellent papers including 3 invited papers. 5 regular papers, and 3 brief papers covering quick startup low-power hybrid crystal oscillator, injection-locked frequency divider, power-scalable sub-sampling PLL, SOI-based lock-in pixel with a shallow buried channel, nonvolatile storage cells using FiCC, On-chip characterization of backside ESD impacts, Security attack on SAR ADCs, and reconfigurable input unit designs. The first invited paper by Prof. Akira Matsuzawa from Tech Idea and Tokyo Institute of Technology presents “A Brief History of Nyquist Analog-to-Digital Converters”. The second invited paper by Dr. Nick Van Helleputte, Dr. Carolina Mora-Lopez, and Dr. Chris Van Hoof from IMEC present “Design of CMOS circuits for electrophysiology”. The third invited paper by Dr. Chris Mangelsdorf, former member of Analog Devices presents “Encouraging Innovation in Analog IC Design”.

On behalf of the editorial committee, I would like to express our sincere appreciation to all the authors who submitted their manuscripts for this special section. I would also like to take this opportunity to thank all the reviewers and all of the editorial committee members, as listed below, for their enthusiastic support. Finally, I would like to thank Prof. Takuji Miki, Prof. Makoto Takamiya and Dr. Yohei Nakamura for their extensive contribution as guest editors.

Kazuko Nishimura (Panasonic Holdings Corporation), Guest Editor-in-Chief

Kazuko Nishimura *(Nonmember)* received the B.E. degree in mechanical engineering from Osaka University, Osaka, Japan in 1995 and the Ph.D. degree in technology and innovation from Kobe University, Hyogo, Japan in 2022. She joined the Semiconductor Research Center, Panasonic Corporation where she engaged in R&D of high-speed analog-to-digital converters in 1995. Her team developed ultra-high-speed ADCs and contributed for a lot of digital read channel applications; DVDs and DVCs. From 1998 to 2007, she joined the task force of optical communication systems, and developed fiber-to-the-home systems. Her team developed Gbit/s-class CMOS burst-mode optical transceivers. From 2009 to 2012, she worked in R&D of RF systems. Her team developed industry's-first LSI that integrated one-segment tuner and demodulation function. From 2006 to 2014, she developed CMOS image sensors and contributed various applications. Currently, she is a manager in Technology Division, Panasonic Holdings Corporation and pursues research on the organic photoconductive film (OPF) CMOS image sensors and sensor applications. She serves A-SSCC data converter subcommittee chair and ISSCC Imagers, Medical, MEMS and Displays subcommittee, SSCS Adcom and Image Sensor Europe advisory board. She is a senior member of IEEE.