

Design of CMOS Circuits for Electrophysiology

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SUMMARY Electrophysiology, which is the study of the electrical properties of biological tissues and cells, has become indispensable in modern clinical research, diagnostics, disease monitoring and therapeutics. In this paper we present a brief history of this discipline and how integrated circuit design shaped electrophysiology in the last few decades. We will discuss how biopotential amplifier design has evolved from the classical three-opamp architecture to more advanced high-performance circuits enabling long-term wearable monitoring of the autonomous and central nervous system. We will also discuss how these integrated circuits evolved to measure in-vivo neural circuits. This paper targets readers who are new to the domain of biopotential recording and want to get a brief historical overview and get up to speed on the main circuit design concepts for both wearable and in-vivo biopotential recording.

key words: *biopotential amplifier, instrumentation amplifier, ECG, EEG, neural recording*

1. Introduction

The roots of electrophysiology can be traced back to the groundbreaking research from Luigi Galvani, published in 1791 [1]. He discovered that the muscles of dead frogs could be activated by the application of electrical currents, effectively performing early electrostimulation experiments. Galvani's research inspired numerous other scientists to further explore the concept of "bioelectricity". Despite the ingenuity with which scientists like Galvani and others explored these concepts, they were hindered by the technology available at the time. Their quests to understand the fundamentals of how our nervous system works inevitably kickstarted a technological development race with the sole goal of being able to record the minute electrical currents and potentials of tissue and even individual cells. In 1828, Leopoldo Nobili was able to record actual electrical signals from animal tissue making use of an electromagnetic galvanometer. These were very intricate devices based on the principle that current through a coil generates a magnetic field, which was used to deflect a pointer in proportion to the current magnitude. Incredibly, these devices, while being very cumbersome to work with, allowed early pioneers like Nobili to measure the very small currents (down to 100pA) of nerve fibers. The first electrical instrumentation for rudimentary electrophysiology was born. In the 1850s, Hermann von Helmholtz experimented with galvanometers

and was able to measure the propagation speed of electrical signals along a nerve fiber. In the following decade, Étienne-Jules Marey experimented with various techniques to measure the heartbeat signal. Initial attempts included implanting small balloons into the heart chambers of a horse and using a catheter to measure intracardiac pressure. While he was able to acquire a heartbeat recording this way, Marey quickly realized that an electrical means of recording would be a lot more convenient and yield more precise insights. In 1876, he succeeded, using a Lippmann capillary electrometer to measure the electrical activity in an exposed heart of a frog, which can be considered the first true electrocardiogram recording ever. Only 1 year later Augustus D. Waller managed the first human electrocardiogram (ECG) with a similar Lippmann electrometer [2]. Interestingly, Waller managed this with surface electrodes which were strapped to the front and back of the chest. He later used saline jars in which the subjects' extremities were immersed. This work inspired Willem Einthoven, who invented a new type of string galvanometer, making use of fine quartz string coated in silver (see Fig. 1). Einthoven developed a number of techniques and also laid foundational groundwork for ECG recording and interpretation. It was Einthoven who first named the PQRST waves in an ECG. For his groundbreaking work he was awarded the Nobel Prize in 1924. Electrophysiology has since grown to become one of the most important medical techniques to measure biopotentials originating from the heart (electrocardiogram - ECG), the brain (electro-encephalogram - EEG) or muscles (electromyogram - EMG). CMOS technology allowed for a rapid development of very powerful, ultra-low-power and

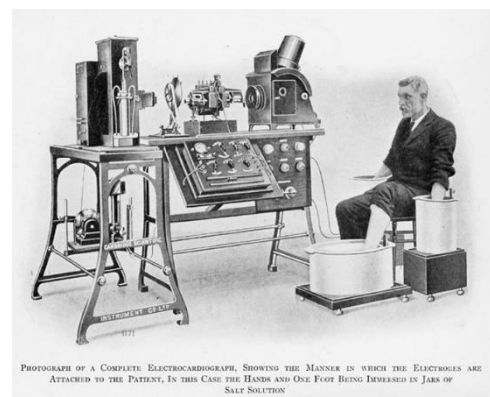


Fig. 1 Einthoven's galvanometer.

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highly integrated electronic readout interfaces.

2. Wearable Cardiac Monitoring

The foundational measurement technique pioneered by Einthoven in essence is still valid today, although the saline jars have been replaced with small and comfortable electrodes. In clinical practice often silver/silver-chloride gel electrodes are used which provide a reasonably low-impedance contact in the bandwidth of interest. However, for long-term monitoring, dry electrodes are preferred for improved patient comfort. Since dry electrodes usually have much larger impedances, this poses more strict requirements on the required input impedance of the readout electronics. Figure 2 shows the typical signal amplitudes and frequency ranges of interest of typical biopotential signals.

Figure 3 shows a typical ECG recording setup. To amplify the biopotential signal, a fully-differential high input-impedance instrumentation amplifier (IA) is used. This IA usually dominates the overall performance, such as noise, input impedance, CMRR and power. The main design challenges for a decent biopotential IA are to achieve a low noise performance in the presence of large DC offset and low frequency drift, originating from the polarization voltage of the electrodes. The IA should also have a high input impedance to avoid signal attenuation due to the electrode impedance and avoids common-mode to differential mode conversion due to electrode impedance imbalance. In fact, the complete readout should achieve high CMRR to reject mains interference. Finally motion artefacts will appear as differential signals within the band of interest necessitating a sufficiently

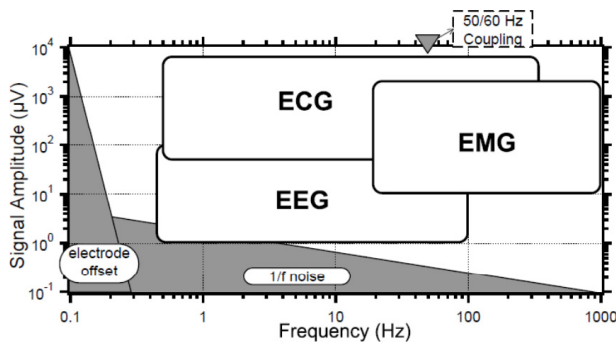


Fig. 2 Typical signal amplitude and frequency of biopotential signals

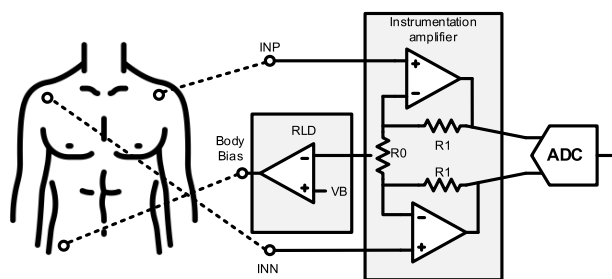


Fig. 3 Typical ECG recording with driven-right-leg body biasing.

large differential input range to avoid saturation. Notice that the electronics should be electrically with respect to the body. This is usually done via a 3rd electrode which biases the body to a DC voltage. In Fig. 3, this happens through an active feedback loop called “right-leg drive (RLD)”. This circuit monitors the input common-mode voltage and compares it with a bias voltage (VB) and drives to body to ensure the input common-mode voltage remains equal to VB. Figure 3 shows a simplified version, because the RLD signal has to be filtered to ensure loop stability. The benefit of RLD body biasing is that can suppress mains interference. However, other body biasing methods are commonplace also. It is even possible to bias the input leads with high-valued resistors to record an ECG with only 2 electrodes. With a growing interest in wearable, battery-powered devices, there was a need to come up with ultra-low-power circuits meeting all these design requirements.

There are various commonly used architectures for IAs, each having their own benefits and drawbacks. Probably the most well-known architecture is the 2-opamp IA where the input amplifiers act as impedance buffers (Fig. 3). Since the inputs go the CMOS gates, it inherently provides high input impedance, only limited by the parasitic input capacitances. But it relies on resistor matching to achieve a good CMRR and it doesn’t provide a good power-noise trade-off. The primary noise contributors will be the input amplifiers and the feedback resistor R0. Hence for low-noise, the amplifiers need large-power input stages (to have low-noise input differential pairs) as well as large-power output stages (to drive R0 which needs to be small for noise considerations). Furthermore, since it is DC-coupled in nature, the IA cannot have high gain to avoid saturation due to the DC electrode offset (DEO), which puts stringent noise specifications on the subsequent blocks.

Single-opamp AC-coupled amplifiers (Fig. 4 (a)) have been proposed achieving very low power consumption since they don’t suffer from the above-mentioned power-noise tradeoff. While AC-coupling can effectively filter the DC-offset from the electrodes, this requires very low (sub-Hz) cutoff frequencies. This can be implemented on chip using transistors in cut-off region to create very large resistances, called pseudo-resistor [3]. However, these have very poor accuracy and are extremely sensitive to PVT varia-

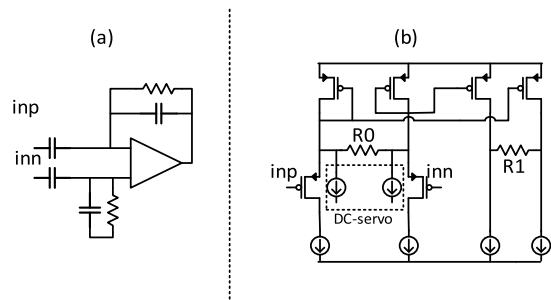


Fig. 4 Other commonly used IA architectures are single-opamp capacitive-coupled IA (a) or current-feedback (b)

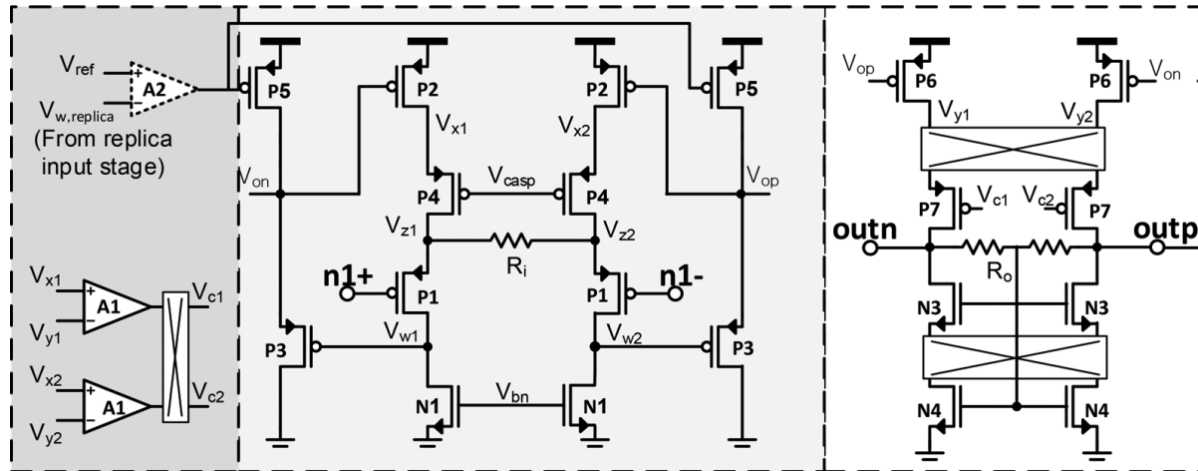


Fig. 5 Chopper-modulated current-feedback amplifier.

tions. Switched-resistor implementations [4] solve this issue by switching a medium sized resistor only for a short period, so the effective resistance is boosted by the duty cycle of the pulse at the expense of a high frequency clock. Arguably a bigger drawback of AC-coupled architectures is that they suffer from low input impedance, especially when chopping [5] is performed prior to the input capacitors to mitigate the IA's intrinsic $1/f$ noise. Because of the extremely stringent noise requirements and the low frequency-band of interest, chopping is almost always employed in biopotential IA's.

Current-Feedback IAs (CFBIA—Fig. 4 (b)) have emerged as an interesting alternative to obtain a high CMRR (which doesn't rely on resistor matching) while maintaining low power consumption [6], [7]. The noise will be determined by the input stage and resistor R_0 . Contrary to the 3-opamp IA, the input stage actually drives this resistor. Hence, CFBIAs don't require high-power output stages to satisfy the noise requirement. Figure 5 shows a possible circuit implementation of a chopper-modulated CFBIA [6]. The input-stage is based on a so-called flipped voltage follower. The input-devices (P1) are biased in source follower mode, and hence act primarily as impedance buffers copying the input voltage to their sources. The input voltage is converted into a current via resistor R_i . This differential signal current flows into devices P2 and is mirrored to the output stage via current mirrors P2/P6. It is eventually converted back to an output voltage via R_o . P5, P3 are just level shifters to maintain proper biasing of the flipped voltage follower. The whole structure is chopper-modulated to reduce $1/f$ noise.

To deal with the DEO, either passive high-pass filtering, or active DC-servo loops (DSL) can be used by injecting an offset current into R_0 as shown in Fig. 4 (a). Both of these solutions have drawbacks, however. DSLs usually have a limited range of a few 10s of mV [7], [8]. Increasing this range can only be achieved by increasing R_0 (which leads to higher noise) or increasing the current (which leads to higher power consumption). In addition, a large DC-

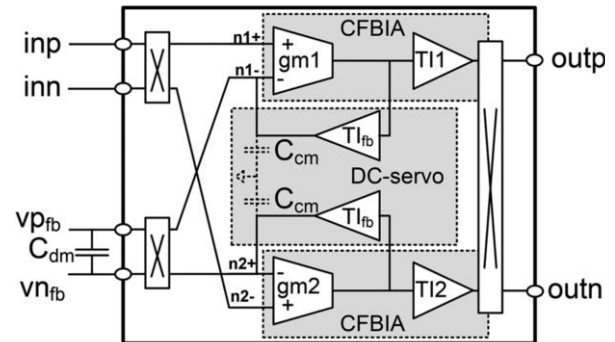


Fig. 6 Chopper-modulated IA based on dual difference CFBIAs to achieve large DEO rejection.

offset will result in a significant operating point mismatch in the input differential pair which would negatively impact the CMRR and linearity.

To break this trade-off, we proposed a current-feedback IA based on a dual difference amplifier where the second input differential pair is used to implement a large signal servo loop [9]. Figure 6 shows the block diagram of the proposed IA architecture. It consists of two internal CFBIAs similar to [6] for the forward signal path and a feedback loop which behaves differently for common-mode signals than for differential mode signals and is responsible for rejecting the DEO. The input signals of the IA contain three main components: 1) desired differential signal of interest (ECG); 2) undesired DEO; and 3) undesired common-mode interference. The proposed IA rejects the two undesired components by replicating both of them at the output of the feedback loop and feeding those signals to the negative inputs of the CFBIAs where they will be rejected by the inherent high CMRR of the CFBIA. Notice that it is not sufficient to provide only the DEO at the output of the feedback loop as traditional DC-servo loops do. To achieve a good CMRR, it is necessary to ensure that the differential input pairs of each of the individual forward amplifiers will see exactly the same common-mode signals. Each CB-

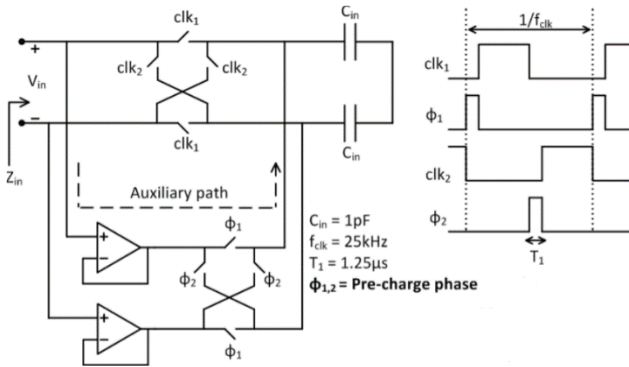


Fig. 7 Input impedance boosting by using two auxiliary buffers [4].

FIA consists of a transconductance (G_m) stage which converts the differential input voltage into a current which is copied to the transimpedance (TI) output stage. The DC-servo consists of a similar TI stage but with high DC-gain (T_{ifb}) and capacitors C_{dm} and C_{cm} . It essentially acts as a high-pass filter (HPF) with cutoff frequency set by C_{dm} for differential mode (DM) signals (assuming $C_{dm} \gg C_{cm}$). For common-mode signals, however, C_{dm} acts as an open (same common-mode voltage across its terminals) and the HPF cutoff is determined by C_{cm} for common-mode signals. This results in an architecture where the CM HPF can be controlled independently from the DM one. Such an arrangement rejects the differential polarization voltages below 0.5 Hz as well as the CM mains interference at the input stage before amplification. Hence the IA can have a large gain since it will not saturate due to the DC-offset. Since no additional circuitry is added to the input lines to implement the DEO filtering, the proposed architecture achieves very high input impedance. The noise contribution of the feedback loop will be filtered by C_{dm} which is sufficiently large so that the overall noise level isn't significantly increased. Finally, since the DC-offset is not cancelled after the input differential pair of the gm-stage the proposed method doesn't face the power versus noise versus DC-offset range tradeoff from CFBIAs with DC-servos. The DC-offset range is now only limited by the common-mode input range of the CFBIAs which can be several 100s of mV. With such DC-coupled chopper-modulated IAs with active DC servo loops, the input impedance is limited mostly by the parasitic capacitances on the input lines, which is even more prominent when chopper modulation is applied. Input impedance boosting techniques as shown in Fig. 7 can achieve $>10^{10}$ Ohm input impedances by pre-charging these parasitic caps prior switching the choppers.

For applications like EEG, where scalp electrodes are placed all over the scalp, additional challenges arise. Especially if dry electrodes are used, the long routing to the differential IAs coupled with the high electrode impedance makes this system very prone for signal degradation and noise pickup before the signal even reaches the IA. An electrode with a co-integrated amplifier, namely Active Electrode (AE) [10] can reduce noise pick-up by minimizing

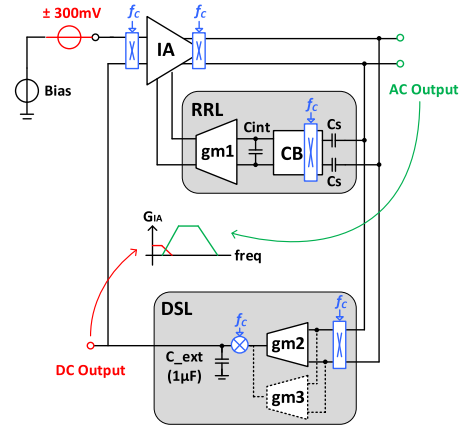


Fig. 8 An IA-based active electrode for EEG recording.

the length of cabling between the electrode and the amplifier's input. However, there are significant challenges to realize a medical-grade system with low-noise, high-input impedance, large electrode offset tolerance, and high CMRR while making use of Active Electrodes. Analog buffers have low output impedance and low gain variation across process corners. In addition, analog buffers require only 3 connections between the AE and the rest of the system (V_{dd} , V_{ss} and V_{out}). However, a major drawback of the buffer AE systems is their noise-power efficiency. Analog buffers only perform impedance conversion without providing any voltage gain. As a result, the succeeding back-end circuit also needs target low-noise performance, increasing the power dissipation of the overall system. An AE can be also implemented using instrumentation amplifiers. By amplifying signals using AEs, noise and precision requirements of the following stages are significantly relaxed, reducing the power dissipation of the overall system. Figure 8 shows one particular implementation of an IA-based AE [10]. The input electrode signal is amplified while the DC polarization voltage is rejected using a DSL. The DSL is implemented with a gm-C integrator that tracks the output offset and then cancels it by driving the IA's inverting input. The biggest advantage of voltage-to-voltage feedback based on gm-C architecture is that it can compensate up to hundreds of mV electrode offset with low power. Figure 8 also shows another interesting technique, the ripple-reduction-loop (RRL). While chopping is a very powerful technique to mitigate $1/f$ noise, chopper clock feedthrough can lead to chopper-glitches in the output which after low-pass filtering manifest in ripple at the chopper clock frequency. This high-frequency ripple can be converted to baseband and removed via low-pass filter and negative feedback as shown in Fig. 8.

The concept of an active electrode combined with various input impedance boosting techniques where all parasitic input capacitances are bootstrapped out and even ESD protection leakage is compensated (see Fig. 9), can achieve up to 400 GOhm of input impedance [11]. Such a high input impedance is interesting for extremely high electrode impedances, namely purely capacitively coupled elec-

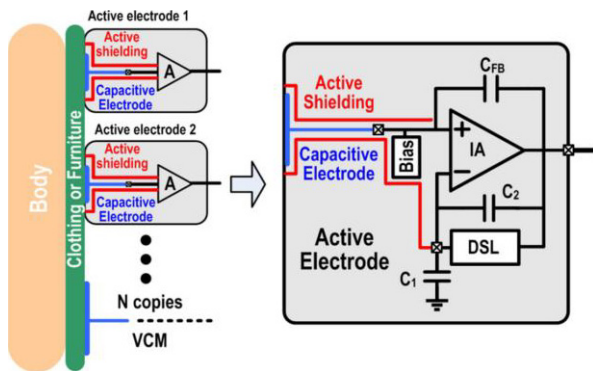


Fig. 9 Active electrode for non-contact capacitive ECG recording.

trodes. These kind of electrodes do not even require physical connection to the skin and enable biopotential recording through thin layers of clothing.

3. In-Vivo Neural Interfacing

So far, we have mostly talked about electrophysiology in the framework of systemic non-invasive recording. These systemic biopotentials ultimately arise from cellular activity. In order to better understand cellular pathways and how they contribute to systemic mechanisms, researchers have tried to measure the minute biopotentials of nerve fibers and even individual cells. While traditionally patch-clamp technology has been used for recording these, patch-clamps are not very scalable. Implantable neural probes are currently the most widely used tool to monitor electrical neural activity at single-cell level [12], [13]. Although they have been fabricated using diverse techniques and materials, silicon neural probes have become popular because they offer important advantages such as precise definition of shank shapes and recording sites, accurate fabrication processes and automation capabilities to produce low-cost microprobes in large volumes. Additionally, silicon probes can integrate CMOS circuits in the same silicon substrate [14]–[19], thus enabling the implementation of a large number of electrodes with a reduced number of connecting wires.

In order to design effective and robust tools for neural recording, the following challenges need to be tackled:

- *Neural signal amplitude and frequency:* With implantable devices, it is possible to sense two types of neural signals [2]. The action potentials (AP) or spikes are fast transients that represent single-neuron activity and have amplitudes from 10's to 100's of μV . Their signal bandwidth is from ~ 300 Hz to 10 kHz. The local-field potentials (LFPs) in the lower frequency (< 1 Hz to ~ 1 kHz) represent the combined activity of many neurons in a volume of tissue and have amplitudes from 100's of μV to a few mV.
- *High-density neural interfaces:* In order to increase the recording yield and cover larger brain volumes, high-density neural probes connected to high-channel-count readout chips are required [14]–[17]. In such tools, the

readout channels must achieve very low power consumption and very small area so that they can easily be scaled. Furthermore, the channel electrical performance must be robust over process, voltage and temperature (PVT) variations so that a high channel-to-channel uniformity can be achieved.

- *Electrode DC offset (EDO):* The DC voltage between the recording and reference electrode will mostly depend on the materials of both electrodes and it can reach 100's of mV. However, the total EDO that is seen by the readout channel will depend on the attenuation caused by the channel's DC input impedance.
- *Electrode impedance:* Very small (e.g. $< 30\text{-}\mu\text{m}$ diameter) electrodes are desirable for the recording of APs and LFPs with implantable probes. Therefore, depending on the material, these electrodes can exhibit very large impedances and high thermal noise. Although many new materials and fabrication techniques have been proposed in the last decades to maximize the surface area and minimize the impedance of an electrode [21], the electrode impedance is still in the range of 100's of k Ω to a few M Ω at 1 kHz.

Two very important trends in neural readout architectures can be found in literature to tackle the above mentioned challenges: i) a conventional architecture consisting of one or more amplification stages followed by an analog-to-digital converter (ADC), and ii) a trendy direct-digitization approach where the input transconductance stage is merged within the ADC loop. The characteristics, advantages and disadvantages of these architectures are discussed in this section.

3.1 IA-ADC Readout Architectures

The most widespread architecture for neural-signal readout consists of an AC-coupled instrumentation amplifier (IA) followed by a time-multiplexed moderate-resolution (8-12 bits) ADC [14]–[16], [22]–[31]. AC coupling is the most effective way to deal with EDOs, since it is possible to achieve rail-to-rail EDO rejection without complex feedback loops. In order to bias the IA input nodes at DC, pseudo-resistor elements that can achieve up to T Ω resistances are utilized [3]. Although these pseudo-resistor elements have some important disadvantages, namely high sensitivity to process variation and light as well as strong non-linearity with voltage, they are still the most power- and area-effective way of implementing the ultra-low cutoff frequencies required to record LFPs (< 1 Hz). The AC coupling capacitor must be large enough to provide sufficient gain (e.g. 50-100 V/V) in a closed loop IA, but not too large to avoid excessive deterioration of the AC input impedance. To solve this trade-off, the minimum feedback-capacitor size, the electrode impedance, the supply voltage and the area constraints must be taken into account. Contrary to the common belief that AC-coupling requires large area, the area of this input capacitor is normally not a big concern since it can be placed

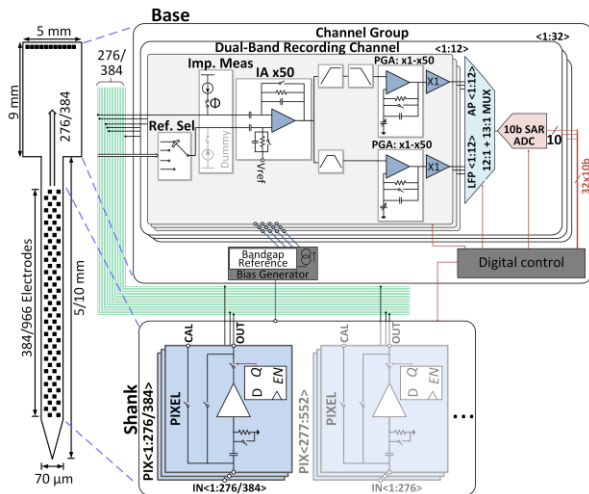


Fig. 10 High-level architecture of the 384-channel neural probe reported in [15].

on top of the active circuits when it is implemented using metal-insulator-metal (MIM) or metal-oxide-metal (MOM) devices. Therefore, EDO rejection using AC-coupling and pseudo-resistors can be both area and power efficient.

Diverse operational-transconductance-amplifier (OTA) architectures can be used to achieve a good trade-off among power, area and noise in the IA. The most popular choices are folded-cascode [14]–[16], [23]–[25], [31] and inverter-based [22], [27], [30] OTAs. The latter can achieve impressive area and power performances while maintaining a low noise. However, it is very difficult to keep this OTA well biased over PVT variations, making it less robust for high-density recording architectures where a uniform channel-to-channel performance is crucial to guarantee signal quality.

In order to solve the trade-off between the power and area required for the ADC and its preceding driver, the multiplexing ratio needs to be optimized as proposed in [32]. A SAR ADC is normally used in this application due to its good power performance in the moderate-resolution and low-frequency ranges [33]. However, hybrid ADCs combining properties of different traditional architectures are also popular since they can be customized to achieve the required power, area, resolution and speed.

An example of a conventional IA-ADC readout architecture can be found in the 384-channel CMOS neural probe reported in [15]. The high-level architecture of this probe is shown in Fig. 10. In this design, each channel is split in two signal paths to filter and amplify the APs and LFPs separately. In this way, the resolution of the SAR ADC can be kept lower (10 bits) to reduce its area contribution. A shared fixed (50 V/V) amplification plus an independent variable (1–50 V/V) amplification are included in the signal paths. A 12:1 multiplexing ratio is used here to optimize the channel area and power. The channel design was optimized to achieve PVT robustness and very good channel-to-channel uniformity. Today, this neural probe is widely used by the neuroscience community, becoming the new gold standard

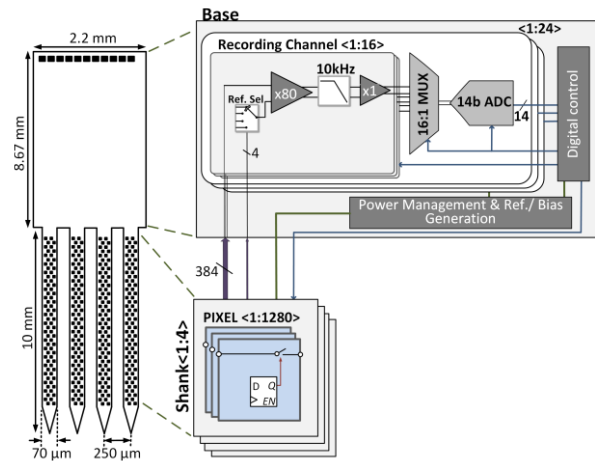


Fig. 11 High-level architecture of the 384-channel neural probe reported in [16].

in *in vivo* electrophysiology.

To significantly reduce the area in [15], the CMOS neural probe in [16] implements a full-band readout channel followed by a higher resolution (14 bits) hybrid SAR-assisted pipeline ADC (Fig. 11). In this way, the area-consuming band splitting filters could be eliminated. The channel includes only one fixed amplification stage (80 V/V), while a multiplexing ratio of 16:1 is used. This design achieved an area reduction of >3x for the same number of channels.

3.2 Direct-to-Digital Readout Architectures

The conventional AC-coupled readout architectures described above suffer from a few significant drawbacks and limitations: i) they heavily rely on analog-intensive techniques to implement the front-end IA and, in some cases, the bandpass filter to separate AP and LFP bands, which make their scalability with technology difficult; ii) the pseudo-resistors used for input biasing are highly sensitive to process variation and light, nonlinear, and very prone to large offsets caused by leakage currents; iii) due to the front-end high-gain amplification, such designs have a limited input dynamic range (typically <20 mVpp), which makes them prone to saturation by the large stimulation artifacts in closed-loop neuromodulation applications. To address these challenges, direct-to-digital readout architectures (i.e., without front-end high-gain amplification) that use oversampling ADCs have been explored extensively in the last years [19], [34]–[56]. Depending on the required input range, these designs can generally be classified into two different categories: recording-only architectures and artifact-tolerant architectures for bidirectional neural interfaces.

For neural recording in the absence of artifacts, a moderate-resolution ADC (~8–11 bits) can be employed to directly digitize the raw neural signals in a very area- and power-efficient manner, while the large EDOs can be either compensated by a mixed-signal DSL [34] or filtered out by conventional AC-coupling [38], [41], as shown in

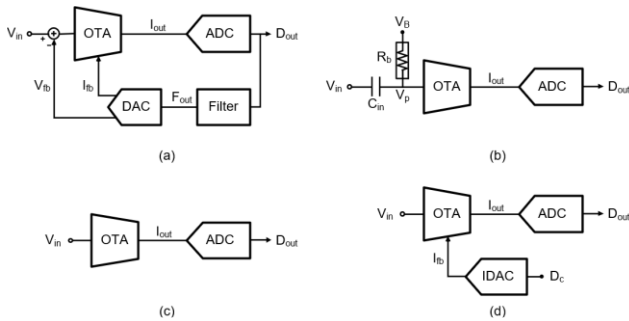


Fig. 12 Diagrams of recording-only direct-to-digital neural readouts with, (a) mixed-signal DSL, (b) AC coupling, (c) ADC linear input range, and (d) coarse IDAC for EDO compensation.

Fig. 12(a) and 12(b). The main drawback of the DSL-based approaches is the limited EDO compensation range, typically ~ 100 mVpp. Although this range can be extended, it may result in significant area and/or power overhead for the high-resolution and wide-dynamic-range feedback DACs. For this reason, significant area reduction has been obtained in [19] by removing the EDO compensation loop (see Fig. 12(c)). Nevertheless, such approach suffers from either degraded noise ($20.19 \mu\text{Vrms}$) or limited EDO tolerance (22.5 mVpp). While adding a coarse offset IDAC (Fig. 12(d)) extends the EDO cancellation range up to 120 mVpp in [39], it results in significant noise degradation due to the unbalanced input differential pair when large EDOs are present. In contrast, rail-to-rail EDOs can be tolerated by using AC coupling. The penalty is the required large-area coupling capacitors. This claim, however, has been challenged in some recent designs [38], [41]. This is because the capacitor can be designed reasonably small via proper engineering, and its density increases with technology scaling as more metal layers are available and the spacing between two adjacent metal tracks becomes narrower. Additionally, the AC-coupling capacitor can be stacked above the active circuits for further area saving. At the same time, the drawbacks associated with the pseudo-resistor biasing can be avoided by periodically resetting the OTA input to its common mode [53], [57], applying a reset when the OTA input drifts outside the linear input range of the ADC [38], or resetting via the incremental operation [45]. The reset-induced kT/C noise is usually not a big concern since it gets averaged and becomes negligible compared to the overall ADC input-referred noise due to the very infrequent reset operation [38], or converted into out-of-band chopper ripple and then filtered out by the subsequent integrator [45].

For artifact-tolerant recording, many different readout architectures based on delta-sigma ($\Delta\Sigma$) modulation, Δ modulation, and a combination of both (i.e., $\Delta\text{-}\Delta\Sigma$ or $\Delta 2\Sigma$) have been proposed. On the one hand, to accommodate both the large EDOs and stimulation artifacts on top of the weak neural signals, the linear input range of the $\Delta\Sigma$ ADC can be extended to tens or hundreds of mV [42], [45], [51], [52], [54], [55]. This comes at the expense of substantially larger area and higher power compared to those designs with a small

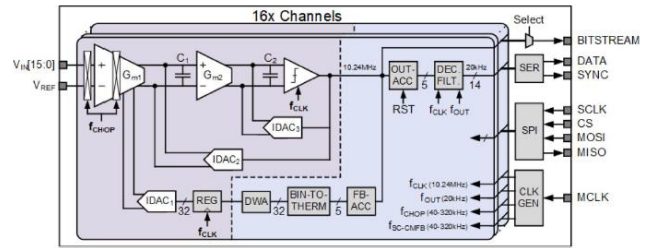


Fig. 13 High-level architecture of the 16-channel $\Delta\text{-}\Delta\Sigma$ neural readout reported in [28].

linear input range (typically around a few mV) mentioned above. While the power consumption can be reduced by employing high order modulators with reduced oversampling ratios, the power- and area-overhead of the backend decimation filters grow rapidly, which unfortunately are rarely mentioned and implemented in most designs. For this reason, the reported channel counts are typically very limited (one or a few). On the other hand, the large EDOs and stimulation artifacts can be compensated by the feedback loop in Δ modulators. Nevertheless, due to the limited tracking speed of the Δ modulation, this usually requires some recovery time for the ADC to settle after a stimulation event. Additionally, very large oversampling ratios are required in order to keep the quantization noise sufficiently low. As a result, these architectures have mostly been reported in low-bandwidth readouts used for electrocorticography (ECoG) [35], [36], [56], and cannot easily be applied to high-frequency AP recording.

To reduce the oversampling ratio while maintaining the tracking for artifacts and/or EDO compensation, $\Delta\text{-}\Delta\Sigma$ or $\Delta 2\Sigma$ topologies have been reported widely [37], [50], [53]. Good area and power efficiencies have already been achieved for several low-bandwidth designs [50], [53], while the number of high-bandwidth design is still limited. In [37], a high-bandwidth readout architecture has been proposed, which achieves a promising channel area of 0.0077 mm². In this example, a 16-channel readout IC was implemented, featuring a DC-coupled 2nd order $\Delta\text{-}\Delta\Sigma$ architecture as shown in Fig. 13. Combining $\Delta\text{-}\Delta\Sigma$ modulation with new bootstrapping and chopping schemes, this design achieves large dynamic range while maintaining high input impedance and low noise. However, the reported power efficiency is not sufficient for high-channel-count implementations. It is worth mentioning that while almost rail-to-rail artifact and/or EDO tolerance can be achieved when the feedback integrator is realized with a charge pump, such scheme is prone to saturation in the final output reconstruction step. This is because the digital accumulation in the backend reconstruction circuit does not match the leaky integration performed by the charge pump.

Finally, several mixed-signal techniques have also been proposed to reduce the transient recovery time after a stimulation event. In [53], adaptive step size (or digital auto-ranging) is utilized in the Δ -modulation path, achieving a recovery from >200 -mVpp artifacts within <1 ms. The tran-

sient recovery time can further be reduced by boosting the ADC sampling clock when an artifact is detected [56]. Recently, adaptive clock boosting combined with SAR-assisted artifact cancellation has been employed, resulting in a maximum recovery time of 20 μ s for ± 175 mV artifacts [49].

4. Future Outlooks

This paper aimed to provide an overview of current circuit design techniques for electrophysiology. The standard instrumentation amplifier architecture has evolved significantly in the past decades. Leveraging the power provided by modern CMOS technology, it has become possible to design highly integrated, ultra-low noise, ultra-low power and high channel count ICs. While this paper primarily focused on electrophysiology, the field has been evolving rapidly. Multi-modal sensing, where electrical recording is being combined with other modalities like movement, optical sensing, tissue impedance spectroscopy, or chemical sensing is actively being explored together with sensor fusion data algorithms to provide even more useful actionable information. As we are able to design ICs with ever more parallel recording capabilities, a new problem arises, namely the data bottleneck. As more and more data is being recorded, it becomes increasingly more challenging to offload all that data for analysis in a low-power fashion. In line with advancements in edge-AI, this field is also seeing an increased research effort in data analytics where sensor fusion, feature extraction and classification is being implemented directly in the recording ICs. This offers exciting new design challenges for the analog front-ends to maximally facilitate this on-the-node data processing. So, while this paper merely offers a brief introduction focusing on the analog front-end design, there are plenty of exciting research opportunities still ahead of us in this field.

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