

## PAPER

# A Study of Phase-Adjusting Architectures for Low-Phase-Noise Quadrature Voltage-Controlled Oscillators

Mamoru UGAJIN<sup>†a)</sup>, Member, Yuya KAKEI<sup>††</sup>, Nonmember, and Nobuyuki ITOH<sup>†††</sup>, Senior Member

**SUMMARY** Quadrature voltage-controlled oscillators (VCOs) with current-weight-average and voltage-weight-average phase-adjusting architectures are studied. The phase adjusting equalizes the oscillation frequency to the LC-resonant frequency. The merits of the equalization are explained by using Leeson's phase noise equation and the impulse sensitivity function (ISF). Quadrature VCOs with the phase-adjusting architectures are fabricated using 180-nm TSMC CMOS and show low-phase-noise performances compared to a conventional differential VCO. The ISF analysis and small-signal analysis also show that the drawbacks of the current-weight-average phase-adjusting and voltage-weight-average phase-adjusting architectures are current-source noise effect and large additional capacitance, respectively. A voltage-average-adjusting circuit with a source follower at its input alleviates the capacitance increase.

**key words:** *integrated circuit, phase noise, voltage-controlled oscillator, gate delay, phase-adjusting architecture, quadrature signal, impulse sensitivity function*

## 1. Introduction

High-bit-rate wireless communications demand high carrier frequencies [1], such as 24-GHz WLAN [2], IEEE802.11ad [3], and 24-29 GHz 5G mobile phones [4]. One of essential circuit blocks in the high-frequency wireless systems is a voltage-controlled oscillator (VCO). Various VCOs are investigated [5]–[9] for quadrature signal processing [10]–[17] in the high-performance wireless systems, however, a high-frequency VCO usually needs an exceptionally fine CMOS technology and/or a special high-Q inductor process [18]–[23] for suppressing the phase noise. Thus, their process cost could be considerably high. The high-cost fine CMOS technology reduces a transistor delay and then the VCO phase noise. Instead of using the high-cost process, we used a phase-adjusting architecture with a quadrature VCO for suppressing the delay-related phase noise [24]. The phase-adjusting architecture is composed of poly-phase VCO outputs, mitigates the transistor-delay influence, and can be implemented without process-cost increase.

This paper analyzes the relation between the

transistor delay and the VCO phase noise. Then two types of phase-adjusting architectures are evaluated using ac analysis, small-signal analysis, and measurement results. Both architectures are using weight-average phase adjusting but different in the phase-noise suppressing performances.

## 2. Relation between VCO Phase Noise and Gain-Cell Transistor Delay

Figure 1 shows the circuit structure and the ac-analysis results for a differential LC VCO. The open-half-loop gain and phase of a differential VCO (Fig. 1 (b)) were estimated using Spectre simulation. A dummy LC amplifier was added in the simulation for adding gate capacitances to an LC parallel resonant circuit. The phase-change rate, which is the derivative of the phase response ( $|\phi'(f)|$ ), was also calculated using the phase-frequency dependence (Fig. 1 (b)) as shown in Fig. 1 (c). The gain peak locates at the LC resonant frequency of 29.4 GHz, however, the oscillation occurs at 28.7 GHz because of oscillation condition ( $180^\circ$  phase delay). The difference between the LC resonant frequency and the oscillation frequency arises from an RC delay in a gain-cell transistor. The RC delay of  $\Delta t$  causes a phase delay of  $\Delta\phi$  ( $= 2\pi f\Delta t$ ), thus the gain-cell transistor changes a voltage input to a current output with a phase delay of  $(\pi + \Delta\phi)$ . At the oscillation frequency, the LC resonant circuit changes the current output to the voltage output with a phase lead of  $\Delta\phi$ . Therefore, the oscillation occurs at the inductive frequency region of the LC parallel resonant circuit and the oscillation frequency is lower than the LC resonant frequency.

The relationship between oscillation frequency and phase noise is well known as Leeson's phase noise equation [25], and is as follows:

$$L(\Delta f) = \frac{2kTF}{P_{osc}} \left\{ 1 + \left( \frac{1}{\phi'(f_{osc})\Delta f} \right)^2 \right\} \left( 1 + \frac{f_{1/f}}{\Delta f} \right) \quad (1)$$

where,  $f_{osc}$  is the oscillation frequency,  $\Delta f$  is the carrier offset frequency,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature,  $F$  is the noise factor of the gain cell, and  $f_{1/f}$  is the flicker noise corner frequency. And  $\phi'(f_{res}) = -2Q_{tank}/f_{res}$  where  $Q_{tank}$  is the Q factor of the tank circuit and  $f_{res}$  is the LC resonant frequency of the tank circuit. When the time delay of the gain cell is negligible compared to the LC resonant frequency,  $f_{res} \approx f_{osc}$  and  $Q_{tank}$  improvement is a main target for suppressing the VCO phase noise [26]. However, when the delay time is not sufficiently

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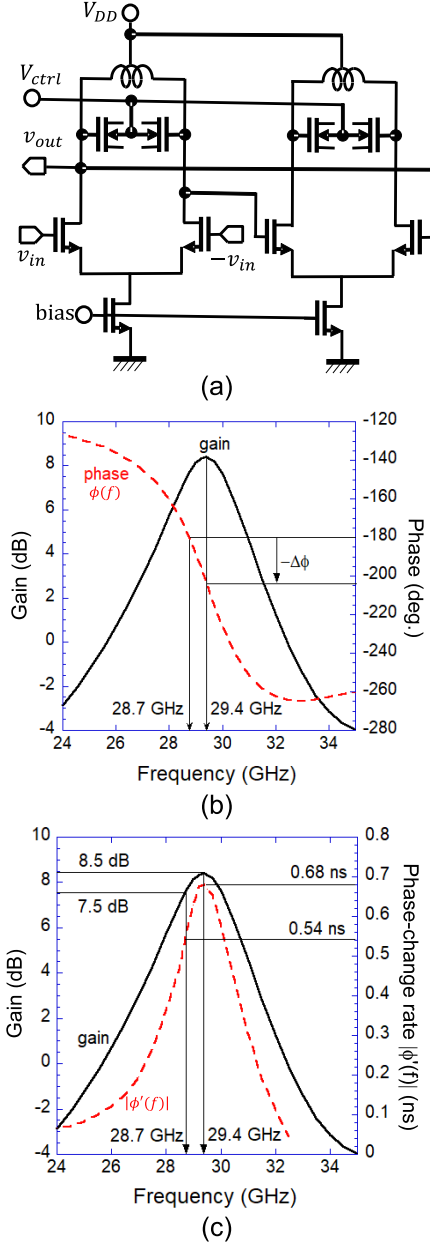
<sup>†</sup>The author is with Nippon Institute of Technology, Saitama ken, 345–8501 Japan.

<sup>††</sup>The author is with Saizeriya Co., Ltd., Yoshikawa-shi, 342–0008 Japan.

<sup>†††</sup>The author is with Okayama Prefectural University, Soja-shi, 719–1197 Japan.

a) E-mail: uga@nit.ac.jp

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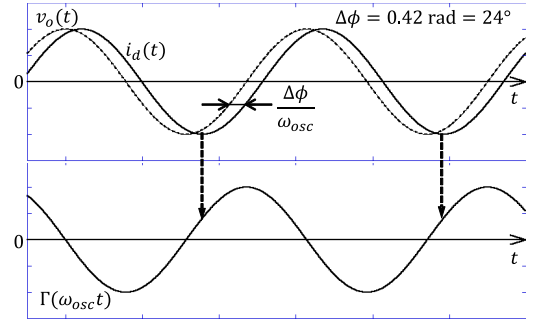


**Fig. 1** (a) The circuit structure, (b) the gain and phase and (c) the phase-change rate ( $|\phi'(f)|$ ) of open-half-loop ac analysis for a differential LC VCO.

small, the phase noise could be enlarged by the delay [24].

As shown in Fig. 1(c), the frequency difference between the oscillation frequency and the LC resonant frequency lowered the loop gain of VCO by about 1 dB, then the oscillation power ( $P_{osc}$ ) in Eq. (1) must be decreased. Equation (1) also predicts that the decrease of the phase-change rate ( $|\phi'(f)|$ ) could deteriorate the phase noise about 2 dB.

Figure 2 shows a typical shape of the impulse sensitivity function (ISF)  $\Gamma(\omega_{osc}t)$  for an LC oscillator [27].  $\Gamma(\omega_{osc}t)$  indicates the sensitivity of the oscillator to an impulse injected at phase  $\omega_{osc}t$ . Noise sensitivity has its maximum



**Fig. 2** Impulse sensitivity function for LC oscillator with  $24^\circ$  voltage-current phase delay.

value near the zero crossings of the oscillation, and a zero value at maxima of the oscillation waveform. The current-source noise is injected into the output nodes through gain-cell transistors, then the injected current-source noise has its maximum value when the drain current reaches its peak value (at the negative peak of  $i_d(t)$ ). The dotted arrows (shown in Fig. 2) indicate the timing when the current-source noise reaches its maximum. The phase difference between the output voltage of the VCO ( $v_o(t)$ ) and the drain current of gain-cell transistor ( $i_d(t)$ ) is  $\Delta\phi$ . If  $\Delta\phi$  is zero, the maximum current-source noise is injected at the zero-impulse-sensitivity timing. Therefore, when  $\Delta\phi$  is not zero, the maximum current-source noise is injected at the non-zero-impulse-sensitivity timing and VCO phase noise becomes worse.

### 3. Phase Adjusting Architectures and Performances

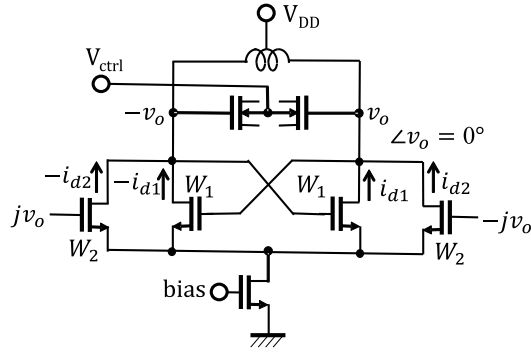
Phase adjusting architectures were designed and were fabricated to reduce the phase delay  $\Delta\phi$ , equalize the oscillation frequency to the LC resonant frequency, and were expected to suppress VCO phase noise. To evaluate the phase-adjusting-architecture performance, the inductors and the total width of the gain-cell transistors were same in all fabricated VCOs. The phase noises of the fabricated VCOs were measured with various bias voltages,  $V_{DD} = 2.2 \text{ V}$  and  $V_{ctrl} = 0 \text{ V}$ . The value of  $V_{DD}$  was selected to optimize the figure-of-merit (FOM) of the VCOs with source followers. The figure-of-merit (FOM) is defined as [28]:

$$FOM = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\text{mW}}\right). \quad (2)$$

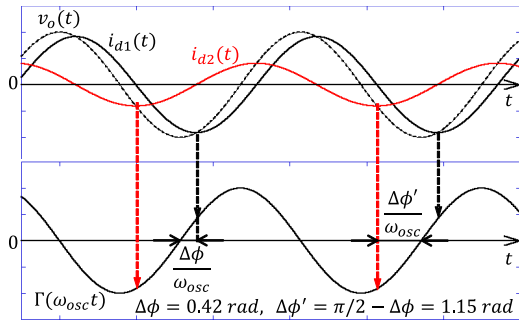
#### 3.1 Current-Weight-Average Phase-Adjusting Architecture

Figure 3 shows the concept of current-weight-average phase adjusting. The drain currents of gain-cell transistors are controlled by differential output voltages ( $0^\circ$  and  $180^\circ$ ) and  $90^\circ$ -advanced differential output voltages ( $90^\circ$  and  $270^\circ$ ). By optimizing the transistor-size ratio  $W_2/W_1$ , the phase angle of total current is adjusted as

$$\angle i_{d1} = -\Delta\phi$$



**Fig. 3** Concept of current-weight-average phase adjusting.



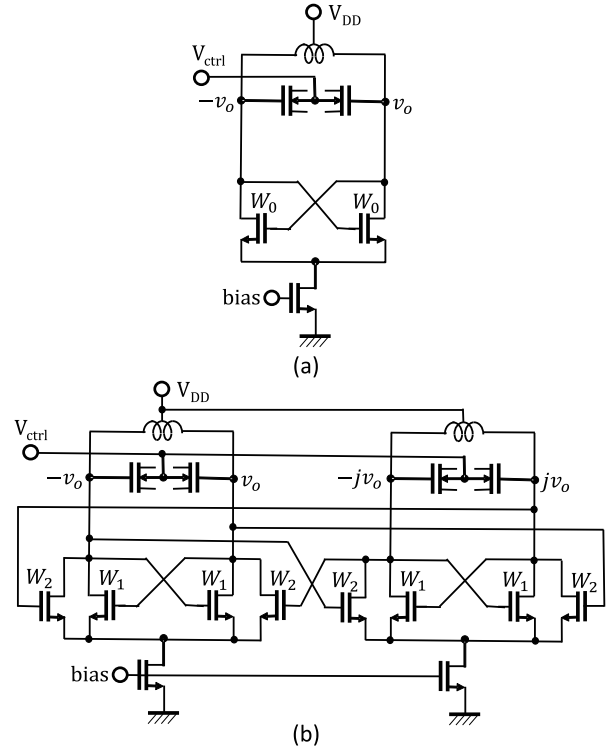
**Fig. 4** Impulse sensitivity function for LC oscillator with a current-weight-average phase-adjusting architecture.

$$\begin{aligned} \angle i_{d2} &= 90^\circ - \Delta\phi \\ \angle(i_{d1} + i_{d2}) &= 0^\circ. \end{aligned}$$

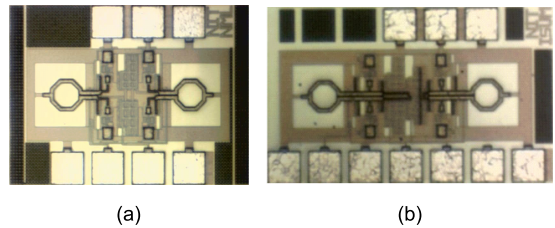
There is neither area penalty nor power penalty in this architecture. However, the noise from the current source could worsen the VCO phase noise because there are large phase differences between the drain currents and the output voltage ( $\Delta\phi$  and  $\pi/2 - \Delta\phi$ ) as shown in Fig. 4.

The conventional differential VCO [29]–[32] and the current-weight-average phase-adjusted quadrature VCO were fabricated using TSMC 180-nm CMOS technology (as shown in Figs. 5 and 6). There are two differential VCOs on a chip in Fig. 6(a). The value of  $W_0$  for the conventional VCOs was  $5 \mu\text{m} \times 10$ . The ratio of  $W_2/W_1$  was optimized using Spectre simulations for low phase noise. To verify the current-weight-average phase-adjusting effect, the simulations were done on the condition of  $W_0 = W_1 + W_2$ . And the values of  $W_1$  and  $W_2$  for the quadrature VCO were  $5 \mu\text{m} \times 8$  and  $5 \mu\text{m} \times 2$ , respectively.

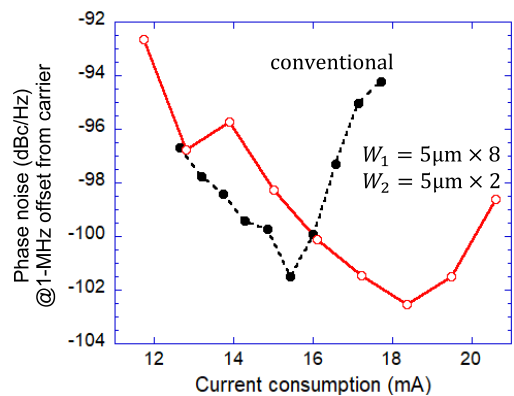
Figure 7 shows the measured results of the relation between phase noise at 1-MHz offset frequency and current consumption. The current consumption shows the current of the one conventional differential VCO and that of the quadrature VCO. The current of the quadrature VCO was about 2 times larger than that of the conventional differential VCO. This means that the current-weight-average phase-adjusting architecture needs no extra power consumption than that of a quadrature VCO without phase adjusting. Oscillation frequencies were 28.05 GHz for the



**Fig. 5** Circuit architectures of (a) a conventional differential VCO and (b) a quadrature VCO using a current-weight-average phase-adjusting architecture.



**Fig. 6** Chip microphotographs of (a) two conventional differential VCOs and (b) a quadrature VCO with a current-weight-average phase-adjusting architecture.



**Fig. 7** Relation between phase noise and current consumption for a conventional differential VCO and a quadrature VCO with a current-weight-average phase-adjusting architecture. Phase noise was measured at 1-MHz offset frequency from the carrier frequency.

conventional VCO and 26.56 GHz for the quadrature VCO. When the current consumption increases, both the output-voltage amplitude and the current-source noise increase. In the small-current region, the voltage-amplitude gain overwhelms the current-noise increase, then the VCO phase noise decreases. However, in the large-current region, the non-linear response of the gain-cell transistor saturates the voltage amplitude, and then the phase noise increases. The minimum phase noises in Fig.7 are  $-101.5$  dBc/Hz and  $-102.6$  dBc/Hz for the conventional VCO and the quadrature VCO, respectively. The phase-noise difference is only 1 dB because of the trade-off between the phase-adjusted effect and the current-source noise impact. The phase-adjusted effect was expected to reduce the phase noise more than 2 dB as explained with Eq. (1). However, the impulse sensitivity of the current-source noise with  $i_{d2}(t)$  is stronger than that with  $i_{d1}(t)$  as shown in Fig. 4. Therefore, the total impulse sensitivity of current-source noise becomes worse.

### 3.2 Voltage-Weight-Average Phase-Adjusting Architecture

The main drawback of the current-weight-average phase adjusting is the phase difference between the output voltage and the drain currents as shown in Fig.4. Therefore the  $\Delta\phi$ -phase shifters at two gate inputs of a differential VCO (depicted in Fig. 8(a)) are thought to be extremely helpful to adjust phase delay and suppress phase noise. The  $\Delta\phi$ -phase shifter was designed using a weight-average architecture with two capacitors as shown in Fig. 8(b). Phase adjusting at the input of the gain-cell transistor is expected to reduce the phase difference and the current-source noise effect as shown in Fig. 9.

Using small signal analysis, three currents in Fig. 8(b) are expressed as

$$\begin{aligned} i_1 &= j\omega_{osc}C_1(v_o - v_g) \\ i_2 &= j\omega_{osc}C_2(jv_o - v_g) \\ i_3 &= j\omega_{osc}C_g v_g \\ i_1 + i_2 &= i_3 \end{aligned}$$

Thus, the gate voltage  $v_g$  is expressed by using  $v_o$  as

$$v_g = \frac{C_1 + jC_2}{C_1 + C_2 + C_g} v_o \quad (3)$$

and

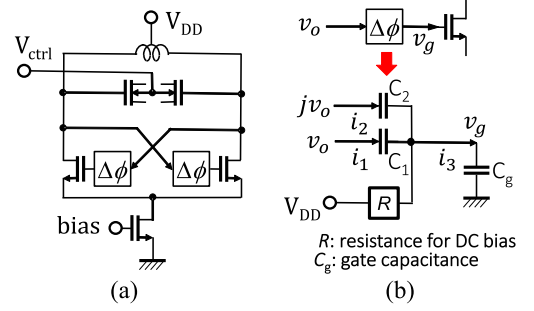
$$\frac{|v_g|}{|v_o|} = \frac{\sqrt{C_1^2 + C_2^2}}{C_1 + C_2 + C_g}. \quad (4)$$

Then

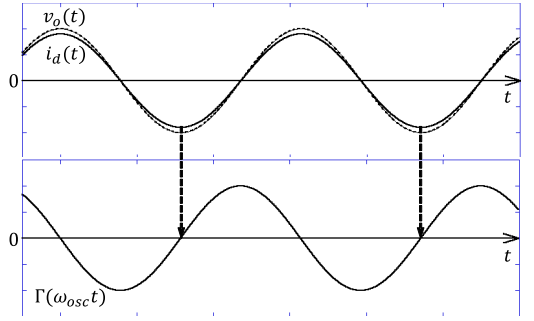
$$i_1 = j\omega_{osc} \frac{C_1(C_2 + C_g)}{C_1 + C_2 + C_g} v_o + \frac{\omega_{osc}C_1C_2}{C_1 + C_2 + C_g} v_o \quad (5)$$

and

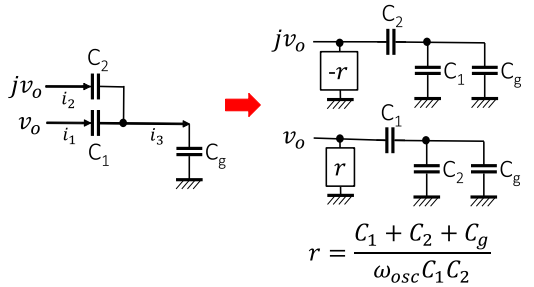
$$i_2 = j\omega_{osc} \frac{C_2(C_1 + C_g)}{C_1 + C_2 + C_g} jv_o - \frac{\omega_{osc}C_1C_2}{C_1 + C_2 + C_g} jv_o. \quad (6)$$



**Fig. 8** (a) A differential VCO with two phase shifters and (b) A phase-shifter circuit using a weight-average architecture with two capacitors.  $R$  is a resistance for DC bias.

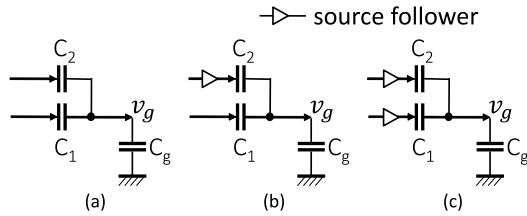


**Fig. 9** Impulse sensitivity function for LC oscillator with a voltage-weight-average phase adjusting architecture.

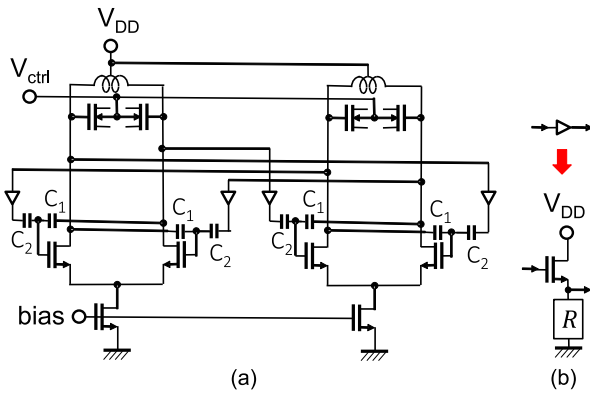


**Fig. 10** Equivalent capacitor connection to VCO outputs.

Equations (5) and (6) mean that additional capacitances connected to the VCO output are seemed to be increased considerably as shown in Fig. 10. Small values of  $C_1$  and  $C_2$  could reduce the additional capacitances but decrease the loop gain as shown in Eq.(4). Then three types of phase-shifter circuits depicted in Fig. 11 were evaluated using simulations and measurements. Type-(b) and -(c) phase shifters use source-follower circuits at their inputs. The source follower changes the additional capacitance to the source-follower gate capacitance. However, Type-(c) phase shifter could not produce a VCO oscillation even in the simulation because it decreases the amplitude of the signal flowing through the source follower and a loop gain. Type-(a) phase shifter was expected to lower phase noise in the simulation, but it could not produce VCO oscillation in the measurement. The cause of the inoperability is still under consid-



**Fig. 11** Three types of voltage-weight-average phase-shifter circuits. (a) Basic phase shifter consisted by two capacitors and (b) one source follower is added to the  $90^\circ$  input of basic shifter, (c) two source followers are added to the  $0^\circ$  and  $90^\circ$  inputs of basic shifter.

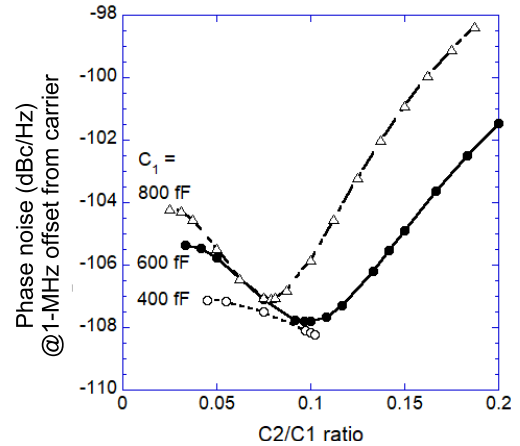


**Fig. 12** Circuit architecture of (a) a voltage-weight-average phase-adjusted quadrature VCO using four phase adjusters formed by 8 capacitors and 4 source followers and (b) a source follower.

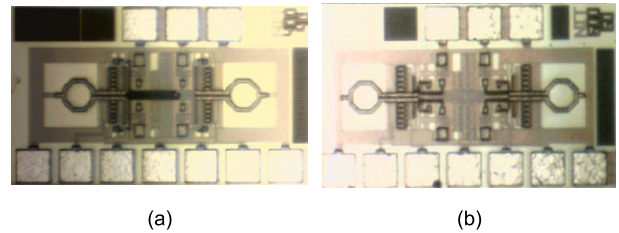
eration. Finally, only Type-(b) phase shifter could produce VCO oscillation.

Figure 12 shows a quadrature VCO circuit using the voltage-weight-average phase-adjusting architecture. Four  $\Delta\phi$ -phase shifters are added to two conventional differential VCOs. The optimum value of  $C_2/C_1$  ratio is determined by many effects such as the phase-adjusting effect, signal loss (as expressed as Eq. (4)), and additional resistances and capacitances (as shown in Fig. 10). Therefore, the optimum  $C_2/C_1$  ratio for the voltage-weight-average phase-adjusted VCOs was estimated using Spectre simulations (as shown in Fig. 13) with  $V_{DD} = 2.2$  V and  $V_{ctrl} = 0$  V. The current-source bias voltage was optimized for low phase noise. The optimum ratio of  $C_2/C_1$  was about 0.1 for VCOs with  $C_1$  of 400 fF and 600 fF. However, no oscillation was obtained when the ratio of  $C_2/C_1$  was larger than 0.11 with  $C_1$  of 400 fF due to loop-gain shortage. Then two phase-adjusted quadrature VCOs were fabricated using TSMC 180-nm CMOS technology (as shown in Fig. 14). The values of  $C_1$  and  $C_2$  of the  $\Delta\phi$ -phase shifters were 400 fF and 40 fF for chip (a), and 600 fF and 60 fF for chip (b), respectively.

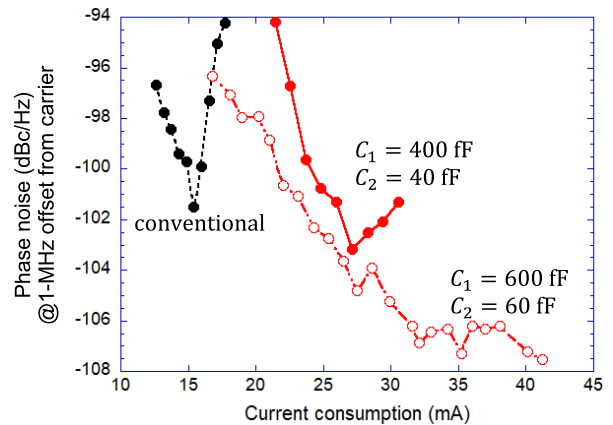
The phase noises of the quadrature VCOs were measured with various bias voltages,  $V_{DD} = 2.2$  V and  $V_{ctrl} = 0$  V. The VCO test chip was measured using an EXA series signal analyzer by Keysight Technologies Inc. with an on-wafer probe station. Figure 15 shows the relation between phase noise at 1-MHz offset frequency and current



**Fig. 13** Simulated phase-noise performances of voltage-weight-average phase-adjusted quadrature VCOs with  $V_{DD} = 2.2$  V and  $V_{ctrl} = 0$  V. The current-source bias voltage was optimized for low phase noise.



**Fig. 14** Chip microphotographs of voltage-weight-average phase-adjusted quadrature VCOs with (a)  $C_1 = 400$  fF,  $C_2 = 40$  fF and (b)  $C_1 = 600$  fF,  $C_2 = 60$  fF.



**Fig. 15** Relation between phase noise and current consumption for a conventional differential VCO and two quadrature VCOs with a voltage-weight-average phase-adjusting architecture. Phase noise was measured at 1-MHz offset frequency from the carrier frequency.

consumption. The current consumption shows the currents of the phase-adjusted quadrature VCOs with four source followers. In terms of bias setting, the quadrature VCO with  $C_1 = 600$  fF,  $C_2 = 60$  fF has a larger operation range than those of a conventional VCO and the quadrature VCO with  $C_1 = 400$  fF,  $C_2 = 40$  fF. The phase-adjusting architecture reduces the phase noise and is supposed to expand the op-



eration range, however, the loop-gain reduction (shown in Eq. (4)) in the quadrature VCO with  $C_1 = 400$  fF,  $C_2 = 40$  fF probably disturbed the operation-range expansion. Simulations predicted that further phase-noise improvement could not be expected with larger values of  $C_1$  and  $C_2$  as shown in Fig. 13. Oscillation frequencies were 26.59 GHz for the quadrature VCO with  $C_1 = 400$  fF,  $C_2 = 40$  fF, and 25.17 GHz for the quadrature VCO with  $C_1 = 600$  fF,  $C_2 = 60$  fF. As mentioned, the  $\Delta\phi$ -phase shifter worked not only as a phase shifter but also as an additional capacitor and hence both the LC-resonant frequency and the oscillation frequency of the phase-adjusting quadrature VCO were lowered.

The ranges of oscillation frequencies were 28.05 to 28.73 GHz for the conventional VCO and 25.17 to 25.73 GHz for the quadrature VCO with  $C_1 = 600$  fF,  $C_2 = 60$  fF when  $V_{ctrl}$  was changed from 0 to 2.2 V. Thus, the tuning ranges were 2.4 % and 2.2 % for the conventional VCO and the quadrature VCO, respectively. This means that the additional capacitance of the  $\Delta\phi$ -phase shifter reduced the frequency range by about 10 %. The frequency tuning ranges of the fabricated VCOs were narrow because the DC level of the varactor gate was always approximately  $V_{DD}$ , thus the capacitance variable range was small. Moreover, the parasitic capacitance of cross-coupled NMOS was relatively large.

Figure 16 shows the offset-frequency dependence of phase noise at the conditions of minimum phase noise in Fig. 15. In Fig. 16, the current consumptions of the conventional VCO and the phase-adjusted quadrature VCO with  $C_1 = 600$  fF,  $C_2 = 60$  fF were 15.4 mA and 41.2 mA, respectively. Integrated phase noises (from 100 kHz to 1 MHz) were  $-26.4$  dBc for the conventional VCO and  $-34.0$  dBc for the phase-adjusted quadrature VCO with  $C_1 = 600$  fF and  $C_2 = 60$  fF. The phase-adjusting architecture suppresses phase noise about 9 dB and 6 dB at 100-kHz and 1-MHz offset frequencies, respectively. The 3-dB reduction of phase-noise suppression at 1-MHz offset

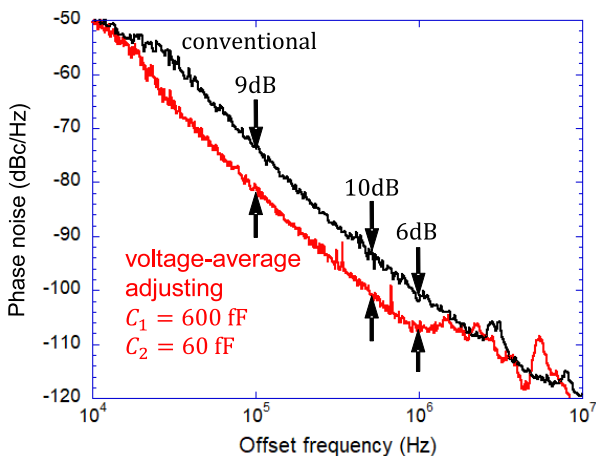


Fig. 16 Measured phase noise as a function of the offset frequency from the carrier frequency.

frequency was probably due to measurement instability as shown in Fig. 16. The reason for the instability is under investigation.

#### 4. Performance Summary and Discussion

The best FOMs of the VCOs in Fig. 7 and Fig. 15 were evaluated as  $-175.1$  dBc/Hz,  $-175.0$  dBc/Hz,  $-173.5$  dBc/Hz and  $-176.4$  dBc/Hz for the conventional VCO, the current-phase-adjusted quadrature VCO, the voltage-phase-adjusted quadrature VCOs with  $C_1 = 400$  fF,  $C_2 = 40$  fF and with  $C_1 = 600$  fF,  $C_2 = 60$  fF, respectively.

Performance summary of the phase-adjusted quadrature VCOs is illustrated in Table 1. A quadrature VCO usually consumes two times larger current than that of a differential VCO, so the FOM improvements compared to the conventional differential VCO are effectively 2.9 dB, 1.4 dB and 4.3 dB for current-phase-adjusted VCO, voltage-phase-adjusted VCOs with  $C_1 = 400$  fF,  $C_2 = 40$  fF and  $C_1 = 600$  fF,  $C_2 = 60$  fF, respectively. The voltage-phase-adjusted VCOs could reduce phase noise by 6 dB with the sacrifice of the source-follower-power increase, and hence the improvement of FOM value is only 1 dB.

Performance comparison with recently published CMOS LC VCOs is illustrated in Table 2. All VCOs are quadrature VCOs. The proposed VCO shows phase-noise performances comparable to the finer-process VCOs. The FOM value of Ref. [33] is better than that of our VCO. There are two reasons for the better FOM value. The first reason is because the VCO of Ref. [33] operated at 10 GHz and produced 20-GHz outputs using a frequency doubler. Therefore, the VCO of Ref. [33] had little delay-

Table 1 Performance summary

	Conv.	Current adjusted	$C_1 = 400$ fF $C_2 = 40$ fF	$C_1 = 600$ fF $C_2 = 60$ fF
$f_{osc}$ (GHz)	28.05	26.56	26.59	25.17
$P_{DC}$ (mW)	33.9	40.4	59.6	90.6
PN @ 1MHz (dBc/Hz)	-101.5	-102.6	-102.8	-107.5
FOM (dBc/Hz)	-175.1	-175.0	-173.5	-176.4

Table 2 Performance comparison

Ref	$C_1 = 600$ fF $C_2 = 60$ fF	[33]	[34]	[35]	[36]
process (nm)	180	180	130	65	65
$f_{osc}$ (GHz)	25.17	19.85	20.17	20.88	26
T.R. (%)	2.2	10.4	-	17.9	14.4
$V_{DD}$ (V)	2.2	1.8	1.2	1.2	-
$P_{DC}$ (mW)	90.6	40.3	28.8	80.0	11.8
chip area ( $\mu\text{m}^2$ )	600 $\times 220$	1280 $\times 760$	650 $\times 400$	1100 $\times 1000$	280 $\times 84$
PN@1MHz (dBc/Hz)	-107.5	-111.5	-102.4	-100	-100
FOM (dBc/Hz)	-176.4	-181.4	-173.9	-173.4	-177.6

related noise degradation. The second reason is because the source-follower circuit in our VCO was not optimized. It consumed large electric power.

## 5. Conclusion

Quadrature VCOs with current-weight-average and voltage-weight-average phase-adjusting architectures were studied. The merits of the oscillation frequency equalization to the LC-resonant frequency were explained by using Leeson's phase noise equation and the impulse sensitivity function (ISF). Quadrature VCOs with the phase-adjusting architectures were fabricated using 180-nm TSMC CMOS and showed low-phase-noise performances compared to a conventional differential VCO. The ISF analysis and small-signal analysis showed that the drawbacks of the current-weight-average phase-adjusting and voltage-weight-average phase-adjusting architectures were the current-source noise effect and the large additional capacitance, respectively. A voltage-average-adjusting circuit with a source follower at its input alleviated the capacitance increase.

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**Mamoru Ugajin** received the B.S., M.S., and Ph.D. degrees in applied physics from the University of Tokyo, Japan, in 1983, 1985 and 1996, respectively. In 1985, he joined Nippon Telegraph and Telephone Corporation (NTT). From 1985 to 1997, he worked on silicon-BJT and SiGe-HBT device technologies for high-speed digital applications at NTT LSI Laboratories, Atsugi. During 1992–1993, he was a visiting researcher at the University of Florida, Gainesville, where he worked on modeling and analysis of SiGe HBTs. From 1999 to 2012, he was engaged in circuit design for CMOS wireless transceiver ICs. From 2012, he is a Professor at Nippon Institute of Technology, where he is working on analog integrated circuit designs. He served as a Program Committee Member of the Symposium on VLSI Circuits, an Associate Editor of the *IEICE Transactions on Electronics*, and an Editor of the *IEICE Electronics Express*. He is a member of IEEE.



**Yuya Kakei** received the B. Eng. and M. Eng. degrees in Electrical Engineering from Nippon Institute of Technology, Saitama, Japan in 2019 and 2021, respectively. In 2021, He joined Saizeriya Co., Ltd.



**Nobuyuki Itoh** received the B.S. and M.S. degrees in chemistry from Tokyo University of Science, Tokyo, Japan, in 1983 and 1985, respectively, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006. In 1985, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of CMOS device technologies, bipolar device technologies, bipolar circuit design and RFCMOS circuit design. He had been a Visiting Scientist at Katholieke Universiteit Leuven, ESAT-MICAS, Leuven, Belgium, from 1996 to 1998, where he had worked on design of fully integrated VCOs and PLLs using RFCMOS. He has been engaged in the research and development of high-frequency analog circuit at Semiconductor Company of Toshiba Corporation since 1998. He was also a part-time lecturer of Chuo University, Tokyo, Japan, since 2009. Since 2010, he has been full time professor of Okayama Prefectural University. His current research interests are high-frequency integrated circuit for telecommunications. Dr. Itoh is a member of IEEE and also senior member of IEICE. He received the Asia-Pacific Microwave Conference (APMC) Prize in 2007. He has been a member of TPC of CICC, BCTM, ESSCIRC, TJMW, and RFIC symposium, was a secretary of URSI-C Japan Committee.