PAPER

A 28GHz High-Accuracy Phase and Amplitude Detection Circuit for Dual-Polarized Phased-Array Calibration

Yudai YAMAZAKI[†a)], **Joshua ALVIN**[†], **Jian PANG**[†], *Nonmembers*, **Atsushi SHIRANE**[†], *Member*, *and* **Kenichi OKADA**[†], *Senior Member*

SUMMARY This article presents a 28GHz high-accuracy phase and amplitude detection circuit for dual-polarized phased-array calibration. With dual-polarized calibration scheme, external LO signal is not required for calibration. The proposed detection circuit detects phase and amplitude independently, using PDC and ADC. By utilizing a 28GHz-to-140kHz downconversion scheme, the phase and amplitude are detected more accurately. In addition, reference signal for PDC and ADC is generated from 28GHz LO signal with divide-by-6 dual-step-mixing injection locked frequency divider (ILFD). This ILFD achieves 24.5-32.5GHz (28%) locking range with only 3.0mW power consumption and 0.01mm^2 area. In the measurement, the detection circuit achieves phase and amplitude detections with RMS errors of 0.17degree and 0.12dB, respectively. The total power consumption of the proposed circuit is 59mW with 1-V supply voltage.

key words: *5G, dual-polarized phased-array, calibration, detection circuit, millimeter-wave, divide-by-6 ILFD*

1. Introduction

In recent years, the amount of data traffic has been increasing exponentially. Such increase in overall traffic not only come from the growing data traffic per device, but also from the rise in the total number of connected devices. It is expected that, in near future this ever-increasing demand for higher data rate cannot be fulfilled using only lower frequency bands, which are already very crowded. To address this problem, spectrum resources at millimeter-wave frequency band is needed because of the possibility of wideband communication. In 5G new radio (NR), millimeter-wave frequency allows more devices to achieve high-data traffics.

Millimeter-wave frequency signal has huge path loss, which heavily limits its coverage. To address the coverage problem, the beamforming technique with phased-array transciever is necessary. In millimeter-wave applications, the phased-array transceiver can compensate the huge path loss with multiple-anntena output and phase shifting [1]–[7]. In addition, dual-polarized phased-array transceivers will also be employed in 5G NR for more high-data-rate communication [8]–[11]. However, on-chip implementation of such transceivers is sensitive to the mismatch caused by the PVT variations. The mismatch between each element will introduce phase and amplitude errors, which degrade the performance of the transceiver, as shown in Fig. 1. This mismatch needs to be calibrated to minimize the phase and amplitude error and restore the performance of the phased-array beamforming. For realizing the calibration system of phased-array transceiver, a detection circuit is needed. Conventionally, the detection circuit using I/Q modulation is applied for calibration [12]–[14]. Such detection circuits achieves low-power detection with small area. However, the I/Q output suffers from large mismatch due to the I/Q generation circuits. So, the I/Q detection technique is not good at phased-array calibrations.

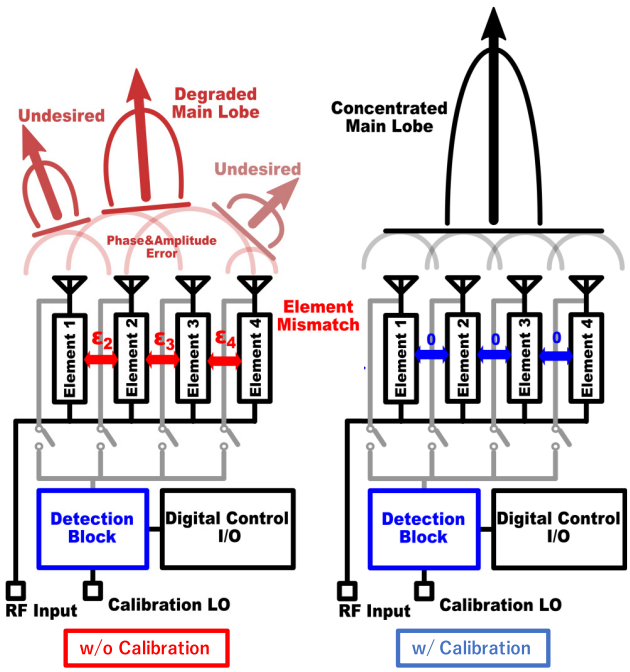

Fig. 1 Calibration for phased-array beamforming

This work introduces the detection circuit based on PDC (Phase-to-Digital Converter) and ADC (Analog-to-Digital Converter) for dual-poralizsed phased-array transceivers. This proposed circuit achieves high-accuracy phase and amplitude detections in 28GHz phased-array calibration. The 28GHz input signal is downconverted to around 140kHz. After that the downconverted signal is sent to the ADC and PDC. For the operations of ADC and PDC, 600MHz reference signal is generated from 28GHz LO signal using divide-by-6 dual-step-mixing injection locked fre-

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[†]The authors are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, 152–8552 Japan.
a) E-mail: yamazaki@ssc.pe.titech.ac.jp
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quency fivider (ILFD). In the measurement, the proposed detection circuit achieves phase and amplitude detections with RMS phase error of 0.17 degree and RMS gain error of 0.12dB, respectively, in 59mW power consumption.

This paper is structured as follow. The high-accuracy dual-polarized phased-array calibration system using proposed detection circuit is discussed in Sect. 2. The proposed phase and amplitude detection circuit is explained in detail in Sect. 3. Section 4 demonstrates the measurement result for the proposed detection circuit. Finally, this work is concluded in Sect. 5.

2. Proposed Calibration Scheme

As mentioned in Sect. 1, phased-array transcievers have mismatch between each element due to PVT variations. The beam performance of the transceiver is thus degraded. Figure 2 shows the results of beamforming simulations using MATLAB. The simulation is performed at a frequency of 28GHz with 8 array elements and an array spacing of $\lambda/2$. The beam-pattern degradation is checked after applying Gaussian errors on the amplitude and phase values of each element output. The black line is the ideal beam pattern, which has no mismatch in each element. On the other hand, the gray line shows the non-ideal beam pattern with random errors. With RMS gain and phase errors of 5.0dB and 2.0degree, as shown in Fig. 2 (a), the beam pattern is degraded compared to an ideal pattern. After the errors is suppressed to 0.5dB and 0.5degree, as shown in Fig. 2 (b), the beam pattern is restored.

To suppress the degradation of beam pattern, the mismatch has to be calibrated by the phase and amplitude detection circuit. Figure 3 shows the proposed dual-polarized phased-array calibration scheme with detection circuit. In dual-polarized phased-array transceivers, there are V and H input ports. The H/V input ports are reused for calibration in this work, which ensures a simplified packaging. When the phase and amplitude errors of V1 element are detected, 28GHz+140kHz detection signal is input from V-IN port, and 28GHz calibration LO signal is input from H-IN port. In this case, only the path of V1 element is turned on. The output signal of V1 element will be sent to the detection circuit through the calibration path. The detection signal is downconverted to 140kHz signal by mixed with 28GHz LO signal. This downconversion scheme makes phase and amplitude information of the RF detection signal converted into the baseband (BB) signal, which can be quantified easily by the digital circuits. This signal is then sent to the ADC for amplitude detection, and to the limited amplifier (LA)-PDC chain for phase detection. The calibration of V1 element is then performed based on the detected digital values. Similarly, the phase and amplitude detection is also performed for V2, H1 and H2 in Fig. 3.

3. Architecture Implementation

Figure 4 shows the block diagram of the calibration circuit, which consists of three parts: RF signal detection part, reference signal generation part, and digital circuits part (ADC and PDC). First, the RF signal detection part is introduced. In the proposed circuit, the phase and am-

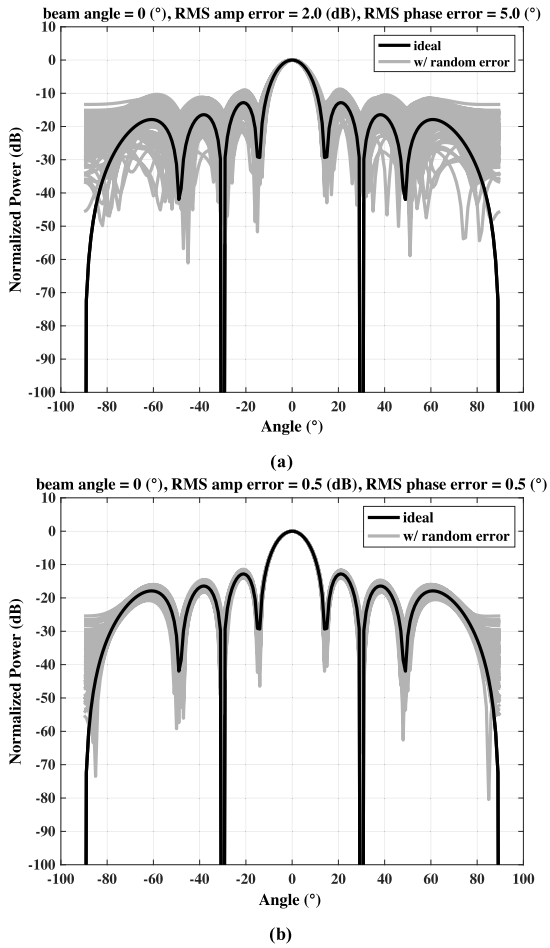

Fig. 2 Simulated phased array beampattern in MATLAB (a) with RMS gain error 2.0dB, RMS phase error 5.0degree (b) with RMS gain error 0.5dB, RMS phase error 0.5degree

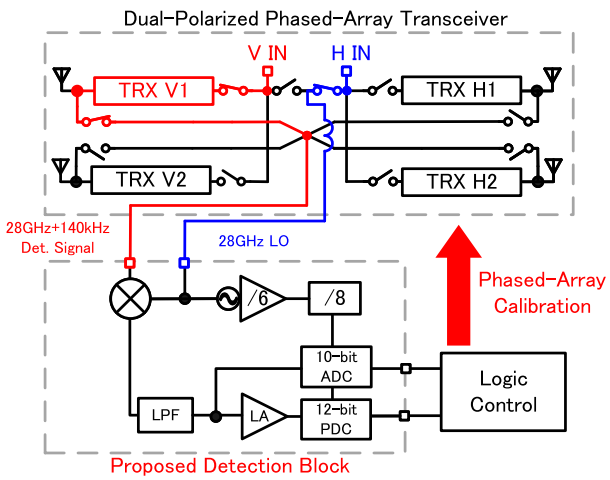

Fig. 3 Proposed dual-polarized phased-array calibration scheme

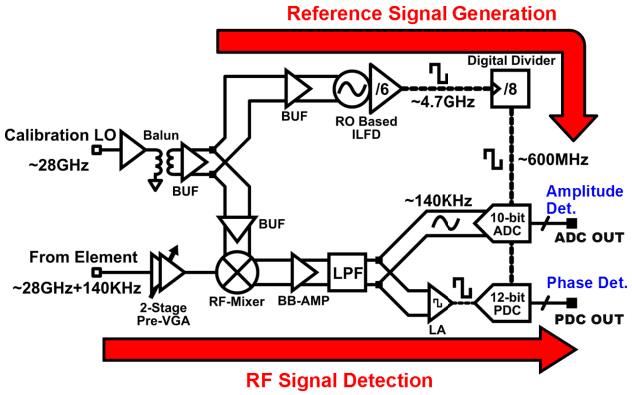

Fig. 4 Proposed 28GHz phase and amplitude detection circuit

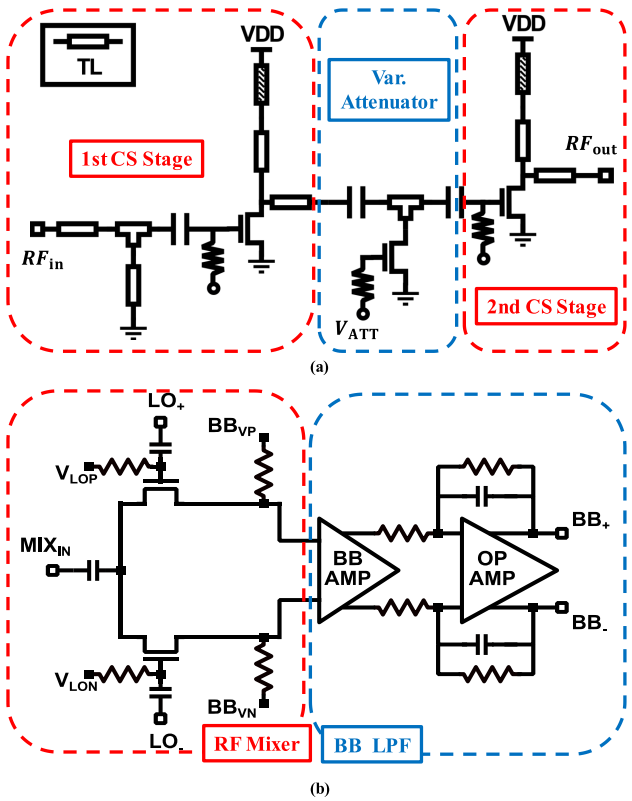

Fig. 5 The schematic of (a) 2-stages RF preamp and (b) downconversion circuit chain

plitude detection of around 28GHz+140kHz signal are realized by 2-stage RF-preamp and downconversion circuit chain. The schematic of the 2-stage RF-preamp is shown in Fig. 5 (a). The preamp consists of two common-source amplifier and an attenuator. It consists of transmission lines for impedance matching at each stage. The preamp is designed to suppress the degradation of AM-PM characteristic within a wide dynamic range. The signal is then sent into the downconversion circuit chain, which is shown in Fig. 5 (b). 28GHz+140kHz signal is downconverted to low frequency signal around 140KHz. This downconversion is realized using RF double-balanced mixer and 28GHz calibration LO signal. The mixer output is connected directly to the low

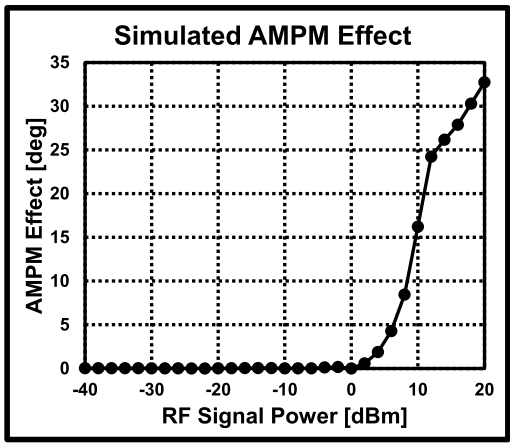

Fig. 6 The simulated AM-PM characteristic from 28GHz+140kHz input to 140kHz LPF output

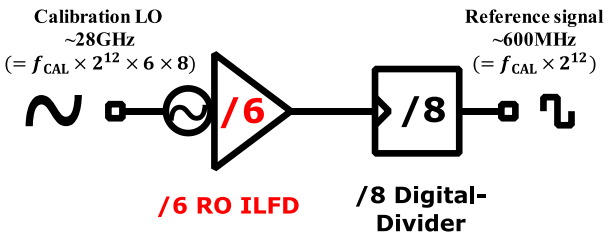

Fig. 7 Proposed divider chain to generate 600MHz reference signal from 28GHz LO signal

pass filter to extract only the signal with target frequency. In the mixer, the voltage BBVP and BBVN can be tuned to eliminate DC offsets and maximize the dynamic range of the detection circuit. In this process, phase and amplitude information of RF signal (28GHz+140kHz) is converted to low frequency (140KHz) signal without degrading AM-PM characteristic. Figure 6 shows the AM-PM characteristic from 28GHz+140kHz input to 140kHz LPF output. In the dynamic range from −40 to 0dBm, the AM-PM characteristic is suppressed to less than 0.12degree. The LPF output signal can be quantized accurately by the ADC and PDC.

Next, the reference signal generation part is explained. To realize the phase detection, reference signal PDC is generated internally from 28GHz calibration LO signal. In the proposed circuit, frequency divider chain shown in Fig. 7 is utilized for the reference signal generation. The divider chain consists of divide-by-6 injection locked frequency divider (ILFD) and divide-by-8 digital frequency divider. Usually, only digital dividers are used at a few GHz frequency. However, at much higher frequency such as millimeter-wave, high-division-ratio analog dividers are also used [15]–[21]. Calibration LO signal around 28GHz is first divided by 6 to a signal near 4.7GHz using ILFD. After that, the 4.7GHz signal is divided by 8 to generate around 600MHz signal with logic-baced digital divider. Using this frequency generation scheme, the RF input and calibration LO frequencies are given as follow. f_{CAL} is the frequency of the calibration signal, which is around 140KHz.

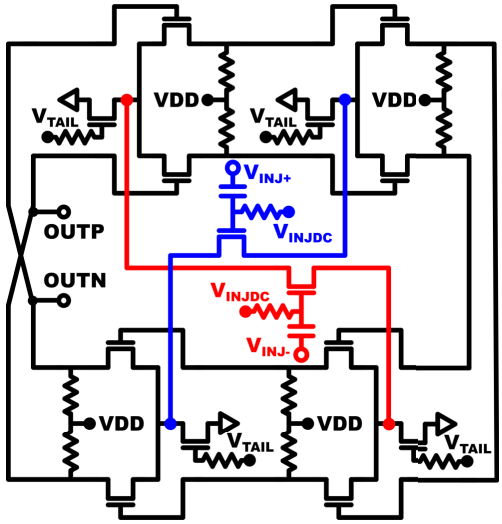

Fig. 8 The schematic of divide-by-6 dual-step-mixing ILFD

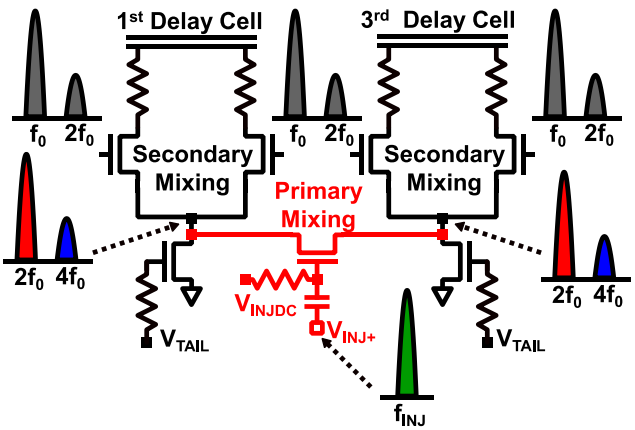

Fig. 9 The dual-step-mixing approach of divide-by-6 ILFD

$$f_{\mathrm{LO}} = (2^{12} \times 6 \times 8) \times f_{\mathrm{CAL}} \quad (1)$$

$$f_{\mathrm{RF}} = (2^{12} \times 6 \times 8 + 1) \times f_{\mathrm{CAL}} \quad (2)$$

The circuit schematic of 28GHz divide-by-6 ILFD is shown in Fig. 8. The ILFD is based on a 4-stage ring oscillator with injection mixers connecting the common nodes of even and odd stages, respectively. This ILFD topology is dual-step-mixing approach. It is chosen because it shows good tradeoff between locking range, power consumption and area, while requiring less headroom than other topologies. Figure 9 shows the dual-step-mixing approach of ILFD. When no injection signal is presented, the ILFD oscillates at free-run frequency of 4.7GHz. To realize divide-by-6 operation, the injection signal around 6 times of the free-running frequency is input to the gates of the injection mixers. During the operation, this injection signal is mixed with even harmonics of the common nodes by the injection mixers. Then, the resulting mixing products are mixed further with the fundamental signal at the transistors of the delay cells. Such dual-step-mixing approach achieves wider locking range in divide-by-6 operation with only one oscillator.

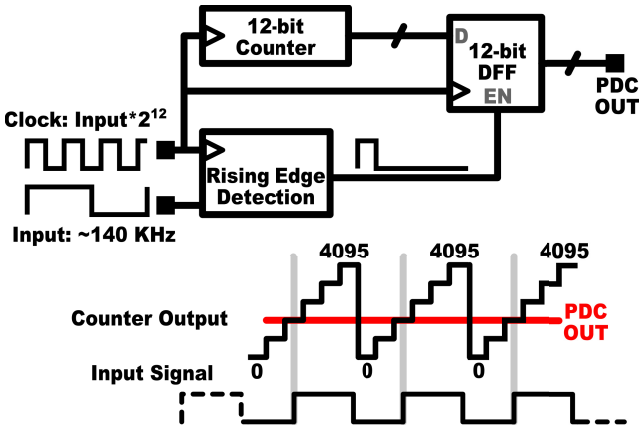

Fig. 10 The system of PDC (phase-to-digital converter)

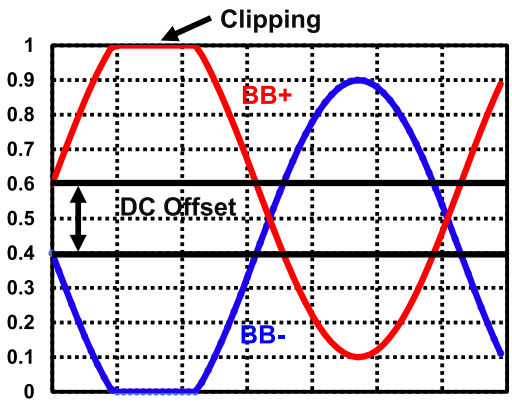

Fig. 11 DC offset of ADC input signal

Finally, the operations of PDC and ADC are explained. The phase detection is realized by LA-PDC chain. To realize the phase detection, the BB_{OUT} signal is first transformed to square wave with LA. The square wave signal is then sent into the PDC for phase detection. The structure and operation of the PDC is shown in Fig. 10. The main components in the PDC are 12-bit counter, falling edge detection and output registers. The clock signal, which is generated by the frequency divider chain, works as reference signal for phase detection. On the other hand, the input signal which comes from the limiting amplifier contains original RF signal's phase information. Here, the frequency ratio between the clock signal and the reference signal is 2^{12} : 1. When both signals are sent to the PDC, the phase of the input signal can be counted directly using digital operation. The converted counter output waveform and the input signal waveforms during the detection process are shown in Fig. 10. The instantaneous phase difference between the input signal and the reference signal can be obtained by evaluating the state of the counter output at that moment. In the proposed circuit, the phase difference is evaluated at each falling edge of input signal by transferring the counter output value to the output registers at each falling edge. The PDC can re-

alize phase detection with 0.088-degree resolution which corresponds to 12-bit accuracy. The amplitude detection is realized by 10-bit successive-approximation-resister (SAR) ADC. Figure 11 shows the DC offset of ADC input signal. Before the detection, the DC offset is required to be removed. The equation of amplitude detection output are shown as follows.

$$ADC_{AVG} = \frac{\sum_{i=0}^{N-1}(ADC_i - 512)}{N} \quad (3)$$

$$ADC_{MS} = \frac{\sum_{i=0}^{N-1}(ADC_i - 512)^2}{N} \quad (4)$$

The average output of ADC is utilized for DC offset calibration. After that, the RMS output of ADC is used for magnitude detection.

4. Measurement Results

Figure 12 shows the die micrograph of proposed detection circuit. This work is fabricated in a standard 65nm CMOS process to minimize the manufacturing cost. The total core area is 1.12 mm^2. Figure 13 shows the locking range of divide-by-6 ILFD. The total locking range is 24.5-32.5GHz (28%) only with −5dBm injection power. Thanks to this ILFD, accurate reference signal generation is achieved in 5G 28GHz band.

Figure 14 shows the measurement setup of the proposed detection circuit. The calibration LO signal and the RF detection signal are generated by AWG and two synchronized signal generators. The calibration LO signal is sent into the chip using external balun. The detection signal passes through external phase shifter to change its phase. The input detection signal is converted to digital value using PDC and ADC. The value can be read out from digital logic circuit by SPI, then the value of phase and amplitude can be detected. In addition, both the LO signal and the phase shifted detection signal are also sent into an external mixer. The detection signal is down-converted to 140KHz signal to check the operation phase detection using

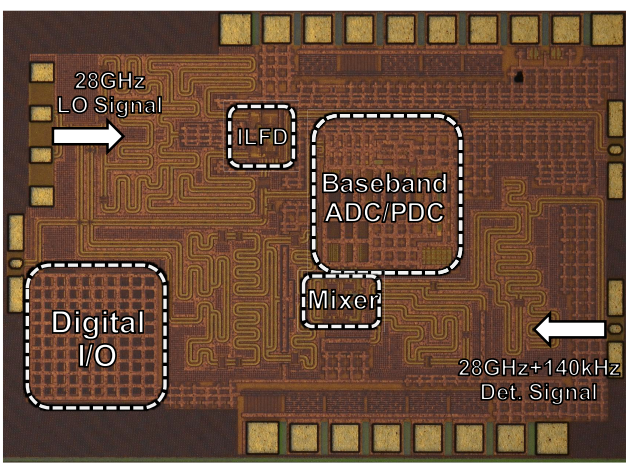

Fig. 12 Die micrograph

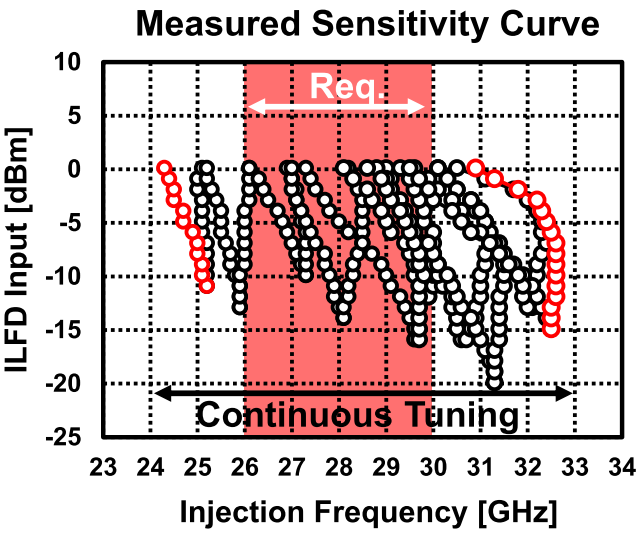

Fig. 13 The Locking range of dual-step-mixing divide-by-6 ILFD

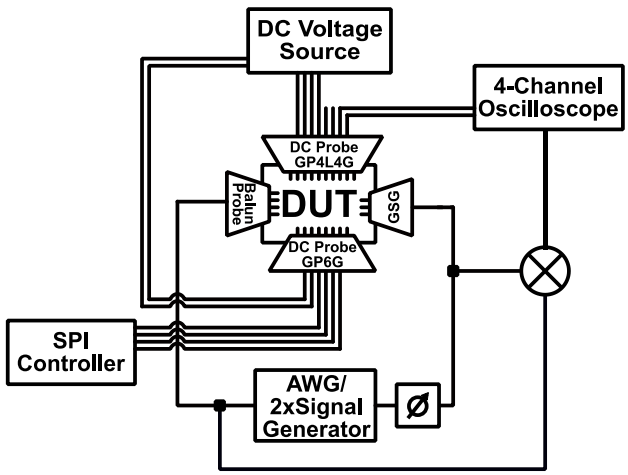

Fig. 14 Measurement setup for proposed phase and amplitude detection

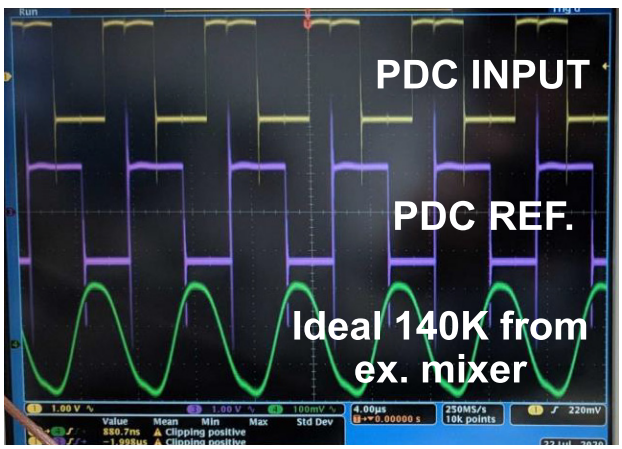

Fig. 15 Measured waveform of PDC input, PDC reference and ideal 140kHz signal

Table 1 Performance comparison

	This Work	[12]	[13]	[14]
Process	65nm CMOS	On-PCB	0.18μm SiGe	130nm CMOS
Frequency[GHz]	28	1	2-15	9.5
Amplitude Detection	ADC	N/A	I/Q	I/Q
Amplitude detection Error	0.12dB(RMS), 0.21dB(MAX)	-	0.3dB(MAX)	0.5dB(RMS)
Phase Detection	PDC	I/Q	I/Q	I/Q
Phase Detection Error	0.17deg(RMS), 0.29deg(MAX)	1deg(MAX)	3deg(MAX)	4deg(RMS)

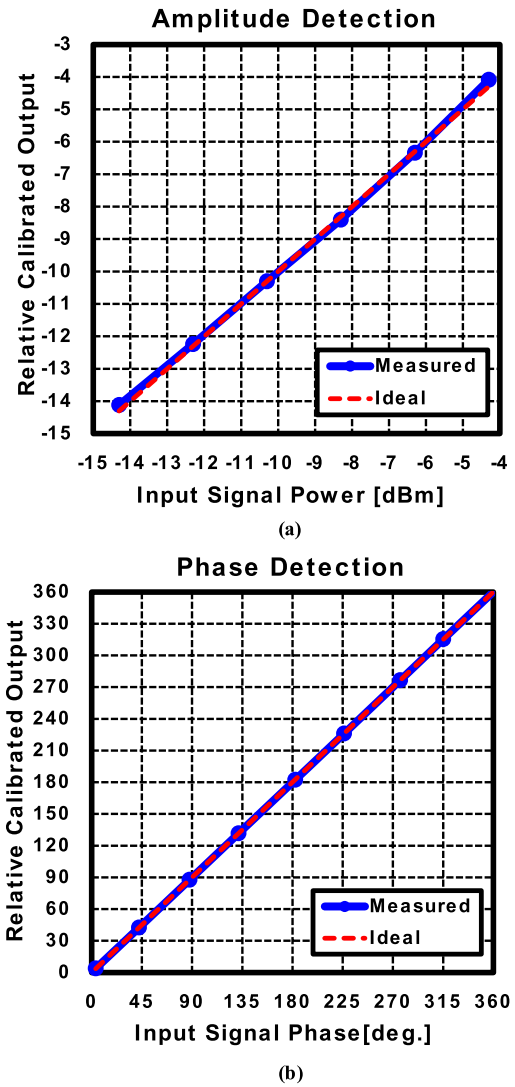

Fig. 16 The measurement results of (a) amplitude and (b) phase detection

4-channel oscilloscope such like Fig. 15. The 140kHz PDC input and reference signal in the detection circuit is output from the DC probe to the oscilloscope. This micrograph shows the frequency of all these signals is 140kHz, so high-accuracy reference signal generation and 140kHz detection signal downconversion for phase and amplitude detection can be achieved.

The measurement is done by reading the phase and amplitude detection result of the circuit while sweeping the RF input signal's power and phase from the signal generator. Measured phase and amplitude detection characteristics of the proposed circuit is shown in Fig. 16 (a) (b). The circuit can achieve amplitude detection with RMS error of 0.12dB and phase detection with RMS error of 0.17 degree. The implemented circuit consumes about 59mW of power with 1V supply voltage. Detection performance of the proposed circuit and the comparison with several other state of the art detection circuits is summarized in Table 1. The proposed circuits which utilize signal down-conversion and detections with ADC and PDC with single signal path can perform amplitude and phase detections with higher accuracy compared to conventional circuits, which use I/Q demodulation schemes with multiple signal paths to realize phase and amplitude detections.

5. Conclusion

A 28GHz high-accuracy phase and amplitude detection circuit for dual-polarized phased-array transceiver is introduced in this article. The dual-polarized calibration scheme can support high-accuracy beamforming without external LO signal. By utilizing 28GHz-to-140kHz downconversion and reference signal generation scheme using divide-by-6 dual-step-mixing ILFD, the independent detections of phase and amplitude with PDC and ADC are achieved. The RMS detection error is 0.12dB and 0.17deg, which is much lower than conventional detection scheme.

Acknowledgements

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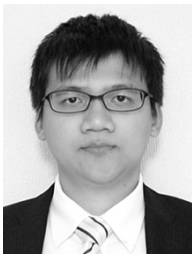
Yudai Yamazaki received B.E. degree in Electrical and Electronic Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2021. He is now continuing his M.E. degree in Electrical and Electronic Engineering at Tokyo Institute of Technology, Tokyo, Japan. His research interests include millimeter-wave CMOS wireless transceivers.



Joshua Alvin received B.E. degree in Electrical and Electronic Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2019, and received the M.S. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2021. He is currently working for Western Digital, Kanagawa, Japan.

Jian Pang received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019. From 2019 to 2020, he was a Post-Doctoral Researcher with the Tokyo Institute of Technology Dr. Pang is currently a Special-Appointed Assistant Professor with the Tokyo Institute of Technology, Tokyo, Japan, focusing on 5G millimeter-wave systems. His current research interests include high-data-rate low-cost millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile systems, multiple-in-multiple-out (MIMO), and mixed-signal calibration systems. Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Pre-Doctoral Achievement Award for the term 2018-2019, the Seiichi Tejima Oversea Student Research Award in 2020 and the IEEE MTT-S Japan Young Engineer Award in 2021.

Atsushi Shirane received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively. From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec corporation, Kawasaki, Japan, where he researched on intelligent motor with wireless communication. He is currently an Assistant Professor in the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include RF CMOS transceiver for IoT, 5G, and satellite communication. He is a member of the IEEE Solid-State Circuits Society, and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada received the B.E., M.E., and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science in Kyoto University. In 2003, he joined Tokyo Institute of Technology as an Assistant Professor. He is now a Professor of Electrical and Electronic Engineering at Tokyo Institute of Technology, Tokyo, Japan. He has authored or co-authored more than 500 journal and conference papers. His current research interests include millimeter-wave and terahertz CMOS wireless transceivers for 20/28/39/60/77/79/100/300GHz for 5G, WiGig, satellite and future wireless system, digital PLL, synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth Low-Energy, and Sub-GHz applications. Prof. Okada is a member of the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC, Prolific Author Award in 2020, the Kenjiro Takayanagi Achivement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC, Best Paper Award in 2020, and more than 50 other international and domestic awards. He is/was a member of the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), Radio Frequency Integrated Circuits Symposium (RFIC), and he also is/was Guest Editors and an Associate Editor of IEEE Journal of Solid-State Circuits (JSSC), an Associate Editor of IEEE Transactions on Microwave Theory and Techniques (T-MTT), a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS), and IEEE Fellow.