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PAPER

Single-Power-Supply Six-Transistor CMOS SRAM Enabling Low-Voltage Writing, Low-Voltage Reading, and Low Standby Power Consumption

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SUMMARY We developed a self-controllable voltage level (SVL) circuit and applied this circuit to a single-power-supply, six-transistor complementary metal-oxide-semiconductor static random-access memory (SRAM) to not only improve both write and read performances but also to achieve low standby power and data retention (holding) capability. The SVL circuit comprises only three MOSFETs (i.e., pull-up, pull-down and bypass MOSFETs). The SVL circuit is able to adaptively generate both optimal memory cell voltages and word line voltages depending on which mode of operation (i.e., write, read or hold operation) was used. The write margin (V_{WM}) and read margin (V_{RM}) of the developed (dvlp) SRAM at a supply voltage (V_{DD}) of 1 V were 0.470 and 0.1923 V, respectively. These values were 1.309 and 2.093 times V_{WM} and V_{RM} of the conventional (conv) SRAM, respectively. At a large threshold voltage (V_t) variability (= +6 σ), the minimum power supply voltage (V_{Min}) for the write operation of the conv SRAM was 0.37 V, whereas it decreased to 0.22 V for the dvlp SRAM. V_{Min} for the read operation of the conv SRAM was 1.05 V when the V_t variability (= −6 σ) was large, but the dvlp SRAM lowered it to 0.41 V. These results show that the SVL circuit expands the operating voltage range for both write and read operations to lower voltages. The dvlp SRAM reduces the standby power consumption (P_{ST}) while retaining data. The measured P_{ST} of the 2k-bit, 90-nm dvlp SRAM was only 0.957 μW at V_{DD} = 1.0 V, which was 9.46% of P_{ST} of the conv SRAM (10.12 μW). The Si area overhead of the SVL circuits was only 1.383% of the dvlp SRAM.

key words: *complementary metal-oxide-semiconductor (CMOS), static random-access memory (SRAM), write margin, read margin, standby power consumption, leakage current, minimum supply voltage, area overhead, self-controllable voltage level circuit, single power source*

1. Introduction

Decreasing the size of the metal-oxide-semiconductor field-effect transistor (MOSFET) not only decreases the threshold voltage (V_t) but also increases the standard deviation (σ) of V_t [1]. As a result, the write and read margins are reduced, write and read operations fail at low voltages, and leakage currents increase appreciably.

Conventional (conv) six-transistor (6T) static random-access memory (SRAM) memory cells offer high areal densities, but as the supply voltage decreases, they are unable to simultaneously achieve large write and read margins. A number of techniques have been proposed to improve the write margin and/or read margin at a low supply voltage [2]–[5], as in the examples of a dual-rail SRAM that generates a lower cell-V_{DD} with a certain voltage offset with respect to the logic-V_{DD} [2], SRAM with an integrated column-based dynamic multi-V scheme [3], 6T SRAM with a level-programmable word line driver [4], and single-power-supply 6T SRAM with read and write cell stabilizing circuits [5].

An eight-transistor (8T) SRAM memory cell, which comprised the original 6T SRAM memory cell and two additional MOSFETs [6]–[9], has alternatively been proposed. Reports of 8T SRAM memory cells included 8T SRAM having a dual-port memory cell with two pairs of parallel pass gates [6], cross-point 8T SRAM with negative bias read/write assist [7], 8T SRAM with a 2T read stack sense amplifier for read only [8], and 8T SRAM with a memory cell adopting sense-amplifier redundancy [9]. However, regardless of which of the above methods is used, the use of an 8T memory cell leads to an area penalty (i.e., a low area density).

To solve the above problems, we developed a new circuit called the self-controllable voltage level (SVL) circuit and implemented it in single-power-supply, 6T, 90-nm, 2-kbit complementary metal-oxide-semiconductor (CMOS) SRAM. The SVL circuit comprises only three MOSFETs, namely pull-up, pull-down, and bypass MOSFETs. The SVL circuit quickly steps down the externally supplied voltage (V_{DD}) and supplies this stepped-down voltage to the memory cells during writing and to the word line drivers during reading. The features of the developed (dvlp) SRAM equipped with this SVL circuit are (1) the low-voltage write and read, (2) the large write and read margins, (3) data retention during standby, and (4) low leakage current during standby.

The present study found that the write margin (V_{MW}) of the dvlp SRAM at V_{DD} = 1.0 V was 0.470 V, which was 1.309 times V_{MW} (= 0.359 V) of conv SRAM. The read margin (V_{MR}) of the dvlp SRAM at V_{DD} = 1.0 V was 0.1923 V, which was 2.093 times V_{MR} (= 0.0919 V) of the conv SRAM. The SVL circuit is an effective means of increasing the write and read margins. The minimum power supply voltage (V_{MinW}) at which data were written to the conv SRAM was 0.37 V when the threshold voltage (V_t) variability was extremely large (= +6 σ). In contrast, V_{MinW} of the dvlp SRAM (applied with the SVL circuit) decreased to 0.22 V. For very large V_t variability (= −6 σ), the min-

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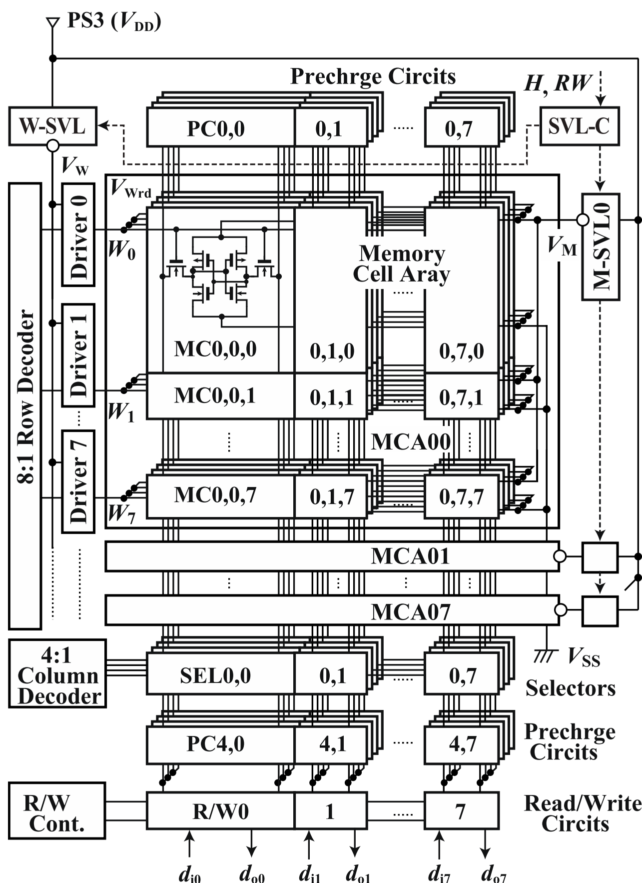


Fig. 1 Developed single-power-supply, six-transistor, 2k-bit SRAM with the built-in self-controllable voltage level (SVL) circuits.

imum supply voltage (V_{MinR}) at which data were read was 1.05 V for conv SRAM and 0.41 V for dvlp SRAM. The dvlp SRAM reduced the standby power consumption (P_{ST}) while retaining data. P_{ST} of the dvlp SRAM measured at V_{DD} = 1.0 V was only 0.957 μW, which is 9.46% of P_{ST} of the conv SRAM (10.12 μW). The area overhead of the SVL circuit was 1.383% relative to the dvlp SRAM area. These results demonstrate that the SVL circuit improves margins (V_{MW} and V_{MR}), lowers minimum power supply voltages (V_{MinW} and V_{MinR}), and reduces P_{ST}.

In the following, we describe the structure and operation of the dvlp SRAM with SVL circuits applied (Sect. 2) and the write, read, and standby mode characteristics of conv and dvlp SRAMs (Sects. 3, 4, and 5).

2. SRAM Structure and Operation

2.1 Structure of the Developed SRAM

Figure 1 shows the circuit configuration of the dvlp single-power-supply 6T, 2k-bit CMOS SRAM. This SRAM includes a memory cell array (8 bits × 4 words × 64 words), self-controllable voltage level (SVL) circuits for the memory cell array (M-SVLs), an SVL circuit for word line drivers (W-SVL), an SVL circuit controller (SVL-C), and

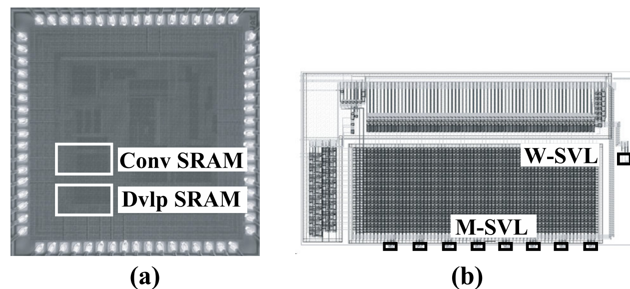


Fig. 2 Prototype chip fabricated through 90-nm CMOS processing. (a) A 2.5 × 2.5-mm^2 chip with the developed SRAM and conventional SRAM. (b) Layout of the developed SRAM incorporating the SVL circuits.

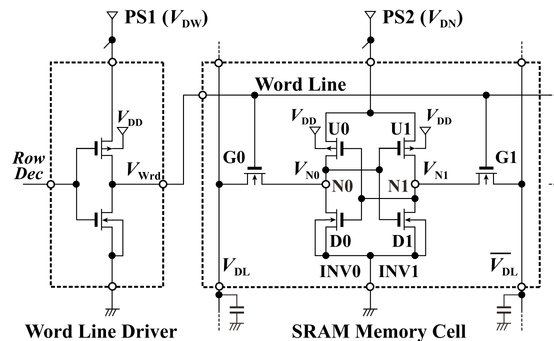


Fig. 3 Memory cell and word line driver of the conventional SRAM.

peripheral circuits. There are eight M-SVLs in total, one for each 256-bit (8 bits × 4 words × 8 words) memory cell array, which supply power (V_M) to the memory cell array. One W-SVL is included to supply power (V_W) to the word line drivers.

Figure 2 (a) shows a 2.5 × 2.5-mm^2 prototype chip made using 90-nm CMOS technology. It includes the dvlp SRAM and a conv SRAM (without M-SVLs, the W-SVL and the SVL-C). Figure 2 (b) presents the layout of the dvlp SRAM. The silicon areas of the conv SRAM and dvlp SRAM are 65,365 and 66,269 μm^2, respectively. The area overhead of the M-SVLs, W-SVL, and SVL-C is 1.383% relative to the dvlp SRAM area.

2.2 Circuit Diagram

A Conventional SRAM

Figure 3 shows the memory cell and word line driver in the conv SRAM. The memory cell comprises inverter 0 (INV0), inverter 1 (INV1), and two path gates (G0 and G1). U0 and U1 are pMOSFETs, whereas D0, D1, G0, and G1 are nMOSFETs. PS1 and PS2 are the power terminals for the word line driver and memory cell, respectively.

B Developed SRAM

Figure 4 shows the memory cell, word line driver, M-SVL, W-SVL, and SVL-C of the dvlp SRAM. The memory cell structure of the dvlp SRAM is the same as that of the conv

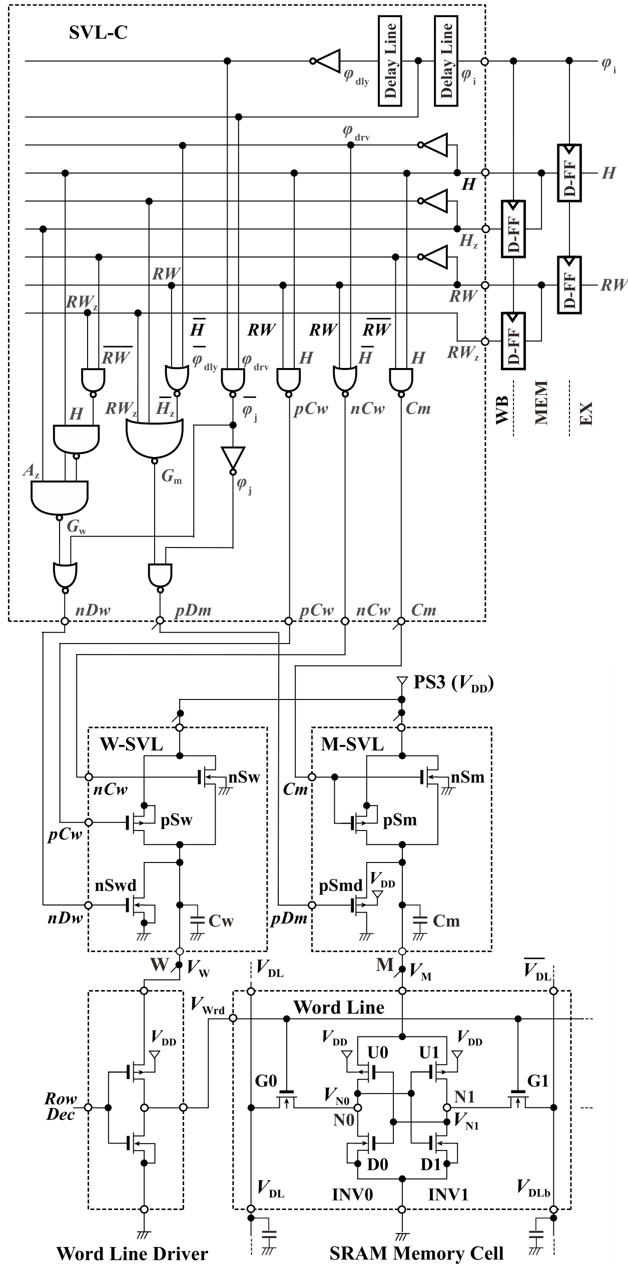
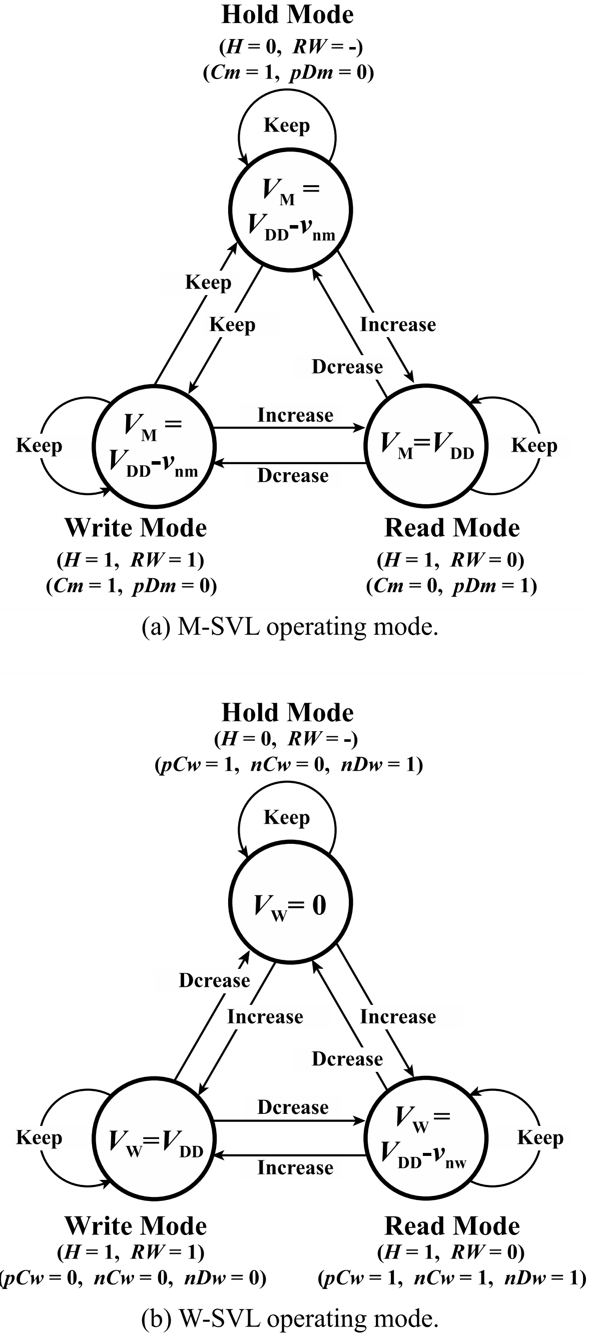


Fig. 4 Memory cell, word line driver, M-SVL, W-SVL, and SVL-C in the developed SRAM.



(a) M-SVL operating mode.

(b) W-SVL operating mode.

Fig. 5 Three operating modes (write, read, and hold modes) of the developed SRAM and the voltages generated by the M-SVL and W-SVL.

SRAM. PS3 is the power terminal for the dvlp SRAM.

M-SVL comprises a pull-up pMOSFET (pSm) that boosts the memory cell supply voltage (V_M) of the dvlp SRAM, a pull-down nMOSFET (nSm) that steps down V_M, and a bypass pMOSFET (pSmd) that discharges Cm. Cm is the stray capacitance of 256 memory cells seen from M-SVL (point M).

W-SVL comprises a pull-up pMOSFET (pSw) that boosts the word line driver supply voltage (V_W) of the dvlp SRAM, a pull-down nMOSFET (nSw) that steps down V_W, and a bypass nMOSFET (nSwd) that discharges Cw. Cw is the stray capacitance of eight-word line drivers seen from W-SVL (point W).

SVL-C is an on-chip circuit that comprises a small number of logic gates and generates three control signals and two discharge pulses from two input signals and a clock pulse (φ_i). Inputs are the hold control signal (H) and read/write control signal (RW). Outputs are the control signal (Cm) and discharge pulse (pDm) for M-SVL and the control signal (nCw, pCw) and discharge pulse (nDw) for W-SVL. SVL-C inputs, SVL-C outputs, V_M and V_W are shown in Figs. 5 and 6 in the next section.

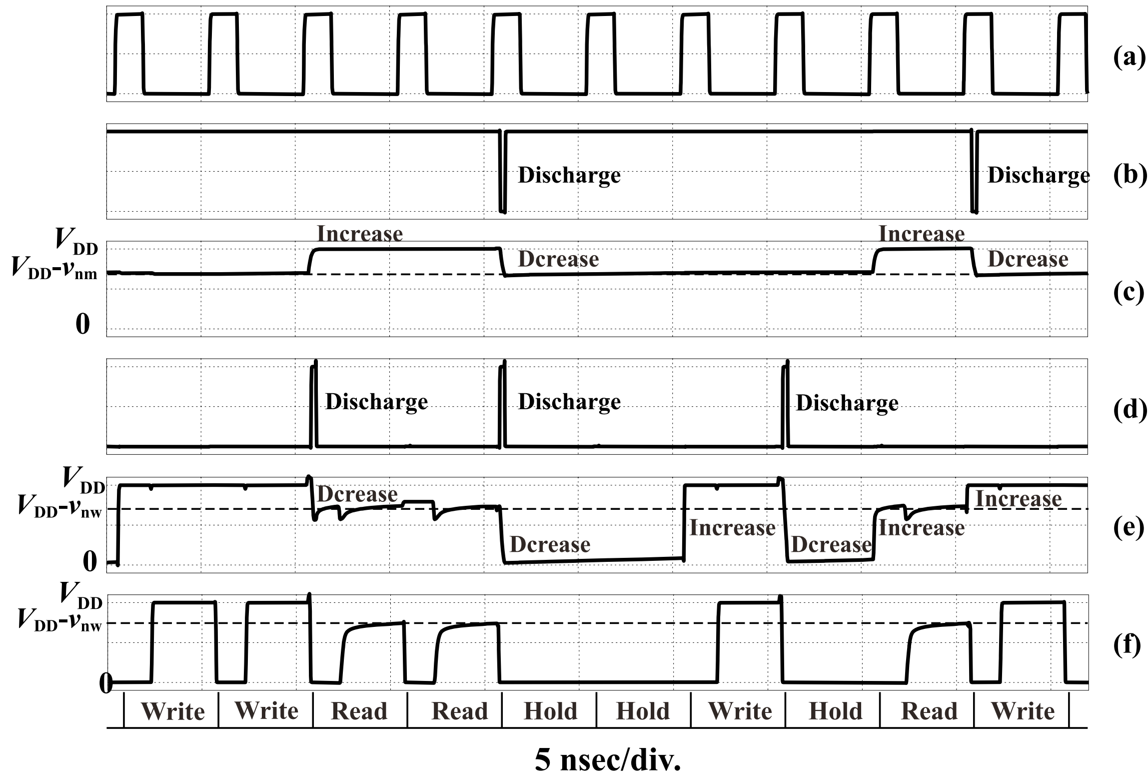


Fig. 6 Voltage waveforms at each node of the developed SRAM. (a) Clock pulse (φ_i). (b) pSmd control pulse (*pDm*). (c) Voltage supply to memory cells (V_M). (d) nSwd control pulse (*nDw*). (e) Voltage supply to the word line driver (V_W). (f) Word line voltage (V_{Wrd}).

Table 1 Voltage (V_M) supplied to the memory cell by M-SVL, control signal 0/1 state (*Cm*,*pDm*), and MOSFET on/off state (pSm, nSm, pSmd)

Mode	V_M	*Cm*	pSm	nSm	*pDm*	pSmd
Write	V_{DD}-v_{nm}	1	off	on	0	on
Read	V_{DD}	0	on	off	1	off
Hold	V_{DD}-v_{nm}	1	off	on	0	on

Table 2 Voltage (V_W) supplied by W-SVL to the word line driver, control signal 0/1 state (*pCw*,*nCw*,*nDw*) and MOSFET on/off state (pSw, nSw, nSwd)

Mode	V_W	*pCw*	pSw	*nCw*	nSw	*nDw*	nSwd
Write	V_{DD}	0	on	0	off	0	off
Read	V_{DD}-v_{nw}	1	off	1	on	1	on
Hold	0	1	off	0	off	1	on

2.3 Operating Modes of the Developed SRAM and Voltage Generated by the SVL Circuit

The dvlp SRAM has three modes of operation, namely write, read, and hold (standby) modes. Figure 5 (a) and (b) shows the operating modes of M-SVL and W-SVL, respectively. Also shown are the M-SVL and W-SVL output voltages (V_M and V_W) and the 0/1 states of the input and output signals of SVL-C. Tables 1 and 2 summarize V_M and V_W for the three SRAM operating modes. These tables contain 0/1 states of control signals and on/off states of MOSFET. Figure 6 shows the voltage waveforms of the dvlp SRAM at various nodes. Figure 6 (a), (b), (c), (d), (e), and (f) respectively presents the clock pulse (φ_i), pSmd control pulse (*pDm*), memory cell supply voltage (V_M), nSwd control pulse (*nDw*), word line driver supply voltage (V_W), and word line voltage (V_{Wrd}).

A Write Mode

With the control signal (*Cm*) set to 1, pSm turns off and nSm operates (Table 1). The voltage (V_M) generated by M-SVL is set to ($V_{DD} - v_{nm}$), when the write mode begins {Fig. 5 (a), Fig. 6 (c)}. Here, ($V_{DD} - v_{nm}$) is the voltage drop of 256 memory cells seen from point M, V_{DD} is the supply voltage to M-SVL (terminal PS3), and v_{nm} is the voltage drop of nSm.

When the write mode starts, the voltage (V_W) generated by W-SVL is set to V_{DD} by turning pSw on and nSw off with the control signals (*pCw* and *nCw*) set to 0 {Table 2, Fig. 5 (b), Fig. 6 (e)}. Thus, the word line voltage (V_{Wrd}) for the selected word line is set to V_{DD} {Fig. 6 (f)}.

B Read Mode

With *Cm* set to 0, pSm turns on and nSm turns off. V_M is

set to V_{DD} when the read mode starts {Table 1, Fig. 5 (a), Fig. 6 (c)}. Meanwhile, V_W is set to ($V_{DD} - v_{nw}$) by turning pSw off and turning nSw on, when the read mode starts {Table 2, Figs. 5 (b) and 6 (e)}. Here, ($V_{DD} - v_{nw}$) is the voltage drop of eight clock drivers seen from point W and v_{nw} is the voltage drop of nSw.

C Hold Mode

As well as the write mode with *Cm* set to 1, pSm turns off and nSm operates {Table 1, Fig. 5 (a)}. V_M is set to ($V_{DD} - v_{nm}$) when the hold mode begins {Fig. 6 (c)}. Meanwhile, V_W is set to 0 V by turning off pSw and nSw when the hold mode starts {Table 2, Fig. 5 (b), Fig. 6 (e), Fig. 6 (f)}. This not only results in data being held (stored) but also reduces leakage current (i.e., reduces standby power consumption).

2.4 Effects of Bypass Switches in SVL Circuits

A M-SVL Operation

When changing from the read mode to the write or hold mode, the voltage supplied to the memory cell (V_M) must be quickly stepped down from V_{DD} to ($V_{DD} - v_{nm}$). However, SRAM with an M-SVL, in which the bypass switch to discharge Cm was not installed [10], [11], took a long time to step down V_M. The reason for this is that stored charge in the large Cm had to be discharged through a large equivalent resistance (Rm). Here, Rm is the equivalent resistance of the memory cell viewed from point M.

To solve the above problem, a bypass switch (pSmd) for the quick discharge of Cm was installed in parallel with Cm (Fig. 4). First, we set the control signal (*Cm*) to 1 to turn on nSm. Next, when the control signal (*pDm*) is set to 0 for a short time {Table 1, Fig. 6 (b)}, pSmd is temporarily turned on, and the charge in Cm is rapidly discharged {Fig. 6 (c)}. Finally, V_M converges quickly to the voltage ($V_{DD} - v_{nm}$) determined by the resistor values of nSm and Rm.

B W-SVL Operation

In the transition from the write mode to the read mode, the voltage supplied to the word line driver (V_W) is stepped down from V_{DD} to ($V_{DD} - v_{nw}$). As with the setting of V_M described above, because the charge in the large Cw must be discharged through the large equivalent resistance (Rw) seen from point W, it takes a long time to step down V_W.

To step down V_W rapidly, a bypass switch (nSwd) with the same function as pSmd in the M-SVL circuit is installed in parallel with Cw (Fig. 4). First, we set the control signals (*nCw* and *pCw*) to 1 to turn on nSw and turn off pSw. Next, when the control signal (*nDw*) is set to 1 for a short time {Table 2, Fig. 6 (d)}, nSwd is briefly turned on, and the charge accumulated in Cw is quickly discharged {Fig. 6 (e)}. Finally, V_W rapidly converges to the voltage ($V_{DD} - v_{nw}$) determined by the resistance values of nSw and Rw.

Similarly, when changing from the read mode to hold mode, V_W is stepped down from ($V_{DD} - v_{nw}$) to 0 V. V_W is also stepped down from V_{DD} to 0 V when changing from the write mode to hold mode. We first set *nCw* to 0 and *pCw* to 1 to turn off nSw and pSw. We next set *nDw* momentarily to 1 {Table 2, Fig. 6 (d)} and turn on nSwd briefly to quickly discharge the charge stored in Cw. Finally, V_W becomes 0 V {Fig. 6 (e)}.

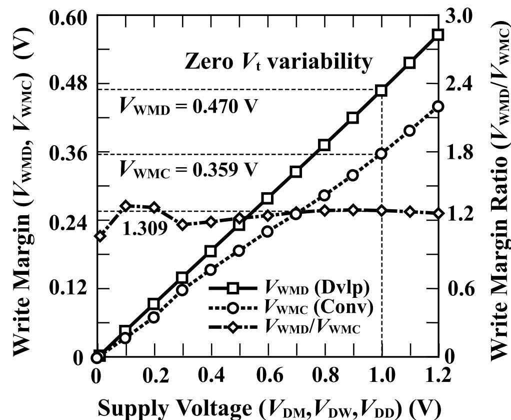


Fig. 7 Write margin (V_{WM}) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis with T = 25°C and zero V_t variability).

Table 3 MOSFET threshold voltage (V_t) and V_t variability

V_t variability	+6σ	0	-6σ
nMOSFET V_{tn} (V)	0.275	0.222	0.142
pMOSFET V_{tp} (V)	- 0.139	- 0.241	- 0.300

3. Characteristics of the Write Mode

3.1 Write Margin

Figure 7 shows the relationship between the static write margin (V_{WM}) and the supply voltages (V_{DW}, V_{DM}, and V_{DD}) applied to the power supply terminals (PS1, PS2, and PS3) (T = 25°C, zero V_t variability).

The write margin (V_{WM}) was obtained via the following procedure using SPICE. First, V_{DW}, V_{DM}, V_{DD}, and V_{DLb} were set to given values (V_D) and V_{DL} was fixed to 0 V, and the transfer characteristics (V_{N0} *vs* V_{N1}) of INV0 and INV1 were obtained. The transfer characteristics were then superimposed to create a butterfly curve. Finally, V_{WM} was defined as the length of the square that touches the eye of the butterfly curve.

The solid line, dashed line, and dash-dotted line in Fig. 7 show the write margin of the dvlp SRAM (V_{WMD}), the write margin of the conv SRAM (V_{WMC}), and the write margin ratio (V_{WMD}/V_{WMC}), respectively. The nMOSFET threshold voltage (V_{tn}) and pMOSFET threshold voltage (V_{tp}) respectively have mean values of 0.222 V and –0.241 V. The threshold voltage (V_t) variability in this case is defined as zero (Table 3).

V_{WMD} is always greater (better) than V_{WMC} when V_{DD}

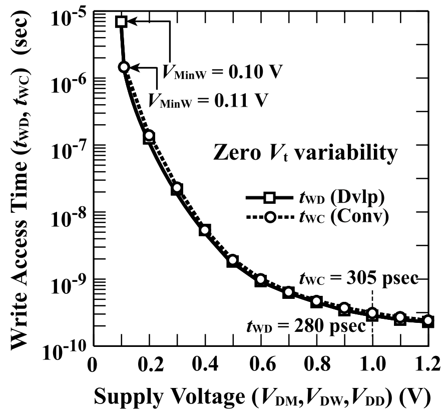


Fig. 8 Write access time (t_W) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis with T = 25°C and zero V_t variability).

is 0.01 V or higher. For example, when V_{DD} is 1 V, V_{WMD} and V_{WMC} are respectively 0.470 and 0.359 V; i.e., V_{WMD} is 1.309 times larger (better) than V_{WMC} [12], [13]. This is explained by the M-SVL stepping down the memory cell supply voltage V_M to ($V_{DD} - v_{nm}$). Similarly, even with large V_t variability (= $+6\sigma$ and -6σ), V_{WMD} is higher than V_{WMC}.

3.2 Write Access Time

Figure 8 shows the relationship between the write access time (t_W) and power supply voltages (V_{DW}, V_{DM}, and V_{DD}) obtained in SPICE analysis (T = 25°C, zero V_t variability). Note that t_W is defined as the time from when the address is latched to when the N0 node potential (V_{N0}) and N1 node potential (V_{N1}) change by 50%. The solid line and dashed line show t_W of the dvlp SRAM (t_{WD}) and t_W of the conv SRAM (t_{WC}), respectively. The minimum writable supply voltage (V_{MinW}) is 0.11 V for the conv SRAM and 0.10 V for the dvlp SRAM. When V_{DD} is 0.11 V or higher, t_{WD} is approximately 10% shorter (faster) than t_{WC}. This is explained in that V_M is stepped down to ($V_{DD} - v_{nm}$) by M-SVL, similar to the reason why V_{WMD} is always higher than V_{WMC}. For example, at V_{DD} = 1 V, t_{WD} (= 280 psec) is 25 psec shorter (8.2% faster) than t_{WC} (= 305 psec).

When the V_t variability is -6σ (where σ is the standard deviation) (Table 3), the write access time characteristics (t_{WD}, t_{WC}) are almost the same as the characteristics when the V_t variability is zero (Fig. 8). V_{MinW} is 0.27 V for both the conv SRAM and dvlp SRAM.

Figure 9 shows the relationships between t_W and V_{DW}, V_{DM}, and V_{DD} when the V_t variability is $+6\sigma$ (Table 3). In this case, V_{MinW} of the conv SRAM is 0.37 V, and writing is not possible below 0.36 V. Meanwhile, the dvlp SRAM has V_{MinW} of 0.22 V, which means that the dvlp SRAM has a wider (improved) writable voltage range than the conv SRAM. That is to say, the SVL circuit is extremely effective in extending V_{MinW} even when the V_t variability (= $+6\sigma$) is large. This is explained in that V_M is stepped down to ($V_{DD} - v_{nm}$) by M-SVL, and it is seen that M-SVL is extremely effective in extending V_{MinW}.

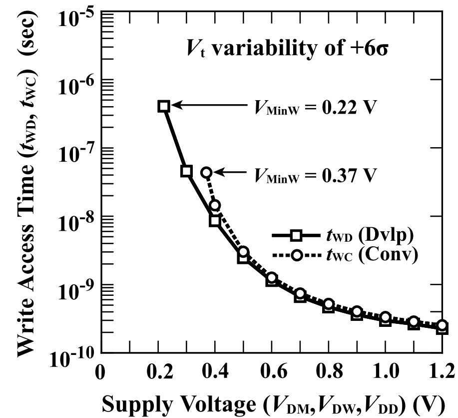


Fig. 9 Write access time (t_W) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis with T = 25°C and V_t variability of $+6\sigma$).

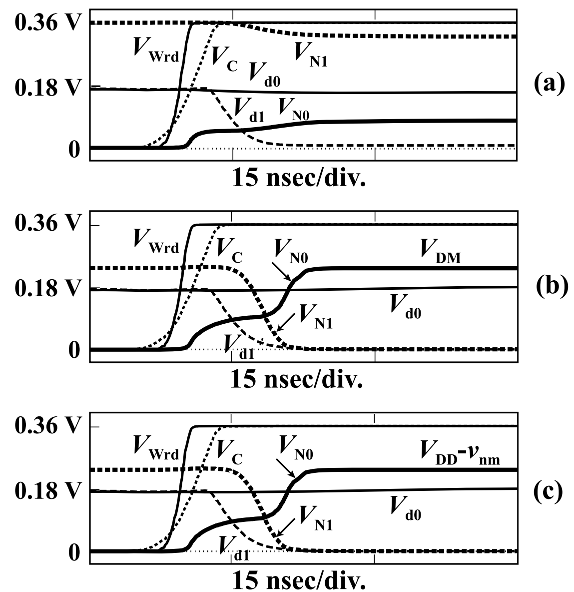


Fig. 10 Potential waveforms at each memory cell node in write mode (SPICE analysis at T = 25°C, f_c = 1 MHz, and V_t variability of $+6\sigma$). (a) Rewrite failure case for conv SRAM at V_{DW} = V_{DM} = 0.36 V. (b) Rewrite success case for conv SRAM at V_{DW} = 0.36 V and V_{DM} = 0.24 V. (c) Rewrite success case for dvlp SRAM at V_{DD} = 0.36 V.

3.3 Data Rewriting Operation

A Rewriting Failure Case for Conv SRAM

As mentioned above, conv SRAM fails to write (rewrite) data when V_{DD} is less than 0.36 V and V_t variability is as large as $+6\sigma$. Figure 10 (a) shows the potential waveform of each node of the conv SRAM when V_{DW} and V_{DM} supplied to PS1 and PS2 are 0.36 V at T = 25°C and V_t variability of $+6\sigma$. This is an example of rewriting the stored datum 0 (V_{N0} = 0, V_{N1} = V_{DM} = 0.36 V) to a new datum 1 (V_{N0} = V_{DM}, V_{N1} = 0). If the rewrite operation is performed correctly, V_{N0} and V_{N1} should be inverted. However, here,

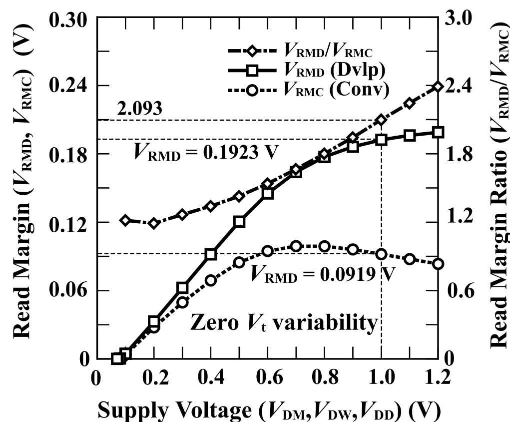


Fig. 11 Read margin (V_{RM}) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis at T = 25°C and zero V_t variability).

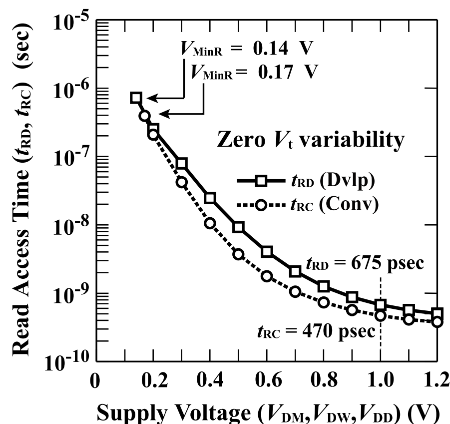


Fig. 12 Read access times (t_R) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis at T = 25°C and zero V_t variability).

the original stored datum is retained as it is, and V_{N0} and V_{N1} are not inverted. That is to say, data rewriting has failed.

B Rewriting Success Case for Conv SRAM

Figure 10 (b) shows the potential waveform of each node of the conv SRAM, when V_{DW} is kept at 0.36 V and only V_{DM} is stepped down, from 0.36 to 0.24 V (T = 25°C and V_t variability of $+6\sigma$). V_{N0} and V_{N1} are inverted, the original stored datum 0 (V_{N0} = 0, V_{N1} = V_{DM} = 0.24 V) is rewritten to the new datum 1 (V_{N0} = V_{DM} = 0.24 V, V_{N1} = 0), and the data rewriting is successful. However, this approach requires two separate power supplies, one for the memory cells and one for the word line drivers.

C Rewriting Success Case for Dvlp SRAM

Figure 10 (c) shows the potential waveform of each node of the dvlp SRAM, where V_{DD} supplied to PS3 is 0.36 V, T is 25°C and V_t variability is $+6\sigma$. Figure 10 (c) shows that the datum has been successfully rewritten. Furthermore, the shape of the potential waveform at each node in Fig. 10 (c) is exactly the same as that of the conv SRAM {Fig. 10 (b)}. This also indicates that the datum has been successfully rewritten. This is because the SVL circuits automatically set the word line driver supply voltage (V_W) and memory cell supply voltage (V_M) to 0.36 and 0.24 V (= $V_{DD} - v_{nm}$), respectively. As mentioned above, the conv SRAM requires two separate power supplies. In contrast, the dvlp SRAM has the advantage of requiring only one power supply.

4. Characteristics of the Read Mode

4.1 Read Margin

Figure 11 shows the relationship between the static read margin (V_{RM}) and the supply voltages (V_{DW}, V_{DM}, and V_{DD}) applied to the power supply terminals (PS1, PS2, and PS3) (T = 25°C, zero V_t variability).

The read margin (V_{RM}) was also obtained by the following procedure using SPICE. We fix V_{DW}, V_{DM}, V_{DD}, V_{DL}, and V_{DLb} to a given value (V_D) and obtain the transfer characteristics (V_{N0} *vs* V_{N1}) of INV0 and INV1 (see Figs. 3 and 4). Next, we superimpose the transfer characteristics to obtain the butterfly curve. V_{RM} is defined as the length of a square that touches the eye of the butterfly curve.

The solid line, dashed line, and dash-dotted line in Fig. 11 are respectively the developed (dvlp) SRAM read margin (V_{RMD}), conventional (conv) SRAM read margin (V_{RMC}), the read margin ratio (V_{RMD}/V_{RMC}).

V_{RMD} is much greater (better) than V_{RMC} when V_{DD} is greater than 0.08 V. For example, when V_{DD} is 1 V, V_{RMD} and V_{RMC} are respectively 0.1923 and 0.0919 V; i.e., V_{RMD}/V_{RMC} is 2.093 [12], [13]. In other words, V_{RMD} is 2.093 times larger (better) than V_{RMC}. This improvement is achieved as a result of W-SVL stepping down the word line driver supply voltage V_W to ($V_{DD} - v_{nw}$). Similarly, even with large V_t variability (= $+6\sigma$ or -6σ) (Table 3), V_{RMD} is higher than V_{RMC}.

4.2 Read Access Time

Figure 12 shows the read access time (t_R) versus supply voltages (V_{DW}, V_{DM} and V_{DD}) obtained from SPICE analysis (T = 25°C, zero V_t variability). Note that t_R is defined as the time from when the address is latched until the datum is output to the readout circuit. The solid line and dashed line show t_R for dvlp SRAM (t_{RD}) and t_R for conv SRAM (t_{RC}), respectively. The minimum readable supply voltage (V_{MinR}) is 0.14 and 0.17 V for dvlp SRAM and conv SRAM, respectively.

For supply voltages above 0.2 V, t_{RD} is longer than t_{RC}. For example, with V_{DD} = 1 V, t_{RD} is 675 psec, which is longer than t_{RC} (= 470 psec). This is because the word line voltage (V_{Wrd}) has been stepped down. Meanwhile, V_{MinR} of dvlp SRAM is 0.14 V, lower than that (= 0.17 V) of conv SRAM. In other words, the readable operating range is extended. This is because V_{Wrd} is stepped down. Note that

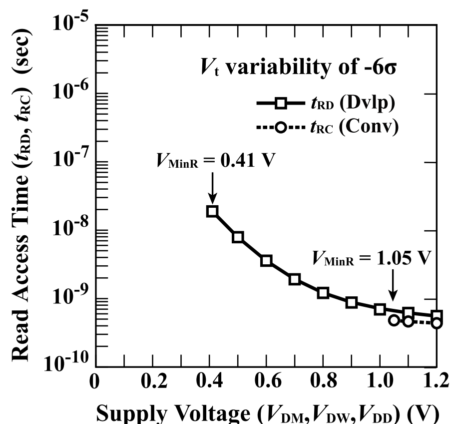


Fig. 13 Read access times (t_R) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) (obtained in SPICE analysis at $T = 25°C$ and V_t variability of -6σ).

t_{RD} can be sped up by increasing the drive capability of the readout circuit.

For V_t variability of $+6\sigma$, the read access time characteristics (t_{RD} and t_{RC}) are similar to those shown in Fig. 12 for zero V_t variability. V_{MinR} is 0.20 V for both the conv SRAM and dvlp SRAM.

The simulated t_{RD} (solid lines) and t_{RC} (dotted lines) are plotted as functions of V_{DD}, V_{DM}, and V_{DW} in Fig. 13 (at V_t variability of -6σ and $T = 25°C$). V_{MinR} is 0.41 V, which is much lower (i.e., much better) than V_{MinR} (= 1.05 V) of the conv SRAM. This means that the dvlp SRAM has a much wider readable voltage range than the conv SRAM. It is clear that a great improvement in the read characteristics of this dvlp SRAM is achieved by lowering the word line voltage (V_{Wrd}).

4.3 Data Reading Operation

A Read Failure Case for Conv SRAM

As mentioned earlier, conv SRAM has V_{MinR} of 1.05 V. Therefore, data cannot be read out when V_{DD} is below 1.04 V. Figure 14 (a) shows the simulated voltage levels at various nodes of the conv SRAM when V_{DW} and V_{DM} supplied to PS1 and PS2 are 1.04 V (at $T = 25°C$ and V_t variability of $+6\sigma$). This is an example of reading the stored datum 0 ($V_{N0} = 0$ V, $V_{N1} = 1.04$ V). However, when the word line (V_{Wrd}) is activated, V_{N0} and V_{N1} are inverted. This means that the wrong datum 1 ($V_{N0} = 1.04$ V, $V_{N1} = 0$ V) is read out and the read operation fails.

B Read Success Case for Conv SRAM

Figure 14 (b) illustrates the simulated voltage levels at various nodes of the conv SRAM, where V_{DW} applied to PS1 is reduced from 1.04 to 0.70 V whereas V_{DM} applied to PS2 is set at 1.04 V ($T = 25°C$, V_t variability of $+6\sigma$). Here, the stored datum is 0 ($V_{N0} = 0$, $V_{N1} = 1.04$ V). When the word line (V_{Wrd}) is activated, V_{N0} and V_{N1} are maintained at

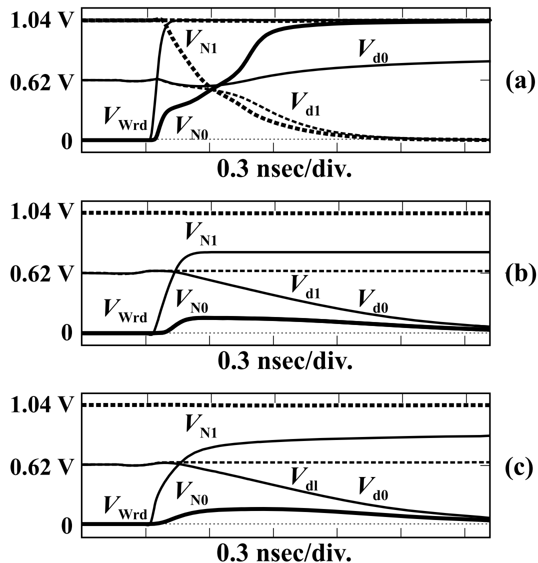


Fig. 14 Potential waveforms at each memory cell node in read mode (SPICE analysis at $T = 25°C$, $f_c = 1$ MHz, and V_t variability of -6σ). (a) Read failure case for conv SRAM at $V_{DW} = V_{DM} = 1.04$ V. (b) Read success case for conv SRAM at $V_{DW} = 0.70$ V and $V_{DM} = 1.04$ V. (c) Read success case for dvlp SRAM at $V_{DD} = 1.04$ V.

their original low level (0 V) and high level (1.04 V). Therefore, lowering V_{Wrd} makes the conv SRAM successful in the read operation. However, this technique requires two power supplies, namely V_{DM} for the memory cells and V_{DW} for the word line drivers.

C Read Success Case for Dvlp SRAM

The dvlp SRAM successfully reads the stored data when the voltage (V_{DD}) applied to the terminal (PS3) is 1.04 V ($T = 25°C$, V_t variability of $+6\sigma$) {Fig. 14 (c)}. The shape of the potential waveform of each node in Fig. 14 (c) is exactly the same as that for the conv SRAM {Fig. 14 (b)}. The conv SRAM requires two power supplies to set the word line voltage (V_{DW}) and memory cell voltage (V_{DM}) to 0.7 and 1.04 V, respectively. In contrast, the dvlp SRAM requires only one power supply ($V_{DD} = 1.04$ V). This is because the SVL circuit automatically sets the word line driver supply voltage (V_W) and memory cell supply voltage (V_M) to 0.7 V (= $V_{DD} - v_{nw}$) and 1.04 V, respectively. It is seen that the SVL circuit is effective in extending the minimum read operation voltage of the single-power-supply SRAM even with large V_t variability (= $+6\sigma$).

5. Power Consumption and Operation Speed

As MOSFETs become smaller, the leakage current (I_L) and standby power consumption (P_{ST}) increase. Figure 15 shows the measured P_{ST} of developed (dvlp) SRAM as a function of the supply voltage (V_{DD}) at $T = 25°C$. This P_{ST} includes P_{ST} for peripherals that are stopped by clock gating in the SRAM standby period. The range of values obtained for five chips is indicated by error bars. The

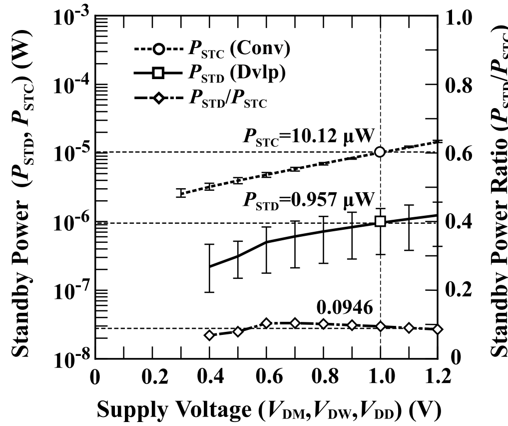


Fig. 15 Measured standby power (P_{ST}) versus supply voltages (V_{DM}, V_{DW}, and V_{DD}) at T = 25°C.

Table 4 Characteristics of conv SRAM and dvlp SRAM at T = 25°C

		Conv	Dvlp	Dvlp /Conv
Write margin V_{WM} (V)	*	0.359	0.470	1.309
Minimum writable voltage V_{MinW} (V)	*	0.11	0.10	
Minimum writable voltage V_{MinW} (V)	**	0.37	0.22	
Read margin V_{RM} (V)	*	0.0919	0.1923	2.093
Minimum readable voltage V_{MinR} (V)	*	0.17	0.14	
Minimum readable voltage V_{MinR} (V)	***	1.05	0.41	
Standby power P_{ST} (μW)		10.12	0.957	0.0946
Max. f_c (MHz)	*	834	826	0.9904
Active power P_{AT} (mW) at f_c = 800 MHz	*	2.038	1.944	0.9540
Silicon area (μm^2)		65,365	66,269	1.01383

*zero V_t variability, **V_t variability of +6σ,
***V_t variability of -6σ

dashed, solid, and dotted/dashed lines show the average P_{ST} of conv SRAM (P_{STC}) for the five chips, the average P_{ST} of dvlp SRAM (P_{STD}) for the five chips, and the power ratio (average-P_{STD}/average-P_{STC}), respectively.

The average value of P_{STC} at V_{DD} = 1 V is 10.12 μW, which is comparable to the simulated P_{STC} (10.28 μW). Additionally, the average P_{STD} is 0.957 μW, which is likewise equivalent to P_{STD} (0.984 μW at zero V_t variability) obtained in SPICE analysis. The average-P_{STD}/average-P_{STC} ratio is approximately 10% over any voltage band and is 9.46% at V_{DD} = 1 V [13]. This shows that the M-SVL and W-SVL circuits are extremely effective in reducing I_L and thus decreasing P_{ST}. This is explained in that the M-SVL steps down the memory cell supply voltage V_M to ($V_{DD} - v_{nm}$) and the W-SVL steps down the word line driver supply voltage V_W to 0 V.

At a clock frequency f_c = 800 MHz and zero V_t variability, the operating power consumption (P_{AT}) for the dvlp SRAM is 1.944 mW, which is 95.4% of that for the conv SRAM (2.038 mW) [13]. Additionally, the maximum operating f_c (Max. f_c) of dvlp SRAM is 826 MHz, which is 99.04% of that of conv SRAM (834 MHz) [13]. It is thus concluded that the SVL circuit does not affect P_{AT} or the speed performance.

Table 4 summarizes the dvlp SRAM and conv SRAM characteristics.

6. Conclusion

We developed a single-power-supply, 90-nm, 6T, 2-kbit CMOS SRAM equipped with a newly proposed self-controllable voltage level (SVL) circuit comprising only three MOSFETs. The newly developed (dvlp) SRAM (1) provides larger write and read margins, (2) writes and reads data at low voltages, (3) retains data during standby, and (4) reduces standby power consumption.

The write margin (V_{WM}) and read margin (V_{RM}) of the dvlp SRAM at a supply voltage (V_{DD}) of 1 V are 0.470 V and 0.1923 V, respectively. These values are 1.309 and 2.093 times V_{WM} and V_{RM} of the conv SRAM, respectively.

We showed that the minimum writable supply voltage (V_{MinW}) for conv SRAM is 0.37 V when the threshold voltage (V_t) variability (= +6 σ) is large. Meanwhile, V_{MinW} of the dvlp SRAM drops (improves) appreciably to 0.22 V. The minimum readable supply voltage (V_{MinR}) for conv SRAM is 1.05 V when the V_t variability (= −6 σ) is large. In contrast, V_{MinR} of the dvlp SRAM decreases to 0.41 V. These results demonstrate that the SVL circuit is useful not only for expanding write and read margins but also for further lowering V_{MinW} and V_{MinR}.

The dvlp SRAM significantly reduces the standby power consumption (P_{ST}) without losing data. P_{ST} of the dvlp SRAM measured at V_{DD} = 1 V is only 0.957 μW, which is 9.46% of P_{ST} of the conv SRAM (10.12 μW). We thus find that the SVL circuit not only retains data but also appreciably reduces standby power consumption due to leakage current during standby. Furthermore, the area overhead of the SVL circuit is only 1.383% relative to the total area of the dvlp 2-kbit SRAM.

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