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Programmable Differential Bandgap Reference Circuit for Ultra-Low-Power CMOS LSIs

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SUMMARY This paper describes a programmable differential bandgap reference (PD-BGR) for ultra-low-power IoT (Internet-of-Things) edge node devices. The PD-BGR consists of a current generator (CG) and differential voltage generator (DVG). The CG is based on a bandgap reference (BGR) and generates an operating current and a voltage, while the DVG generates another voltage from the current. A differential voltage reference can be obtained by taking the voltage difference from the voltages. The PD-BGR can produce a programmable differential output voltage by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. Simulation results showed that the proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step within a ±0.7% temperature inaccuracy in a temperature range from -20 to 100°C. A Monte Carlo simulation showed that the coefficient of the variation in the reference was within 1.1%. Measurement results demonstrated that our prototype chips can generate stable programmable differential output voltages, almost the same results as those of the simulation. The average power consumption was only 88.4 nW, with a voltage error of −4/+3 mV with 5 samples.

key words: *Internet-of-Things (IoT), bandgap voltage reference, programmable reference, differential voltage reference*

1. Introduction

Ultra-low-power analog, digital, and mixed-signal CMOS LSIs are strongly required to realize next-generation IoT (Internet-of-Things) edge node devices [1]–[6]. They will have the power to change the world we live in. Voltage references (VRs) are one of basic and important circuit building blocks for processing analog signal information and converting physical information into digital form. They are used in various circuits, such as analog-to-digital Converters (ADCs), digital-to-analog Converters (DACs), power management circuits (PMCs), low-dropout linear regulators (LDOs), and versatile sensor interface circuits. Therefore, we must develop ultra-low power and high precision VRs for such IoT edge node devices.

Various VRs capable of operating with nano-watt (nW) power, or less, have been investigated [7]–[13]. The reference voltages of these VRs are based on the bandgap voltage of silicon (V_{BGR}) [7], [8], threshold voltage (V_{TH}) of a MOSFET [9], [10], and threshold voltage difference (ΔV_{TH}) [11]–[14]. However, almost all of them are realized in a single-ended configuration, so differential or programmable VRs have not been adequately considered. A differential and programmable VR could be useful and advantageous, especially when it must directly interface itself with other differential circuit blocks [15]–[22]. This would lead to a superior noise-immunity and high process-stability for the overall system. In addition, such VRs can be utilized for generating functional and intelligent temperature sensor current [23]–[25]. In the studies, two reference voltages that have a constant voltage difference are required to generate a sensor signal. However, these voltages are supplied from an off-chip voltage source. Thus, an on-chip differential VR is required. Some programmable differential VRs have been reported [19], [20]. However, the generated output voltages are higher than 1 V and power consumption is in the order of several tens of microwatts. Thus, they have difficulties in low-voltage and low-power operation.

In light of this background, we present a low-voltage programmable differential bandgap reference (PD-BGR) with nano-watt (nW) power consumption. The PD-BGR consists of a current generator (CG) and differential voltage generator (DVG) [29]. The CG is based on the bandgap reference (BGR) [7] and generates a reference current and a voltage, and the DVG generates another voltage from the current. A differential voltage reference V_{REFD} can be obtained by taking the voltage difference from these two voltages. Our proposed circuit can also produce a programmable differential voltage V_{REFD} by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. The proposed PD-BGR can generate 25- to 200-mV programmable differential output voltages with a 25-mV step. In contrast to our previous work [29], here, we describe circuit operation in more detail and conduct chip measurements fabricated with a 0.18-μm standard CMOS process technology.

This paper is organized as follows, Sect. 2 presents the proposed PD-BGR, Sect. 3 shows the results of simulations and measurements, and Sect. 4 concludes the paper.

2. Programmable Differential Bandgap Reference

2.1 Characteristics of Subthreshold MOSFET and Bipolar Transistor

Before explaining our proposed PD-BGR architecture and

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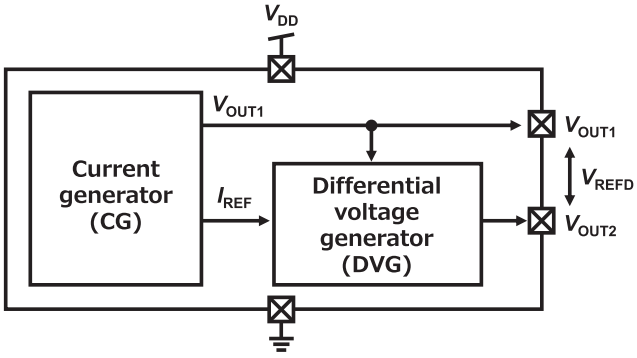

Fig. 1 Block diagram of our proposed differential bandgap reference (©2023 IEEE [29]).

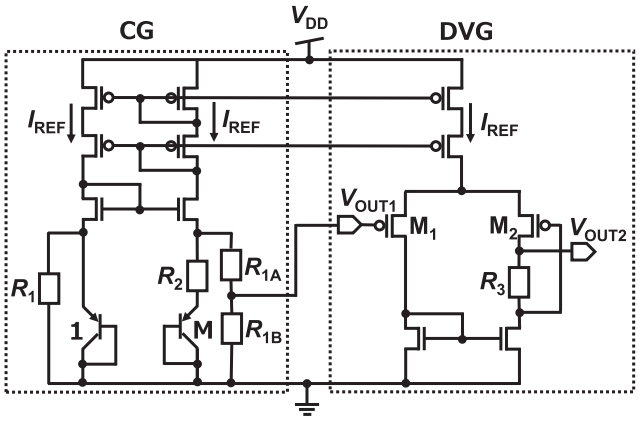

Fig. 2 Schematic of our proposed PD-BGR (©2023 IEEE [29]).

its operation principle, we first briefly summarize the characteristics of the subthreshold current I_D of a MOSFET and base-emitter voltage V_{BE} of a bipolar transistor as follows.

The subthreshold current I_D when the drain-source voltage V_{DS} exceeds 0.1 V is expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{1}$$

where K is the transistor aspect ratio, $I_0 = \mu C_{OX} V_T^2(\eta - 1)$ is a process-dependent parameter, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage ($V_T = k_B T/q$), η is the subthreshold swing parameter, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, V_{GS} is the gate-source voltage, and V_{TH} is the transistor threshold voltage [26].

Regarding the bipolar transistor, in standard CMOS technology, the transistor generates a V_{BE} when it accepts a bias current I_B. The V_{BE} is expressed as

$$V_{BE} = V_T \ln\left(\frac{I_S + I_B}{I_S}\right) \approx V_T \ln\left(\frac{I_B}{I_S}\right), \tag{2}$$

where I_S is the saturation current of a bipolar transistor [26]. For the first order approximation, V_{BE} decreases linearly with the temperature when we use a small temperature dependent bias current I_{BIAS}. Thus, Eq. (2) can be simplified as

$$V_{BE} = V_{BGR} - \gamma T, \tag{3}$$

where V_{BGR} is the bandgap voltage of silicon (i.e., ~1.2 V) and γ is the temperature coefficient of V_{BE}. In actual design, there will be higher order nonlinearities in the V_{BE}, but we consider the nonlinearities to be small compared with the first order temperature characteristics.

2.2 Architecture and Operation Principle

Figure 1 shows a block diagram of our proposed PD-BGR consisting of a current generator (CG) and differential voltage generator (DVG). The CG generates a reference current I_{REF} and voltage V_{OUT1}. The DVG accepts the I_{REF} and V_{OUT1}, and generates V_{OUT2}. A differential voltage reference V_{REFD} can be obtained by taking the voltage difference between V_{OUT1} and V_{OUT2}, or

$$V_{REFD} = V_{OUT2} - V_{OUT1}. \tag{4}$$

Figure 2 shows a schematic of our proposed PD-BGR. To achieve low-power and robust operation, a bandgap reference circuit proposed by *Banba et al.* is used as the CG [7] (start-up circuit is not shown). The area ratio of bipolar transistors Q_1 and Q_2 and resistors R_1, R_{1A}, and R_{1B} are set to $1 : M$ and $R_1 = R_{1A} + R_{1B}$, respectively, as shown in Fig. 2. The current I_{REF} flowing in the CG and the output voltage V_{OUT1} are given by

$$I_{REF} = \frac{V_{BE1}}{R_1} + \frac{V_{BE1} - V_{BE2}}{R_2}, \tag{5}$$

$$V_{OUT1} = \frac{R_{1B}}{R_{1A} + R_{1B}} V_{BE1}. \tag{6}$$

By substituting Eqs. (2) and (3) into Eq. (5), I_{REF} is expressed as

$$I_{REF} = \frac{V_{BGR}}{R_1} - \frac{\gamma T}{R_1} + \frac{V_T \ln(M)}{R_2}. \tag{7}$$

As shown in Eq. (7), the temperature dependence of I_{REF} can be made small because those of the second and third terms are negative and positive, respectively [7].

The DVG accepts the I_{REF} and V_{OUT1} as shown on the right in Fig. 2. The DVG consists of a differential pair circuit M_1–M_2, nMOS current mirror circuit, and resistor R_3. The multipliers of transistors M_1 and M_2 are set to K_1 and K_2, respectively. The current gain of the nMOS current mirror is set to 1 : 1, and thus, currents flowing in transistors M_1 and M_2 become $I_{REF}/2$. Under this condition, the differential output voltage V_{REFD} can be expressed as

$$\begin{aligned} V_{REFD} &= V_{OUT2} - V_{OUT1} \\ &= V_{GS1} - V_{GS2} + R_3 \frac{I_{REF}}{2}, \end{aligned} \tag{8}$$

where V_{GS1} and V_{GS2} are the gate-source voltages of M_1 and M_2, respectively. With Eqs. (1) and (7), the V_{REFD} can be rewritten as

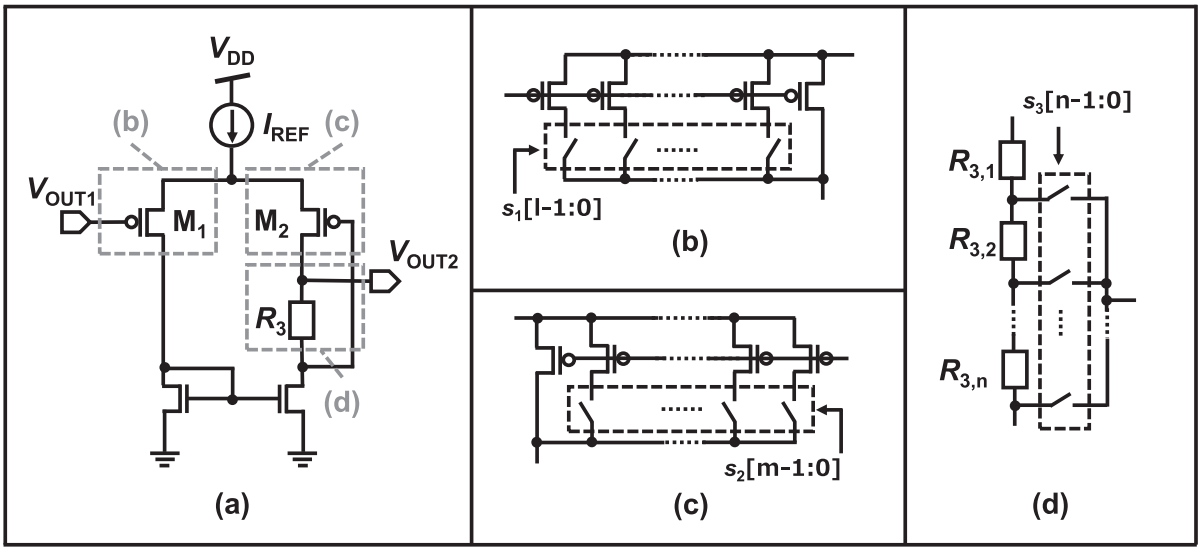

Fig. 3 Schematic of programmable DVG: (a) programmable DVG core, (b) M_1 (l-bit), (c) M_2 (m-bit), and (d) R_3 (n-bit) (©2023 IEEE [29]).

$$\begin{aligned} V_{\mathrm{REFD}} &= V_{\mathrm{TH1}} + \eta V_{\mathrm{T}} \ln\left(\frac{I_{\mathrm{REF}}/2}{K_1 I_0}\right) - V_{\mathrm{TH2}} - \eta V_{\mathrm{T}} \ln\left(\frac{I_{\mathrm{REF}}/2}{K_2 I_0}\right) \\ &\quad + \frac{R_3}{2}\left(\frac{V_{\mathrm{BGR}}}{R_1} - \frac{\gamma T}{R_1} + \frac{V_{\mathrm{T}} \ln(M)}{R_2}\right) \\ &= \frac{R_3}{2R_1} V_{\mathrm{BGR}} + \Delta V_{\mathrm{TH}} - \frac{\gamma R_3}{2R_1} T \\ &\quad + \left\{\eta \ln\left(\frac{K_2}{K_1}\right) + \frac{R_3}{2R_2} \ln(M)\right\} \frac{k_{\mathrm{B}}}{q} T, \end{aligned} \tag{9}$$

where ΔV_{TH} is the threshold voltage difference between M_1 and M_2 in the differential pair and can be ignored when we use large-size MOSFETs and careful design techniques such as a common centroid layout [27]. Thus, Eq. (9) can be simplified to

$$\begin{aligned} V_{\mathrm{REFD}} &= \frac{R_3}{2R_1} V_{\mathrm{BGR}} - \frac{\gamma R_3}{2R_1} T \\ &\quad + \left\{\eta \ln\left(\frac{K_2}{K_1}\right) + \frac{R_3}{2R_2} \ln(M)\right\} \frac{k_{\mathrm{B}}}{q} T. \end{aligned} \tag{10}$$

From Eq. (10), a zero temperature coefficient of V_{REFD} can be obtained by designing the aspect ratios and resistors, or

$$\begin{aligned} \frac{dV_{\mathrm{REFD}}}{dT} &= -\frac{\gamma R_3}{2R_1} + \left\{\eta \ln\left(\frac{K_2}{K_1}\right) + \frac{R_3}{2R_2} \ln(M)\right\} \frac{k_{\mathrm{B}}}{q} \\ &= 0. \end{aligned} \tag{11}$$

Therefore, with the condition where Eq. (11) is satisfied, we obtain temperature compensated V_{REFD} as

$$V_{\mathrm{REFD}} = \frac{R_3}{2R_1} V_{\mathrm{BGR}}. \tag{12}$$

2.3 Programmable DVG

As shown in Eqs. (11) and (12), we can obtain programmable V_{REFD} by changing the ratio of R_1 and R_3 with a combination of R_2, R_3, K_1, K_2, and M. In this work, we design the reference current I_{REF} to be constant (i.e., R_1, R_2, and M are set constant) and then control V_{REFD} by changing K_1, K_2, and R_3 in the DVG.

Figure 3 (a) shows a schematic of a programmable DVG core circuit. The multipliers of M_1 and M_2 and the resistance of R_3 are controlled by digital control signals of $s_1[l-1:0]$, $s_2[m-1:0]$, and $s_3[n-1:0]$. Figures 3 (b), 3 (c), and 3 (d) are detailed schematics of M_1, M_2, and R_3. For M_1 and M_2, the same size transistors are connected or disconnected in parallel using switches and l- and m-bit control signals. With that, we can change the multipliers of M_1 and M_2. For R_3, R_3 is divided into n-th segment resistors, and the appropriate resistance is chosen using switches and n-bit control signals.

3. Results

3.1 Simulation Results

The performance of the proposed PD-BGR was evaluated by SPICE with a set of 0.18-μm standard CMOS process parameters. In this work, the resistors R_1, R_2, $R_{1\mathrm{A}}$, $R_{1\mathrm{B}}$, and M were set to 59.6, 7.05, 32.8, 26.8 MΩ, and 8, respectively. The number of digital control bits was set to $l = 2$, $m = 8$, and $n = 8$. Table 1 lists the design parameters K_1, K_2, and R_3 for the PD-BGR, where K_1 and K_2 are the multipliers of M_1 and M_2.

Figure 4 shows the simulated V_{OUT1} and V_{OUT2} as a function of temperature in the range of –20 to 100°C, when V_{REFD} was set to 100 mV. The voltages decreased as the temperature increased. However, the $V_{\mathrm{REFD}} = V_{\mathrm{OUT2}} - V_{\mathrm{OUT1}}$ was kept almost constant at 100 mV.

Figure 5 shows the simulated V_{REFD}s in the same temperature range. The V_{REFD}s were set to from 25 to 200

Table 1 Design parameters for PD-BGR.

V_{REFD} (mV)	K_1	K_2	R_3 (MΩ)
25	64	78	2.3
50	32	45	4.8
75	64	102	7.3
100	32	59	9.7
125	32	69	12.3
150	64	150	14.9
175	32	89	17.3
200	32	102	19.8

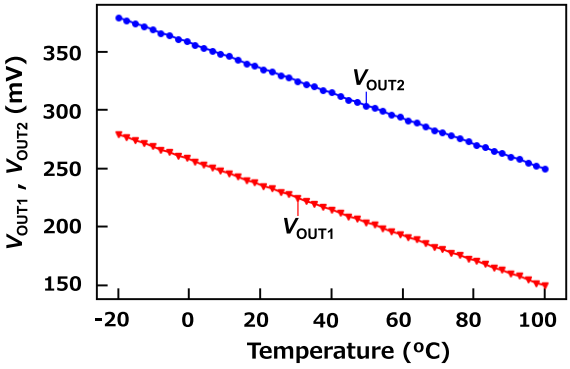

Fig. 4 Simulated V_{OUT1} and V_{OUT2} when V_{REFD} was set to 100 mV (©2023 IEEE [29]).

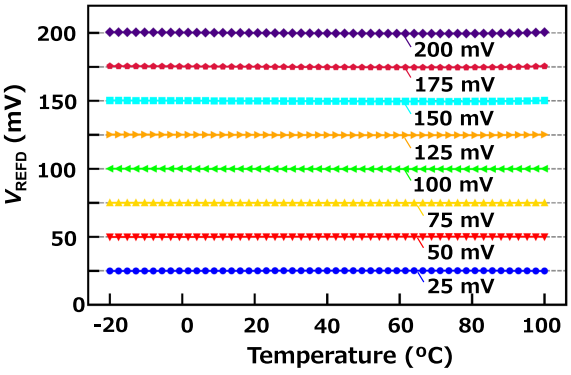

Fig. 5 Simulated programmable V_{REFD}. V_{REFD} was set to 25 – 200 mV with 25-mV step (©2023 IEEE [29]).

mV with a 25-mV step. Almost constant V_{REFD}s were obtained. Figure 6 shows the temperature inaccuracy, derived from Fig. 5. Our PD-BGR achieved high accuracy, within a ±0.7% inaccuracy.

We also performed a Monte Carlo simulation assuming die-to-die (D2D) global variations and within-die (WID) random mismatch variations in all MOSFETs and resistors [27], [28]. The results for 1,000 runs, when the V_{REFD} was set to 100 mV, are depicted in Fig. 7. The average value μ and standard deviation σ of V_{REFD}, in the temperature range from –20 to 100°C were 100 and 0.87 mV, respectively. The coefficient of variation (CV= σ/μ) was 0.87%. Table 2 summarizes the characteristics of the simulated temperature coefficient (TC) and Monte Carlo simulation results of our proposed PD-BGR. In the simulation, we confirmed a highly

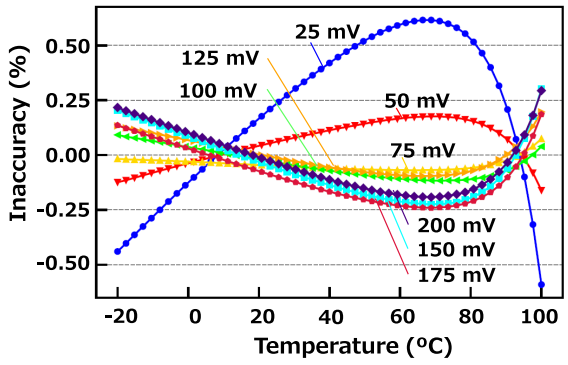

Fig. 6 Temperature inaccuracy of V_{REFD} (©2023 IEEE [29]).

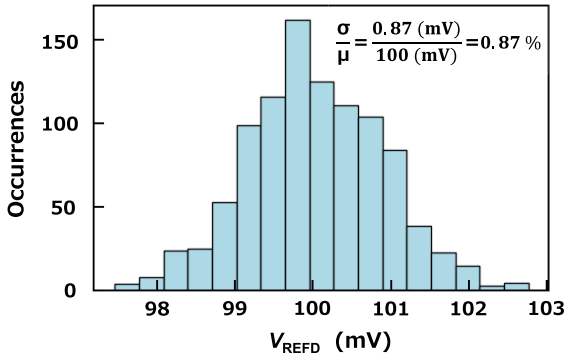

Fig. 7 Distribution of V_{REFD} when V_{REFD} was set to 100 mV, as obtained from Monte Carlo simulation of 1,000 runs (©2023 IEEE [29]).

Table 2 Simulated TC and Monte Carlo simulation results.

V_{REFD} (mV)	TC (ppm/°C)	μ (mV)	σ (mV)	σ/μ(%)
25	100	25.0	0.29	1.10
50	28.1	50.0	0.44	0.88
75	11.9	75.0	0.63	0.83
100	15.8	100	0.87	0.87
125	24.4	125	1.06	0.85
150	44.0	150	1.28	0.86
175	35.6	175	1.48	0.85
200	40.5	200	1.75	0.88

stable PD-BGR, thanks to the reference circuit based on the bandgap voltage reference.

We consider the stability of the PD-BGR. As shown in Eq. (11), the variation of the TC will mainly come from the second term, or the characteristics of the DVG, because the first and third terms are basically stable and determined by the BGR-based CG. To investigate the effect of the process variation on the TC, we performed the Monte Carlo simulation again. Figure 8 shows the simulated average TC with different sizes of unit transistor in the DVG. We set the channel width (W) (μm) and length (L) (μm) of the unit transistor of M1 and M2 as W/L = 1/1, 3/3, and 5/5, respectively. The simulated average TC decreased as the unit transistor size increased. The TC can be made small, 15.8 ppm/°C, when we used the unit transistor size of W/L = 5/5.

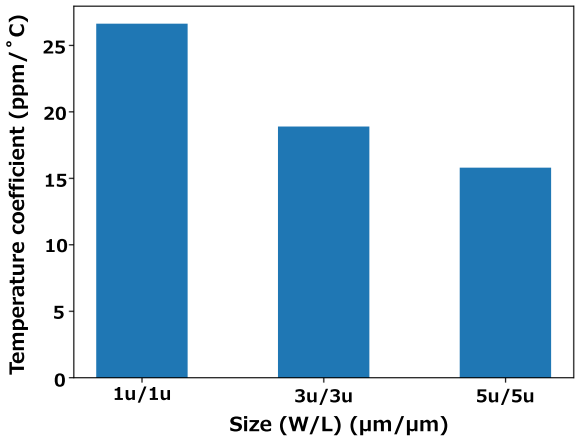

Fig. 8 Simulated average TC with different sizes of unit transistor.

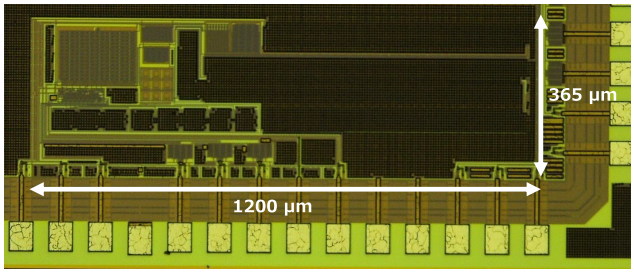

Fig. 9 Chip micrograph.

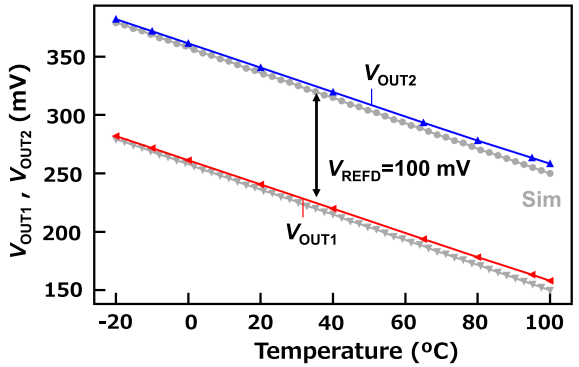

Fig. 10 Measured V_{OUT1} and V_{OUT2} when V_{REFD} was set to 100 mV.

3.2 Measurement Results

The proposed PD-BGR was fabricated with a set of 0.18-μm CMOS process technology. Figure 9 shows the chip micrograph. The total area of our proposed PD-BGR including the digital backend is 0.438 mm^2.

Figure 10 shows the measured V_{OUT1} and V_{OUT2} in the temperature range of –20 to 100°C, when the V_{REFD} was set to 100 mV. We also plotted the simulation results with gray color. The measured output voltages were almost the same as the simulation results, even though the errors from the simulation results increased as the temperature increased. However, the $V_{REFD} = V_{OUT2} - V_{OUT1}$ was kept almost constant at 100 mV. The temperature errors in V_{OUT1} and V_{OUT2} were canceled by the voltage subtraction.

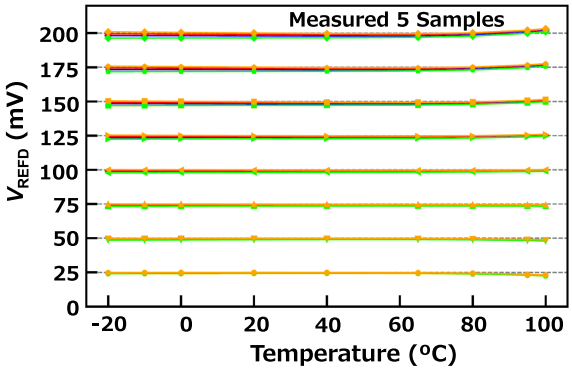

Fig. 11 Measured programmable V_{REFD} as a function of temperature. V_{REFD} was set to 25 – 200 mV with 25-mV step.

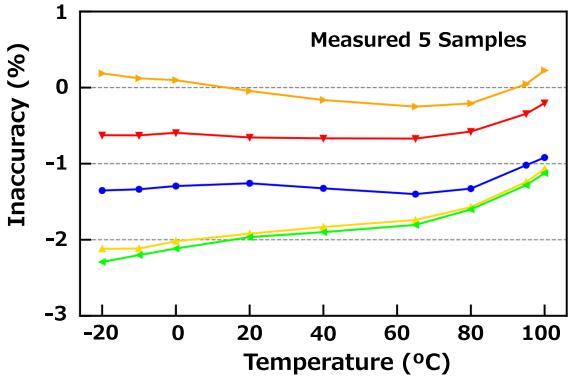

Fig. 12 Measured V_{REFD} inaccuracy as a function of temperature when V_{REFD} was set to 100 mV.

Figure 11 shows the measured V_{REFD} for 5 samples in the same temperature range. As in the simulation, the V_{REFD}s were set to from 25 to 200 mV with a 25-mV step. We obtained almost the same voltages as the simulation results. Figure 12 shows the temperature inaccuracy, when V_{REFD} was set to 100 mV. The inaccuracy was larger than expected (see Fig. 6). This was because of the process variations. However, the absolute value of V_{REFD} and its temperature dependence could be trimmed by the digital control techniques. As discussed in Sect. 2, the output reference voltage V_{REFD} is given by Eq. (12) when Eq. (11) is satisfied. Therefore, the absolute value of V_{REFD} can be trimmed by R_1 and R_3, and its temperature characteristics can be compensated by R_2, K_1, K_2, and M. If we develop binary-weighted control techniques for these parameters, it will be possible to trim the V_{REFD} more accuracy. In this design, we designed the PD-BGR by changing three parameters, K_1, K_2, and R_3, as shown in Table 1. In this case, one possible trimming method is the use of parameters not in use for the V_{REFD} program. That is, trimming of the absolute value and temperature characteristics can be performed by R_1 and R_2, respectively.

Figure 13 shows the measured temperature inaccuracy for all V_{REFD}s. The measured temperature inaccuracy was

kept within ±1% except for V_{REFD} = 25 mV in the temperature range from −20 to 80°C, but became worse at high temperature above 80°C. The reason for the degradation could be leakage current of MOSFETs. The temperature inaccuracy for V_{REFD} = 25 mV was quite large even though the voltage spread of V_{REFD} = 25 mV was comparable to others as shown in Table 3 (see MAX and MIN values in Table 3). One possible reason for this could be that the denominator of the temperature inaccuracy itself was low of V_{REFD} = 25 mV.

Table 3 summarizes the measured V_{REFD}s and TCs for 5 samples. The measured TCs had larger errors than the simulation results. The errors became large when the temperature was over 80°C, or when V_{REFD} was set to 25 mV. When the temperature became over 80°C, leakage current from the body to the source of the MOSFET increased significantly and this caused the voltage errors. The effect of the leakage current could be large for the small V_{REFD} of 25 mV.

Figure 14 shows the measured V_{REFD} as a function of power supply voltage V_{DD} in the range from 1.0 to 1.8 V when V_{REFD} was set to 100 mV. Simulated V_{REFD} was also plotted for comparison. Our proposed circuit can operate at higher than 1.2 V. The line regulation (LR) is given by LR = ΔV_{REFD}(mV)/ΔV_{DD}(V), where ΔV_{REFD} is the reference voltage change in the supply voltage change ΔV_{DD}. The measured LR was 2.64 mV/V. We obtained the stable V_{REFD} in the supply voltage range from 1.2 to 1.8 V.

Table 4 summarizes the characteristics of our PD-BGR in comparison with other CMOS differential BGRs in [14]–[20]. Our proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step. The measured inaccuracy was −4/+3 mV for 5 samples. The power consumption is the lowest, 88.4 nW. These significant achievements come from our proposed voltage reference architecture. As shown in Eq. (10), the reference voltage V_{REFD} can be obtained by not only the conventional bandgap voltage reference circuit architecture, but also the proposed differential pair circuit consisting of MOSFETs operating in the subthreshold region. By using these, we can obtain compact and low-voltage programmable output reference voltages with nanowatt power consumption.

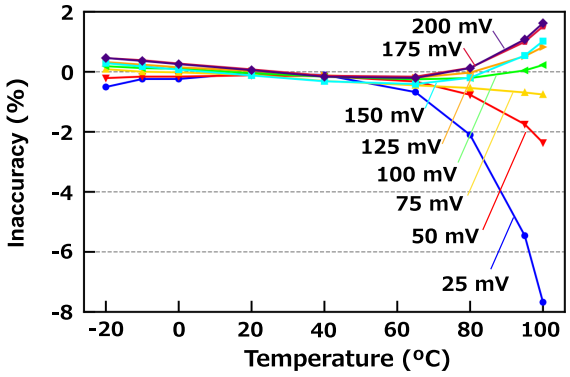

Fig. 13 Measured temperature inaccuracy of V_{REFD}s as a function of temperature

Table 3 Measured V_{REFD}s and TCs among 5 samples.

V_{REFD} (mV)	Measured V_{REFD} (mV)				TC (ppm/°C)		
	μ	σ	MAX	MIN	μ	MAX	MIN
25	24.1	0.31	25.0	22.3	688	753	649
50	49.0	0.45	49.9	47.9	191	213	176
75	73.9	0.60	75.1	73.1	46.7	70.5	31.8
100	98.9	0.78	100	97.7	61.5	99.1	39.1
125	124	0.96	126	122	111	144	85.1
150	149	1.09	152	147	136	156	119
175	174	1.27	178	172	162	188	139
200	199	1.43	203	196	176	200	152

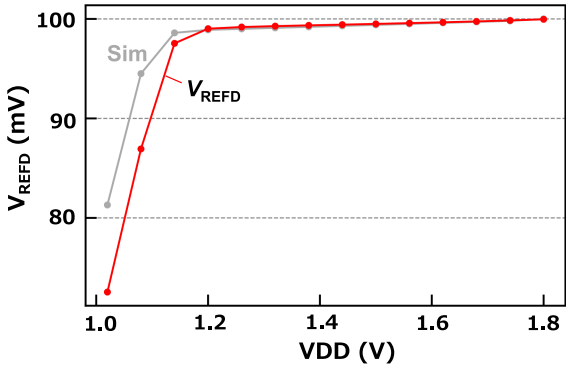

Fig. 14 Measured V_{REFD} as a function of power supply voltage V_{DD} when V_{REFD} was set to 100 mV.

Table 4 Performance summary and comparison.

Ref.	[15]	[16]	[17]	[14]	[18]	[19]	[20]	This work
Tech. (μm)	2.0	0.65	0.25	0.35	0.18	0.18	0.18	0.18
V_{DD}	5	5	2.5	1.5	0.9 - 1.8	1.5, 2.2, 2.95	3.3	1.2 - 1.8
Temp. (°C)	0 - 100	–	–50 - 150	–20 - 100	–20 - 115	–50 - 140	5 - 85	–20 - 100
Programmable	NO	NO	NO	NO	NO	YES	YES	YES
V_{REFD} (V)	2.48	2.01	1.01	0.01	0.315	1.22 / 2.00 / 2.80	1.25 / 2.05 / 2.88	25.0 - 200 mV (25-mV step)
σ (mV)	24	5.5	NA	NA	NA	±5, ±7, ±11	0.8 / 2 / 2.5	(see Tab. 3)
Power	6 mW	2.2 mW	0.98 mW	4.6 μW	36 μW	63 μA†	50 μA†	88.4 nW††
TC (ppm/°C)	20.9	115	20	25	89.3	28 / 36 / 38	<13 / 38 / 38	(see Tabs. 2 and 3)
LR (mV/V)†††	0.45	NA	NA	NA	2.9	NA	NA	2.64††
Meas./Sim.	Meas.	Meas.	Sim.	Sim.	Meas.	Sim.	Meas.	Meas.

†: Supply current, ††: Average of 5 samples, †††:LR : Line Regulation

4. Conclusion

We presented a PD-BGR consisting of a CG and DVG. The CG generates a current and a voltage, while the DVG generates another voltage from the current. A differential reference voltage can be obtained by taking the voltage difference from the voltages. The PD-BGR can produce a programmable differential output voltage by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. Simulation results showed that our proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step within a ±0.7% inaccuracy in a temperature range from -20 to 100°C. A Monte Carlo simulation showed that our circuit was robust against process variation and that the CV of the V_{REFD} was less than 1.1%. Measurement results demonstrated that our prototype chips can generate stable programmable differential output voltages. The average power consumption was only 88.4 nW, with a voltage error of $-4/+3$ mV with 5 samples.

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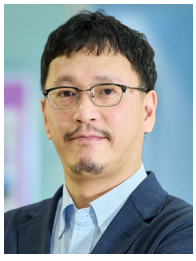

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