on Electronics

DOI: 10.1587/transele.2023CTP0004

Publicized: 2024/04/09

This advance publication article will be replaced by the finalized version after proofreading.
Programmable Differential Bandgap Reference Circuit for Ultra-Low-Power CMOS LSIs

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SUMMARY This paper describes a programmable differential bandgap reference (PD-BGR) for ultra-low-power IoT (Internet-of-Things) edge node devices. The PD-BGR consists of a current generator (CG) and differential voltage generator (DVG). The CG is based on a bandgap reference (BGR) and generates an operating current and a voltage, while the DVG generates another voltage from the current. A differential voltage reference can be obtained by taking the voltage difference from the voltages. The PD-BGR can produce a programmable differential output voltage by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. Simulation results showed that the proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step within a ±0.7% temperature inaccuracy in a temperature range from -20 to 100°C. A Monte Carlo simulation showed that the coefficient of the variation in the reference was within 1.1%. Measurement results demonstrated that our prototype chips can generate stable programmable differential output voltages, almost the same results as those of the simulation. The average power consumption was only 88.4 nW, with a voltage error of -4/+3 mV with 5 samples.

1. Introduction

Ultra-low-power analog, digital, and mixed-signal CMOS LSIs are strongly required to realize next-generation IoT (Internet-of-Things) edge node devices [1]–[6]. They will have the power to change the world we live in. Voltage references (VRs) are one of basic and important circuit building blocks for processing analog signal information and converting physical information into digital form. They are used in various circuits, such as analog-to-digital Converters (ADCs), digital-to-analog Converters (DACs), power management circuits (PMCs), low-dropout linear regulators (LDOs), and versatile sensor interface circuits. Therefore, we must develop ultra-low power and high precision VRs for such IoT edge node devices.

Various VRs capable of operating with nano-watt (nW) power, or less, have been investigated [7]–[13]. The reference voltages of these VRs are based on the bandgap voltage of silicon (VREF_BG) [7], [8], threshold voltage (VT) of a MOSFET [9], [10], and threshold voltage difference (ΔVT) [11]–[14]. However, almost all of them are realized in a single-ended configuration, so differential or programmable VRs have not been adequately considered. A differential and programmable VR could be useful and advantageous, especially when it must directly interface itself with other differential circuit blocks [15]–[22]. This would lead to a superior noise-immunity and high process-stability for the overall system. In addition, such VRs can be utilized for generating functional and intelligent temperature sensor current [23]–[25]. In the studies, two reference voltages that have a constant voltage difference are required to generate a sensor signal. However, these voltages are supplied from an off-chip voltage source. Thus, an on-chip differential VR is required. Some programmable differential VRs have been reported [19], [20]. However, the generated output voltages are higher than 1 V and power consumption is in the order of several tens of microwatts. Thus, they have difficulties in low-voltage and low-power operation.

In light of this background, we present a low-voltage programmable differential bandgap reference (PD-BGR) with nano-watt (nW) power consumption. The PD-BGR consists of a current generator (CG) and differential voltage generator (DVG) [29]. The CG is based on the bandgap reference (BGR) [7] and generates a reference current and a voltage, and the DVG generates another voltage from the current. A differential voltage reference VREF can be obtained by taking the voltage difference from these two voltages. Our proposed circuit can also produce a programmable differential voltage VREF by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. The proposed PD-BGR can generate 25- to 200-mV programmable differential output voltages with a 25-mV step. In contrast to our previous work [29], here, we describe circuit operation in more detail and conduct chip measurements fabricated with a 0.18-μm standard CMOS process technology.

This paper is organized as follows, Sect. 2 presents the proposed PD-BGR, Sect. 3 shows the results of simulations and measurements, and Sect. 4 concludes the paper.

2. Programmable Differential Bandgap Reference

2.1 Characteristics of Subthreshold MOSFET and Bipolar Transistor

Before explaining our proposed PD-BGR architecture and its operation principle, we first briefly summarize the characteristics of the subthreshold current ID of a MOSFET and
base-emitter voltage $V_{BE}$ of a bipolar transistor as follows.

The subthreshold current $I_D$ when the drain-source voltage $V_{DS}$ exceeds 0.1 V is expressed as

$$I_D = K I_0 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right).$$

where $K$ is the transistor aspect ratio, $I_0 = \mu C_{ox} V_T^2 (\eta - 1)$ is a process-dependent parameter, $\mu$ is the carrier mobility, $C_{ox}$ is the gate-oxide capacitance, $V_T$ is the thermal voltage, $V_T = k_B T / q$, $\eta$ is the subthreshold swing parameter, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the elementary charge, $V_{GS}$ is the gate-source voltage, and $V_{TH}$ is the transistor threshold voltage [26].

Regarding the bipolar transistor, in standard CMOS technology, the transistor generates a $V_{BE}$ when it accepts a bias current $I_B$. The $V_{BE}$ is expressed as

$$V_{BE} = V_T \ln \left( \frac{I_S + I_B}{I_S} \right) = V_T \ln \left( \frac{I_B}{I_S} \right),$$

where $I_S$ is the saturation current of a bipolar transistor [26]. For the first order approximation, $V_{BE}$ decreases linearly with the temperature when we use a small temperature dependent bias current $I_{BIAS}$. Thus, Eq. 2 can be simplified as

$$V_{BE} = V_{BGR} - \gamma T,$$

where $V_{BGR}$ is the bandgap voltage of silicon (i.e., ~1.2 V) and $\gamma$ is the temperature coefficient of $V_{BE}$. In actual design, there will be higher order nonlinearities in the $V_{BE}$, but we consider the nonlinearities to be small compared with the first order temperature characteristics.

### 2.2 Architecture and Operation Principle

Figure 1 shows a block diagram of our proposed PD-BGR consisting of a current generator (CG) and differential voltage generator (DVG). The CG generates a reference current $I_{REF}$ and voltage $V_{OUT1}$. The DVG accepts the $I_{REF}$ and $V_{OUT1}$, and generates $V_{OUT2}$. A differential voltage reference $V_{REFD}$ can be obtained by taking the voltage difference between $V_{OUT1}$ and $V_{OUT2}$, or

$$V_{REFD} = V_{OUT2} - V_{OUT1}.$$  

(4)

Figure 2 shows a schematic of our proposed PD-BGR. To achieve low-power and robust operation, a bandgap reference circuit proposed by Banha et al. is used as the CG [7] (start-up circuit is not shown). The area ratio of bipolar transistors Q1 and Q2 and resistors $R_1$, $R_{1A}$, and $R_{1B}$ are set to $1 : M$ and $R_1 = R_{1A} + R_{1B}$, respectively, as shown in Figure 2. The current $I_{REF}$ flowing in the CG and the output voltage $V_{OUT1}$ are given by

$$I_{REF} = \frac{V_{BE1} + V_{BE2} - V_{BE}}{R_1},$$

$$V_{OUT1} = \frac{V_{BE1} - R_{1B}}{R_{1A} + R_{1B}} R_{1B}.$$  

(5)

(6)

By substituting Eqs. 2 and 3 into Eq. 5, $I_{REF}$ is expressed as

$$I_{REF} = \frac{V_{BGR}}{R_1} - \gamma T + \frac{V_T \ln(M)}{R_2}.$$  

(7)

As shown in Eq. 7, the temperature dependence of $I_{REF}$ can be made small because those of the second and third terms are negative and positive, respectively [7].

The DVG accepts the $I_{REF}$ and $V_{OUT1}$ as shown on the right in Figure 2. The DVG consists of a differential pair circuit $M_1$-$M_2$, nMOS current mirror circuit, and resistor $R_3$. The multipliers of transistors $M_1$ and $M_2$ are set to $K_1$ and $K_2$, respectively. The current gain of the nMOS current mirror is set to $1 : 1$, and thus, currents flowing in transistors $M_1$ and $M_2$ become $I_{REF}/2$. Under this condition, the differential output voltage $V_{REFD}$ can be expressed as

$$V_{REFD} = V_{OUT2} - V_{OUT1} = \frac{V_{GS1} - V_{GS2} + R_3 I_{REF}}{2},$$  

(8)

where $V_{GS1}$ and $V_{GS2}$ are the gate-source voltages of $M_1$ and $M_2$, respectively. With Eqs. 1 and 7, the $V_{REFD}$ can be rewritten as

$$V_{REFD} = V_{TH1} + \eta V_T \ln \left( \frac{I_{REF}/2}{K_1 I_0} \right) - V_{TH2} - \eta V_T \ln \left( \frac{I_{REF}/2}{K_2 I_0} \right).$$
As shown in Eqs. 11 and 12, we can obtain programmable $V_{\text{REFD}}$ by changing the ratio of $R_1$ and $R_3$ with a combination of $R_2$, $R_3$, $K_1$, $K_2$, and $M$. In this work, we design the reference current $I_{\text{REF}}$ to be constant (i.e., $K_1$, $R_2$, and $M$ are set constant) and then control $V_{\text{REFD}}$ by changing $K_1$, $K_2$, and $R_3$ in the DVG.

Figure 3(a) shows a schematic of a programmable DVG core circuit. The multipliers of $M_1$ and $M_2$ and the resistance of $R_3$ are controlled by digital control signals of $s_1[1-0]$, $s_2[m-1:0]$, and $s_3[n-1:0]$. Figures 3(b), 3(c), and 3(d) are detailed schematics of $M_1$, $M_2$, and $R_3$. For $M_1$ and $M_2$, the same size transistors are connected or disconnected in parallel using switches and $l$- and $m$-bit control signals. With that, we can change the multipliers of $M_1$ and $M_2$. For $R_3$, $R_3$ is divided into $n$-th segment resistors, and the appropriate resistance is chosen using switches and $n$-bit control signals.

### 3. Results

#### 3.1 Simulation results

The performance of the proposed PD-BGR was evaluated by SPICE with a set of 0.18-μm standard CMOS process parameters. In this work, the resistors $R_1$, $R_2$, $R_{1A}$, $R_{1B}$, and $M$ were set to 59.6, 7.05, 32.8, 26.8 Ω, and 8, respectively. The number of digital control bits was set to $l = 2$, $m = 8$, and $n = 8$. Table 1 lists the design parameters $K_1$, $K_2$, and $R_3$ for the PD-BGR, where $K_1$ and $K_2$ are the multipliers of
M₁ and M₂.

Figure 4 shows the simulated VOUT₁ and VOUT₂ as a function of temperature in the range of −20 to 100°C, when VREFD was set to 100 mV. The voltages decreased as the temperature increased. However, the VREFD = VOUT₂ − VOUT₁ was kept almost constant at 100 mV.

Figure 5 shows the simulated VREFD in the same temperature range. The VREFD were set to from 25 to 200 mV with a 25-mV step. Almost constant VREFD were obtained. Figure 6 shows the temperature inaccuracy, derived from Figure 5. Our PD-BGR achieved high accuracy, within a ±0.7% inaccuracy.

We also performed a Monte Carlo simulation assuming die-to-die (D2D) global variations and within-die (WID) random mismatch variations in all MOSFETs and resistors [27], [28]. The results for 1,000 runs, when the VREFD was set to 100 mV, are depicted in Figure 7. The average value μ and standard deviation σ of VREFD, in the temperature range from −20 to 100°C were 100 and 0.87 mV, respectively. The coefficient of variation (CV = σ/μ) was 0.87%. Table 2 summarizes the characteristics of the simulated temperature coefficient (TC) and Monte Carlo simulation results of our proposed PD-BGR. In the simulation, we confirmed a highly stable PD-BGR, thanks to the reference circuit based on the bandgap voltage reference.

![Figure 4](image1)

![Figure 5](image2)

![Figure 6](image3)

![Figure 7](image4)

Table 2: Simulated TC and Monte Carlo simulation results.

<table>
<thead>
<tr>
<th>VREFD (mV)</th>
<th>TC (ppm/°C)</th>
<th>μ (mV)</th>
<th>σ (mV)</th>
<th>σ/μ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>100</td>
<td>250</td>
<td>0.29</td>
<td>1.10</td>
</tr>
<tr>
<td>50</td>
<td>28.3</td>
<td>500</td>
<td>0.44</td>
<td>0.88</td>
</tr>
<tr>
<td>75</td>
<td>11.9</td>
<td>750</td>
<td>0.63</td>
<td>0.83</td>
</tr>
<tr>
<td>100</td>
<td>15.8</td>
<td>1000</td>
<td>0.87</td>
<td>0.87</td>
</tr>
<tr>
<td>125</td>
<td>24.4</td>
<td>125</td>
<td>1.06</td>
<td>0.85</td>
</tr>
<tr>
<td>150</td>
<td>44.0</td>
<td>150</td>
<td>1.28</td>
<td>0.86</td>
</tr>
<tr>
<td>175</td>
<td>35.6</td>
<td>175</td>
<td>1.48</td>
<td>0.85</td>
</tr>
<tr>
<td>200</td>
<td>40.5</td>
<td>200</td>
<td>1.75</td>
<td>0.88</td>
</tr>
</tbody>
</table>

We consider the stability of the PD-BGR. As shown in Eq. 11, the variation of the TC will mainly come from the second term, or the characteristics of the DVG, because the first and third terms are basically stable and determined by the BGR-based CG. To investigate the effect of the process variation on the TC, we performed the Monte Carlo simulation again. Figure 8 shows the simulated average TC with different sizes of unit transistor in the DVG. We set the channel width (W) (μm) and length (L) (μm) of the unit transistor of M₁ and M₂ as W/L = 1/1, 3/3, and 5/5, respectively. The simulated average TC decreased as the unit transistor size increased. The TC can be made small, 15.8 ppm/°C, when we used the unit transistor size of W/L = 5/5.
3.2 Measurement results

The proposed PD-BGR was fabricated with a set of 0.18-μm CMOS process technology. Figure 9 shows the chip micrograph. The total area of our proposed PD-BGR including the digital backend is 0.438 mm².

Figure 10 shows the measured \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) in the temperature range of −20 to 100°C, when the \( V_{\text{REFD}} \) was set to 100 mV. We also plotted the simulation results with gray color. The measured output voltages were almost the same as the simulation results, even though the errors from the simulation results increased as the temperature increased. However, the \( V_{\text{REFD}} = V_{\text{OUT2}} - V_{\text{OUT1}} \) was kept almost constant at 100 mV. The temperature errors in \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) were canceled by the voltage subtraction.

Figure 11 shows the measured \( V_{\text{REFD}} \) for 5 samples in the same temperature range. As in the simulation, the \( V_{\text{REFD}} \)s were set to from 25 to 200 mV with a 25-mV step. We obtained almost the same voltages as the simulation results. Figure 12 shows the temperature inaccuracy, when \( V_{\text{REFD}} \) was set to 100 mV. The inaccuracy was larger than expected (see Fig. 6). This was because of the process variations. However, the absolute value of \( V_{\text{REFD}} \) and its temperature dependence could be trimmed by the digital control techniques. As discussed in Sect. 2, the output reference voltage \( V_{\text{REFD}} \) is given by Eq. 12 when Eq. 11 is satisfied. Therefore, the absolute value of \( V_{\text{REFD}} \) can be trimmed by \( R_1 \) and \( R_3 \), and its temperature characteristics can be compensated by \( R_2, K_1, K_2 \), and \( M \). If we develop binary-weighted control techniques for these parameters, it will be possible to trim the \( V_{\text{REFD}} \) more accurately. In this design, we designed the PD-BGR by changing three parameters, \( K_1, K_2 \), and \( R_3 \), as shown in Tab. 1. In this case, one possible trimming method is the use of parameters not in use for the \( V_{\text{REFD}} \) program. That is, trimming of the absolute value and temperature characteristics can be performed by \( R_1 \) and \( R_2 \), respectively.

Figure 13 shows the measured temperature inaccuracy for all \( V_{\text{REFD}} \). The measured temperature inaccuracy was
kept within ±1% except for $V_{\text{REFD}} = 25$ mV in the temperature range from 20 to 80°C, but became worse at high temperature above 80°C. The reason for the degradation could be leakage current of MOSFETs. The temperature inaccuracy for $V_{\text{REFD}} = 25$ mV was quite large even though the voltage spread of $V_{\text{REFD}}$ was comparable to others as shown in Tab. 3 (see MAX and MIN values in Tab. 3). One possible reason for this could be that the denominator of the temperature inaccuracy itself was low of $V_{\text{REFD}} = 25$ mV.

Table 3 summarizes the measured $V_{\text{REFD}}$s and TCs for 5 samples. The measured TCs had larger errors than the simulation results. The errors became large when the temperature was over 80°C, or when $V_{\text{REFD}}$ was set to 25 mV. When the temperature became over 80°C, leakage current from the body to the source of the MOSFET increased significantly and this caused the voltage errors. The effect of the leakage current could be large for the small $V_{\text{REFD}}$ of 25 mV.

Figure 14 shows the measured $V_{\text{REFD}}$ as a function of power supply voltage $V_{\text{DD}}$ in the range from 1.0 to 1.8 V when $V_{\text{REFD}}$ was set to 100 mV. Simulated $V_{\text{REFD}}$ was also plotted for comparison. Our proposed circuit can operate at higher than 1.2 V. The line regulation (LR) is given by $LR = \Delta V_{\text{REFD}}(\text{mV})/\Delta V_{\text{DD}}(\text{V})$, where $\Delta V_{\text{REFD}}$ is the reference voltage change in the supply voltage change $\Delta V_{\text{DD}}$. The measured LR was 2.64 mV/V. We obtained the stable $V_{\text{REFD}}$ in the supply voltage range from 1.2 to 1.8 V.

Table 3 summarizes the characteristics of our PD-BGR in comparison with other CMOS differential BGRs in [14]–[20]. Our proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step. The measured inaccuracy was $-4/+3$ mV for 5 samples. The power consumption is the lowest, 88.4 nW. These significant achievements come from our proposed voltage reference architecture. As shown in Eq. 10, the reference voltage $V_{\text{REFD}}$ can be obtained by not only the conventional bandgap voltage reference circuit architecture, but also the proposed differential pair circuit consisting of MOSFETs operating in the subthreshold region. By using these, we can obtain compact and low-voltage programmable output reference voltages with nano-watt power consumption.

4. Conclusion

We presented a PD-BGR consisting of a CG and DVG. The CG generates a current and a voltage, while the DVG generates another voltage from the current. A differential reference voltage can be obtained by taking the voltage difference from the voltages. The PD-BGR can produce a programmable differential output voltage by changing the multipliers of MOSFETs in a differential pair and resistance with digital codes. Simulation results showed that our proposed PD-BGR can generate 25- to 200-mV reference voltages with a 25-mV step within a ±0.7% inaccuracy in a temperature range from -20 to 100°C. A Monte Carlo simulation showed that our circuit was robust against process variation and that the CV of the $V_{\text{REFD}}$ was less than 1.1%. Measurement results demonstrated that our prototype chips can generate stable programmable differential output voltages. The average power consumption was only 88.4 nW, with a voltage error of $-4/+3$ mV with 5 samples.

Acknowledgments

This work was supported through the activities of VDEC, the University of Tokyo, in collaboration with Cadence Design Systems and Mentor Graphics. This work was also partly supported by JSPS KAKENHI Grant Numbers JP20H00606, JP22H03558, JP23H03364, and JST Grant Number JP-MJPF2106.
Table 4 Performance summary and comparison.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (μm)</th>
<th>VDD (V)</th>
<th>Temp. (°C)</th>
<th>VREF (V)</th>
<th>σ (mV)</th>
<th>Power (mW)</th>
<th>TC (ppm/°C)</th>
<th>LR (mV/°C)</th>
</tr>
</thead>
<tbody>
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<td>[15]</td>
<td>2.0</td>
<td>0.65</td>
<td>0.25</td>
<td>0.35</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
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<tr>
<td>[16]</td>
<td>5</td>
<td>2</td>
<td>2.5</td>
<td>1.5</td>
<td>0.9 - 1.8</td>
<td>1.5, 2.2, 2.95</td>
<td>3.3</td>
<td>1.2 - 1.8</td>
</tr>
<tr>
<td>[17]</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>[18]</td>
<td>2.48</td>
<td>2.01</td>
<td>1.01</td>
<td>0.01</td>
<td>0.315</td>
<td>1.22 / 2.00 / 2.80</td>
<td>1.25 / 2.05 / 2.88</td>
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</tr>
<tr>
<td>[19]</td>
<td>24</td>
<td>5.5</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>±5, ±7, ±11</td>
<td>0.8 / 2.7 / 2.5</td>
<td>(see Tab. 3)</td>
</tr>
<tr>
<td>[20]</td>
<td>6 mW</td>
<td>2.2 mW</td>
<td>0.98 mW</td>
<td>4.6 μW</td>
<td>36 μW</td>
<td>63 μA†</td>
<td>50 μA†</td>
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<td>115</td>
<td>20</td>
<td>25</td>
<td>89.3</td>
<td>28 / 36 / 38</td>
<td>&lt;13 / 38 / 38</td>
<td>(see Tabs. 2 and 3)</td>
</tr>
</tbody>
</table>

†† Supply current, ††† Average of 5 samples, †† LR : Line Regulation

References


[8] Y. Osaki, T. Hirose, N. Kuroki and M. Numa, “A 1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.5-V sub-bandgap reference circuits for nanowatt CMOS LSIs,” IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 1530-1538, June 2013. DOI: 10.1109/JSSC.2013.225253.


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