Sub-60-mV Charge Pump and its Driver Circuit for Extremely Low-Voltage Thermoelectric Energy Harvesting

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SUMMARY   Extremely low-voltage charge pump (ELV-CP) and its dedicated multi-stage driver (MS-DRV) for sub-60-mV thermoelectric energy harvesting are proposed. The proposed MS-DRV utilizes the output voltages of each ELV-CP to efficiently boost the control clock signals. The boosted clock signals are used as switching signals for each ELV-CP and MS-DRV to turn switch transistors on and off. Moreover, reset transistors are added to the MS-DRV to ensure an adequate non-overlapping period between switching signals. Measurement results demonstrated that the proposed MS-DRV can generate boosted clock signals of 350 mV from input voltage of 60 mV. The ELV-CP can boost the input voltage of 100 mV with 10.7% peak efficiency. The proposed ELV-CP and MS-DRV can boost the low input voltage of 56 mV.
key words: energy harvesting, power management circuit, voltage boost converter, cold-start circuit, start-up circuit, charge pump, driver circuit

1. Introduction

A large number of IoT (Internet of Things) edge node devices connected to the network will be installed everywhere. They will be an up-and-coming intelligent communication platform for collecting and delivering information throughout the world. However, maintenance and replacement of the batteries of these battery-powered devices are crucial issues. To address those issues, energy harvesting has attracted extensive attention as an autonomous energy sources for IoT edge node devices [1]–[7].

Thermoelectric generators (TEGs) can generate electrical energy from a slight difference in temperature. However, output voltage of a TEG, V_{TEG}, is too low to operate LSI systems and sensors when temperature difference is a few degrees (e.g., V_{TEG}s are less than several tens of millivolts). An ultra-low-power and highly efficient power-management circuit (PMC) is therefore required [3]–[9].

Figure 1 shows a block diagram of a PMC using a TEG energy harvester. The PMC consists of a voltage-boost converter (VBC) and a cold-start subcircuit. The cold-start subcircuit must operate at low voltage V_{IN} and generate control signals for the VBC. For that purpose, a multi-stage charge pump (CP) and its driver (DRV) circuit are extensively used to convert low V_{IN} to a higher output voltage [10]–[21]. However, the control signals generated by the driver significantly
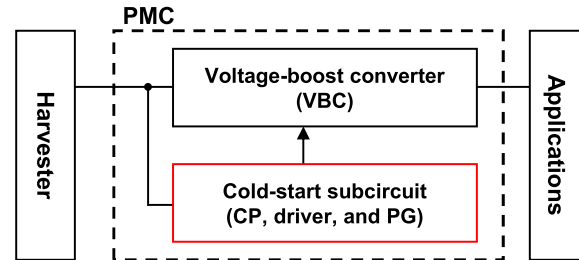
Fig. 1   Power management circuit for low-voltage energy harvesting (©2022 IEEE [24]).

degrade as V_{IN} decreases; therefore, the conventional multi-stage CP cannot generate a sufficient output voltage when V_{IN} is low. Appropriate control signals cannot be obtained even though multi-stage drivers are connected in cascade.

To solve the above-described problem, we propose an extremely low-voltage CP (ELV-CP) and its dedicated multi-stage driver (MS-DRV) for sub-60-mV energy harvesting. The proposed MS-DRV utilizes the output voltages of each ELV-CP to efficiently boost control signals. The boosted clock signals are used as switching signals for each ELV-CP and MS-DRV to turn switch transistors on and off at low V_{IN} [22], [23]. Moreover, reset transistors are added to the MS-DRV to ensure an adequate non-overlapping (NOL) period between switching signals. In contrast to our previous work [24], we add some simulation results and discuss its circuit operation in more detail. In addition, we fabricate a proof-of-concept chip using a 180-nm CMOS process and demonstrate the effectiveness of our proposed circuits. The proposed ELV-CP and MS-DRV can operate at extremely low V_{IN} of 56 mV.

This paper is organized as follows: Section 2 briefly describes conventional CP and DRV and explains the issues concerning them; Section 3 presents the proposed ELV-CP and MS-DRV; Section 4 shows the results of simulations; Section 5 discusses the results of measurements; and Sect. 6 concludes the paper.

2. Conventional CP and DRV

Figure 2 shows a block diagram of conventional CP and its DRV [25], [26]. A high voltage-conversion ratio (VCR) can be realized by connecting *n*-stage CPs in cascade. For the multi-stage CP, a DRV is required to turn the switch transistors in the CPs on and off. As shown in Fig. 2, the boosted clock signals can also be generated by connecting

n-stage DRVs in cascade.

It should be noted that it is difficult to obtain higher boosted clock signals because the voltage-boost ratio of the *n*-stage DRVs is limited by $n + 1$. In addition, conventional CPs use a 4-phase clock generator, which consists of a NOL clock generator and some logic gates, to control the switch transistors in the DRVs [25], [26]. However, when the clock signals are applied to the DRVs, the timing of the signals is delayed, so a multi-stage DRV cannot generate NOL boosted clock signals. The number of the drivers is therefore limited to less than 3 or 4; thus, higher clock signals cannot be obtained stably.

Note that a conventional DRV cannot operate correctly with NOL clock signals. Figure 3 shows schematics of a conventional driver [26] and its operation when NOL clock signals are both low, namely, $\varphi_{P0} = \varphi_{N0} = 0$, and its time chart. Under the condition, both of the top potentials of C_1 and C_2 are V_{IN}, and PMOS switch transistors M3 and M4 are turned on, as shown in Fig. 3 (b) (in which switch transistors colored in gray are turned off). Therefore, both output voltages become V_{IN}. In other words, the NOL period of the output voltages cannot be obtained when $\varphi_{P0} = \varphi_{N0} = 0$, so operation of the multi-stage DRV circuit fails. Consequently, a 4-phase clock generator is conventionally used to control

switching timing [25], [26].

To solve the above-described problems, a low-voltage CP and DRV are proposed and described in detail in the next section.

3. Proposed ELV-CP and MS-DRV

Figure 4 shows a block diagram of the proposed ELV-CP and its MS-DRV. The proposed circuits are based on the conventional one, except the DRV is modified to generate higher-boosted clock signals with adequate NOL period [26]. Note that a dual-input and dual-output CP as reported in [27] is used, and the output voltages of the CP change between V_{IN} and $2V_{IN}$ alternately, as shown in Fig. 5. A conventional rectifier (RECT) is used to obtain the output voltage V_{OUT} [27].

Differing from the conventional design, the proposed MS-DRV accepts output voltages of each CP to boost the control signals, as shown in Fig. 4. Voltage-boost ratio of the *n*-stage MS-DRV can therefore be increased to 2^n, which is much higher than the conventional design of $n + 1$. In addition, each MS-DRV accepts the boosted clock signals φ_{Pn} and φ_{Nn} to improve the performance of the switch transistors in the MS-DRV.

Figure 6 shows a schematic of the first stage of the proposed MS-DRV. Input NOL signals φ_{P0} and φ_{N0} are applied to the MS-DRV, and boosted NOL signals φ_{P1} and φ_{N1} are then generated. The output voltages of CP_1 are applied to V_{INP1} and V_{INN1}. They determine the voltage-boost ratio of φ_{P1} and φ_{N1}. The boost ratio is determined by one of the two CP's output voltages. In this design, we use a lower output voltage of the CP's output voltages because the leakage loss increases when the higher output voltage is used. Boosted control signals φ_{Pn} and φ_{Nn} are applied to the MS-DRV in opposite-phase relation, as shown in Fig. 6.

Figure 7 illustrates operation of the proposed MS-DRV and its time chart. The operation principles are given as follows:
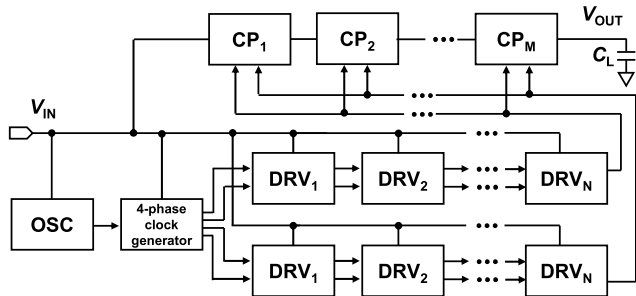

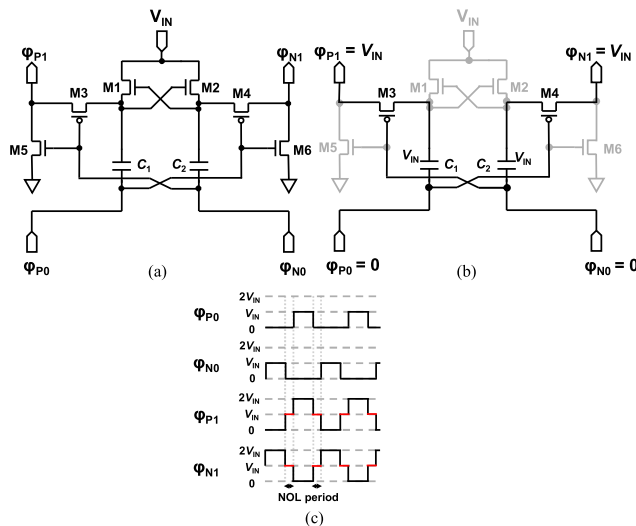**Fig. 2** Block diagram of conventional CP and its driver [25], [26].

Fig. 3 Schematics of (a) conventional driver, (b) its operation when $\varphi_{P0} = \varphi_{N0} = 0$ (switch transistors colored in gray are turned off), and (c) time chart.
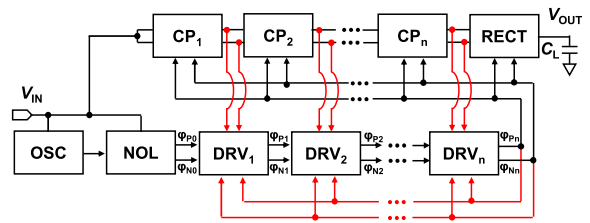

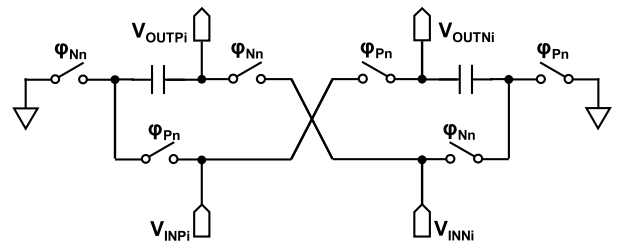**Fig. 4** Block diagram of proposed ELV-CP and its MS-DRV.

Fig. 5 Schematic of CP [27].

1. When input signals $(\varphi_{P0}, \varphi_{N0})$ are $(0, V_{IN})$, top potentials C_1 and C_2 are V_{IN} and $2V_{IN}$, respectively. The output signals $(\varphi_{P1}, \varphi_{N1})$ become $(0, 2V_{IN})$ because switch transistors M4 and M5 are turned on. The boosted signal $(\varphi_{N1} = 2 \times V_{IN})$ can be obtained (see Fig. 7 (a)).

2. When input signals $(\varphi_{P0}, \varphi_{N0})$ are $(V_{IN}, 0)$, top potentials C_1 and C_2 are $2V_{IN}$ and V_{IN}, respectively. The output signals $(\varphi_{P1}, \varphi_{N1})$ become $(2V_{IN}, 0)$ because switch transistors M3 and M6 are turned on. The boosted signal $(\varphi_{P1} = 2 \times V_{IN})$ can be obtained (see Fig. 7 (b)).

3. When input signals $(\varphi_{P0}, \varphi_{N0})$ are $(0, 0)$, top potentials C_1 and C_2 are both V_{IN}. The output signals $(\varphi_{P1}, \varphi_{N1})$ become $(0, 0)$ because reset transistors M5 and M6 are turned on. In this way, the NOL period can be obtained (see Fig. 7 (c)).

Although operation of the proposed MS-DRV was explained by using the first stage of the MS-DRV as an example, the same discussion can be applied to the following drivers.

Note that it is important to point out the cold-start operation of the proposed MS-DRV. When the ELV-CP has not been charged yet during the cold-start period, the output voltage of the MS-DRV cannot be boosted. The output-voltage swing at the last stage of the MS-DRV is therefore given as V_{IN}. However, the output voltage of the ELV-CP is increased by the clock signals, so the output voltage of the MS-DRV also increases. With the mutual relationship between the CPs and DRVs, the output voltage of the ELV-CP increases
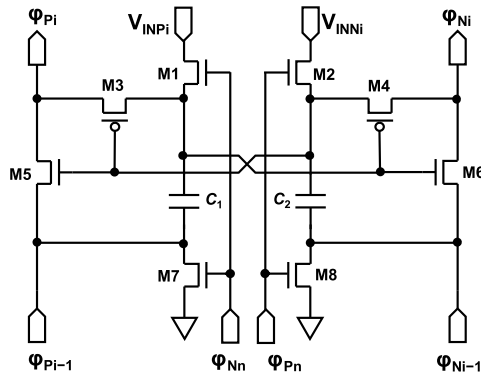
gradually even though the ELV-CP is not precharged.

4. Simulation Results

The performance of the proposed ELV-CP and MS-DRV was evaluated by SPICE with a set of 180-nm CMOS process parameters. A three-stage CP and its driver were designed and evaluated. The ideal voltage-conversion ratio (VCR) of the CP was 8 $(= 2^3)$. All the capacitors were MIM (Metal-Insulator-Metal) capacitors. The charge-transfer capacitors of the first, second, and third CP were set to 55.0, 27.5, and 13.8 pF, respectively. All the capacitors in the DRV and output capacitors were set to 28.8 and 36 pF, respectively. To generate NOL clock signals from V_{IN}, a ring oscillator (ROSC) and an NOL clock generator capable of extremely low-voltage operation were used and designed [17], [28]–[31]. In the simulations, V_{IN} was set to 60 mV for waveforms and 100 mV for other simulations. The output resistance was set to 5 Ω.

Figures 8 (a) and 8 (b) show the simulated output waveforms of the proposed MS-DRV, φ_{P3} and φ_{N3}, and their partial enlarged view, respectively. The voltage swings were 712.6 mV. It is clear that the boosted clock signals were successfully obtained. As shown in Fig. 8 (b), they also have enough NOL time. However, the voltage swings were

Fig. 6 Schematic of proposed DRV.

Fig. 8 (a) Simulated waveforms of proposed DRV and (b) its partial enlarged view. V_{IN} was set to 100 mV (©2022 IEEE [24]).
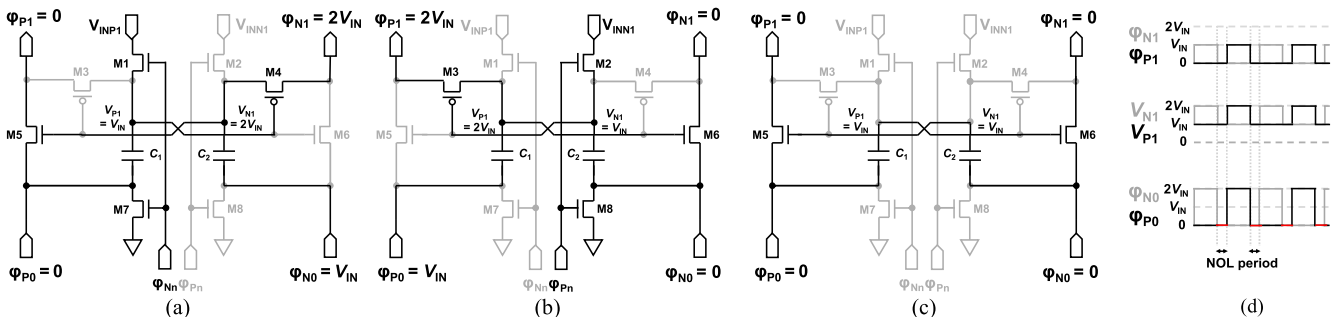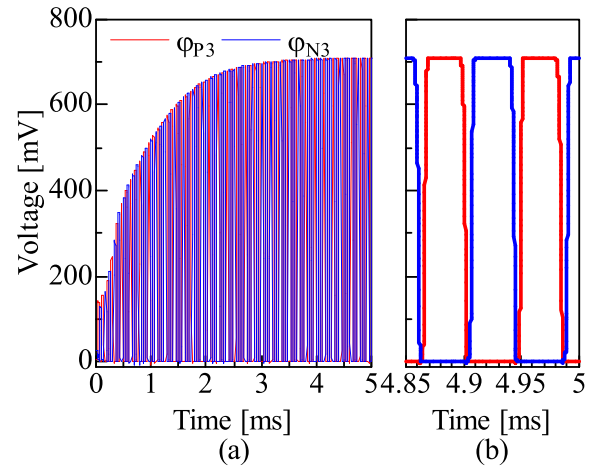

Fig. 7 Operation of the driver: (a) $(\varphi_{P0}, \varphi_{N0}) = (0, V_{IN})$, (b) $(\varphi_{P0}, \varphi_{N0}) = (V_{IN}, 0)$, (c) $(\varphi_{P0}, \varphi_{N0}) = (0, 0)$, and (d) its time chart. Switch transistors colored in gray represent off transistors.
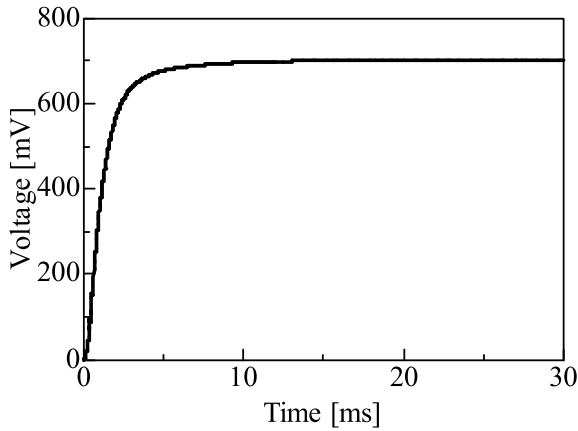
Fig. 9 Simulated transient output voltage of CP (©2022 IEEE [24]).

Fig. 10 Simulated output voltage as a function of load current.

Fig. 11 Simulated power-conversion efficiency as a function of load current.
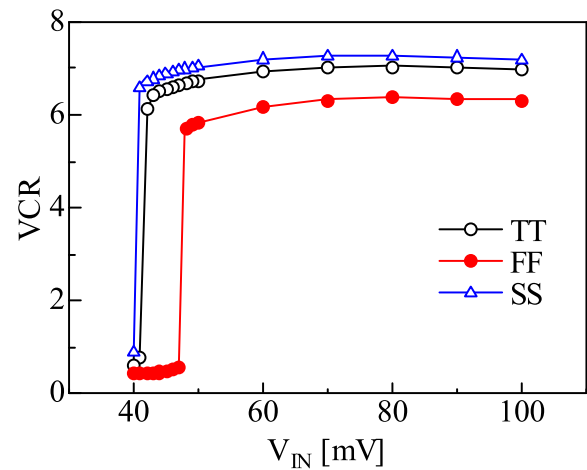
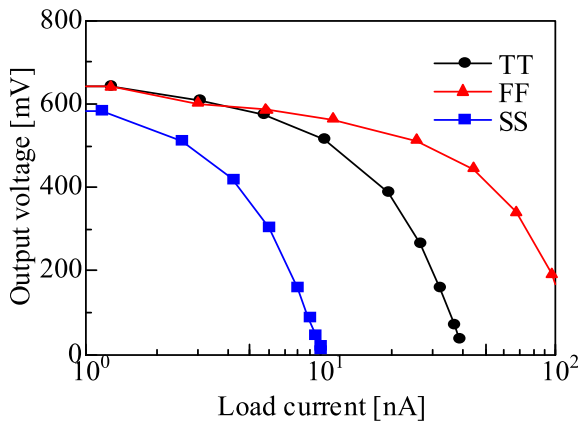**Fig. 12** Simulated VCR as a function of input voltage.

slightly lower than the ideal voltage swings of 800 mV. This was because of the leakage currents of the switch transistors in the ELV-CP and MS-DRV.

Figure 9 shows the simulated transient waveform of the ELV-CP's output voltage under no load. The output voltage increased gradually and settled to 702.5 mV in a steady state.

Figure 10 shows the simulated load-current dependence of output voltage of the ELV-CP at different process corners. In the simulation, we considered typical-typical, fast-fast, and slow-slow (TT, FF, and SS) corners. Slow-fast and fast-slow (SF and FS) corners were not taken in account because it is well known that low-voltage CMOS circuits are hard to operate at the corners [20]. Output voltage decreased as the load current increased. The load-current ranges that can supply output voltage of more than 400 mV at the SS, TT, and FF corners were limited to less than 4, 10, and 44 nA, respectively. This was because the charge transport capability of the ELV-CP depended on the frequency of the ROSC and the frequency changed according to the process corners. As for this cold-start application, the load range is considered acceptable because it is assumed that the generated voltage is used as the supply voltage for the pulse generator [16], [17].

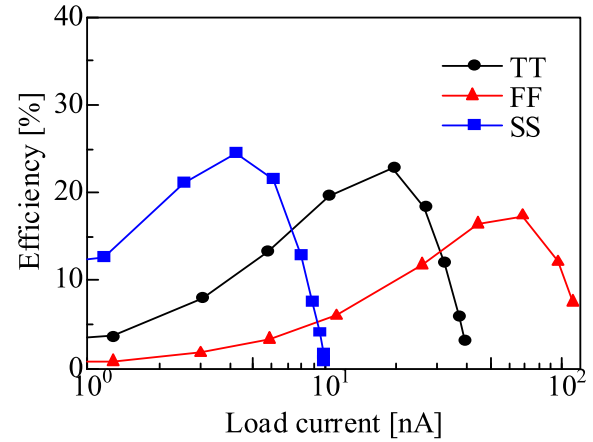Figure 11 shows the power conversion efficiency (PCE) as a function of I_{load} at different process corners. The power dissipation of the ROSC and NOL clock generators was also taken into account. Maximum PCEs at TT, FF, and SS corners were 22.8, 17.4, and 24.5% at 100-mV input voltage and 19.4-, 68.1- and 4.2-nA load current, respectively. As the load current increased, the PCEs decreased due to the on-resistance of the transistors. PCE can also be improved by using larger capacitors in the CP.

Figure 12 shows the VCR as a function of input voltage at different process corners. VCRs at TT, FF and SS corners were higher than 5 when input voltage was higher than 42, 48 and 41 mV, respectively. However, VCR dropped steeply below these voltages, because the open-loop-voltage gain through ELV-CP and MS-DRV decreased to less than 1.

5. Measurement Results

We fabricated a proof-of-concept chip of our proposed ELV-CP and MS-DRV using a 180-nm, 1-poly, 6-metal CMOS technology with a deep n-well option. Figure 13 shows a micrograph of our chip. The area including our proposed ELV-CP, MS-DRV, and peripheral circuits, is 0.36 mm^2.

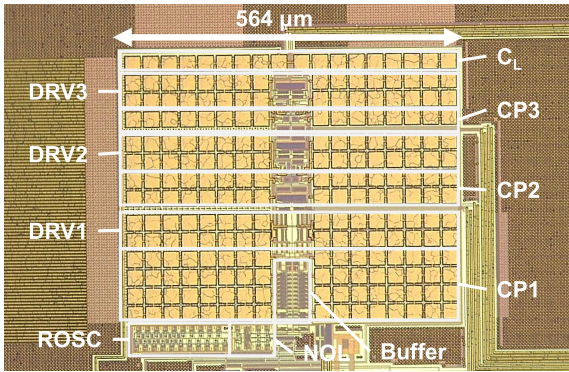Figure 14 shows the measured waveform of the MS-
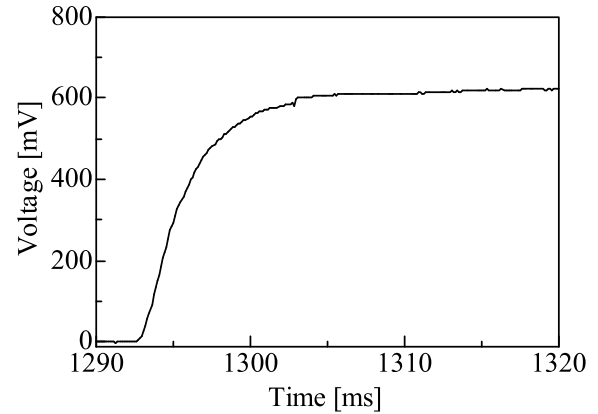
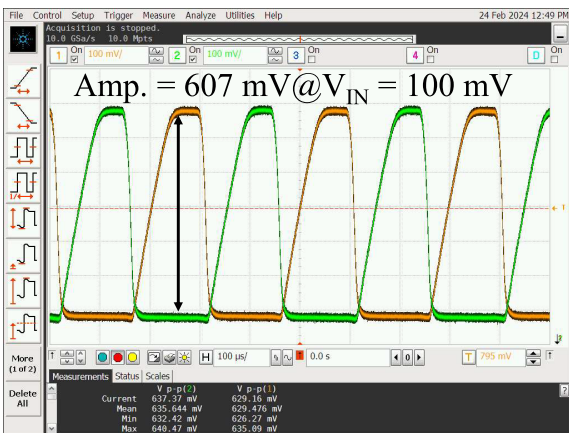**Fig. 13** Chip micrograph.

Fig. 14 Measured waveform of the MS-DRV at V_{IN} = 100 mV.

Fig. 15 Measured waveform of the MS-DRV at V_{IN} = 60 mV.

Fig. 16 Measured output voltage waveform.

Fig. 17 Measured output voltages at different V_{IN}s as a function of load current.

DRV when the V_{IN} = 100 mV. In this measurement, we used a mixed signal oscilloscope (Keysight: MSO9254A) and on-chip source follower buffers to drive the parasitic resistance and capacitance. As can be seen, we obtained two non-overlapping clock signals with enough NOL period. The amplitude of the output signals of the MS-DRV was 607 mV. Figure 15 shows the measured waveform when the V_{IN} = 60 mV. We confirmed the low-voltage operation of the MS-

DRV. The amplitude of the output signals was 350 mV.

Figure 16 shows the measured output voltage of the ELV-CP. In the measurement, we applied a pulse voltage to the input and monitored the output voltage by the semiconductor device parameter analyzer (Keysight: B1500A). The amplitude of the input voltage was set to 100 mV. The output voltage was settled to 620 mV with a 11-ms settling time. The measured output voltage was lower than that of the simulation. The reason for this could be the process variation and leakage current of MOSFETs. As shown in Fig. 12, the simulated VCR decreased as the threshold voltage decreased. Therefore, the threshold voltage condition in our chip might be lower than the TT condition, resulting in the output voltage reduction. The settling time was longer than that of the simulated one. This was because the clock frequency of the ROSC was lower than expected.

Figure 17 shows the measured load-current dependence of the output voltage of the ELV-CP when the V_{IN} was set to 50 to 100 mV. The output voltage decreased as the load current increased. The lower the V_{IN}, the narrower the output current range. This is because the input power and the frequency of the ROSC decreased as the V_{IN} decreased.

Figure 18 shows the measured power conversion effi-

ciency of the ELV-CP when the V_{IN} was set to 50 to 100 mV. The maximum efficiency was 10.7% at V_{IN} = 100 mV and I_{load} = 8.0 nA. The efficiency also degraded as the sim-
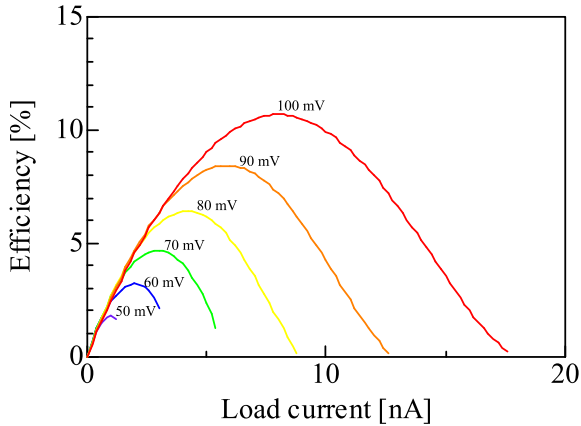

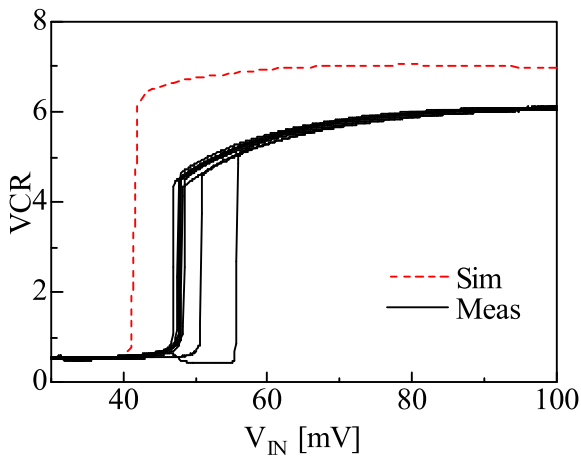**Fig. 18** Measured PCEs at different V_{IN}s as a function of load current.

Fig. 19 Measured and simulated VCRs as a function of input voltage. 10 chips were measured in total.

Table 1 Number of chips among 10 chips that operated at given V_{IN}.

V_{IN} [mV]	45	46	47	48	49	50	55	56	57
Count	0	0	1	5	8	8	9	10	10

ulated results. We consider the difference came from the process variation and parasitic loss. As shown in Fig. 11, the PCEs at FF corner were lower than those at TT corner. As discussed in Fig. 16, the threshold voltage in our chip might be slightly lower than the TT condition. In addition, we obtained Fig. 11 by SPICE simulation. The parasitic loss was no taken into consideration. Therefore, the PCEs were lower than the simulated results.

Figure 19 shows the measured VCRs of the ELV-CP as a function of the input voltage. The results for 10 sample chips were depicted. The simulation results were also plotted for comparison. All 10 chips achieved the VCR above 6 at V_{IN} = 100 mV. The VCR degraded compared to the simulated one. This was because of the process variation and parasitic capacitance.

Table 1 gives the measured number of chips that operated successfully at different V_{IN}s. We counted the number of chips when the VCR exceeds 4 at given V_{IN}. All chips operated successfully with V_{IN} above 56 mV. Even though the voltage was slightly higher than that of simulation results, our proposed circuit achieved extremely low cold-start voltage.

Table 2 summarizes a performance summary and comparison of our proposed circuit and others [16]–[19], [21], [27], [32]. In the table, we used "settling time" for the charge pump circuits and "startup time" for the boost converters, because the charge pump circuit is part of the boost converter. All circuits demonstrate low cold-start voltages. However, [19] is relatively high cold-start voltage compared with others, and [21], [27] need an off-chip external clock signal. Our proposed fully-integrated circuit achieved comparable cold-start voltages to others [16]–[18], [32] with the fastest settling time. Thus, our proposed circuit is efficient and useful for low-voltage thermometric energy harvesting systems.

6. Conclusion

Capable of extremely low-voltage operation for sub-60-mV energy-harvesting applications, an extremely low-voltage charge pump (ELV-CP) and its dedicated multi-stage driver (MS-DRV) were proposed. Although the proposed ELV-CP

Table 2 Performance summary and comparison.

Parameter	This work	[21]	[27]	[17]	[18]	[16]	[19]	[32]
Technology	180 nm	28 nm	350 nm	180 nm	180 nm	180 nm	65 nm	55 nm
Type	CP [1]	CP [1]	CP [1]	CP + PG [2]	CP + PG [2]	BC [3]	BC [3]	BC [3]
Cold-start voltage (mV)	56	50	80	57	60	50	210	83
Cold-start integration	Yes	No (Ext. CLK)	No (Ext. CLK)	Yes	Yes	Yes	Yes	Yes
Settling time (ms)	11 @100 mV	0.4 @50 mV	–	–	–	–	–	–
Startup time (ms)	–	–	–	135 @57 mV	20 @60 mV	21 @100 mV	11 @68 mV	5000 @83 mV
Area (mm^2)	0.36	0.012	0.51	0.96	0.42	1.02	4.6	2.6

1) charge pump, 2) charge pump with pulse generator, 3) switching boost converter

and driver are based on conventional ones, they are modified so that the output voltage of the proposed MS-DRV is maximized. The proposed MS-DRV utilizes the output voltages of each stage of the CP to efficiently boost the control signals. The boosted control clock signals are used as switching signals for each CP and DRV to turn the switch transistors on or off. Moreover, reset transistors are added to the DRV to ensure an adequate non-overlapping period between switching signals. Measured results demonstrated that the proposed MS-DRV can generate boosted clock signals of 350 mV from input voltage of 60 mV. The ELV-CP can boost the input voltage of 100 mV with 10.7% peak efficiency at I_{load} = 8.0 nA. The proposed CP and DRV can boost the low input voltage of 56 mV.

Acknowledgments

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