1. Introduction

A large number of IoT (Internet of Things) edge node devices connected to the network will be installed everywhere. They will be an up-and-coming intelligent communication platform for collecting and delivering information throughout the world. However, maintenance and replacement of the batteries of these battery-powered devices are crucial issues. To address those issues, energy harvesting has attracted extensive attention as an autonomous energy sources for IoT edge node devices [1]–[7].

Thermoelectric generators (TEGs) can generate electrical energy from a slight difference in temperature. However, output voltage of a TEG, $V_{\text{TEG}}$, is too low to operate LSI systems and sensors when temperature difference is a few degrees (e.g., $V_{\text{TEG}}$s are less than several tens of millivolts). An ultra-low-power and highly efficient power-management circuit (PMC) is therefore required [3]–[9].

Figure 1 shows a block diagram of a PMC using a TEG energy harvester. The PMC consists of a voltage-boost converter (VBC) and a cold-start subcircuit. The cold-start subcircuit must operate at low voltage $V_N$ and generate control signals for the VBC. For that purpose, a multi-stage charge pump (CP) and its driver (DRV) circuit are extensively used to convert low input voltage of 56 mV. The ELV-CP can boost the input voltage of 100 mV with 10.7% peak efficiency. The proposed ELV-CP and MS-DRV can boost the low input voltage of 56 mV.

SUMMARY

Extremely low-voltage charge pump (ELV-CP) and its dedicated multi-stage driver (MS-DRV) for sub-60-mV thermoelectric energy harvesting are proposed. The proposed MS-DRV utilizes the output voltages of each ELV-CP to efficiently boost the control clock signals. The boosted clock signals are used as switching signals for each ELV-CP and MS-DRV to turn switch transistors on and off. Moreover, reset transistors are added to the MS-DRV to ensure an adequate non-overlapping period between switching signals. Measurement results demonstrated that the proposed MS-DRV can generate boosted clock signals of 350 mV from input voltage of 60 mV. The ELV-CP can boost the input voltage of 100 mV with 10.7% peak efficiency. The proposed ELV-CP and MS-DRV can boost the low input voltage of 56 mV.

key words: Energy harvesting, Power management circuit, Voltage boost converter, Cold-start circuit, Start-up circuit, Charge pump, Driver circuit

extremely low-voltage CP (ELV-CP) and its dedicated multi-stage driver (MS-DRV) for sub-60-mV energy harvesting. The proposed MS-DRV utilizes the output voltages of each ELV-CP to efficiently boost control signals. The boosted clock signals are used as switching signals for each ELV-CP and MS-DRV to turn switch transistors on and off at low $V_N$ [22], [23]. Moreover, reset transistors are added to the MS-DRV to ensure an adequate non-overlapping (NOL) period between switching signals. In contrast to our previous work [24], we add some simulation results and discuss its circuit operation in more detail. In addition, we fabricate a proof-of-concept chip using a 180-nm CMOS process and demonstrate the effectiveness of our propose circuits. The proposed ELV-CP and MS-DRV can operate at extremely low $V_N$ of 56 mV.

This paper is organized as follows: Section 2 briefly describes conventional CP and DRV and explains the issues concerning them; Section 3 presents the proposed ELV-CP and MS-DRV; Section 4 shows the results of simulations; Section 5 discusses the results of measurements; and Section 6 concludes the paper.

2. Conventional CP and DRV

Figure 2 shows a block diagram of conventional CP and its DRV [25], [26]. A high voltage-conversion ratio (VCR) can be realized by connecting $n$-stage CPs in cascade. For the multi-stage CP, a DRV is required to turn the switch transistors in the CPs on and off. As shown in Fig. 2, the boosted clock signals can also be generated by connecting $n$-stage DRVs in cascade. It should be noted that it is difficult to obtain higher boosted clock signals because the voltage-boost ratio of the $n$-stage DRVs is limited by $n + 1$. In addition, conventional CPs use a 4-phase clock generator, which consists of a NOL.

The authors are with the Graduate School of Engineering, Osaka University, Suita-shi, 565-0871 Japan.

Fig. 1 Power management circuit for low-voltage energy harvesting (©2022 IEEE [24]).
clock generator and some logic gates, to control the switch transistors in the DRVs [25], [26]. However, when the clock signals are applied to the DRVs, the timing of the signals is delayed, so a multi-stage DRV cannot generate NOL boosted clock signals. The number of the drivers is therefore limited to less than 3 or 4; thus, higher clock signals cannot be obtained stably.

Note that a conventional DRV cannot operate correctly with NOL clock signals. Figure 3 shows schematics of a conventional driver [26] and its operation when \( \varphi_{P0} = \varphi_{N0} = 0 \) (switch transistors colored in gray are turned off), and (c) time chart. Under the condition, both of the top potentials of \( C_1 \) and \( C_2 \) are \( V_{IN} \), and PMOS switch transistors M3 and M4 are turned on, as shown in Fig. 3(b) (in which switch transistors colored in gray are turned off). Therefore, both output voltages become \( V_{IN} \). In other words, the NOL period of the output voltages cannot be obtained when \( \varphi_{P0} = \varphi_{N0} = 0 \), so operation of the multi-stage DRV circuit fails. Consequently, a 4-phase clock generator is conventionally used to control switching timing [25], [26].

To solve the above-described problems, a low-voltage CP and DRV are proposed and described in detail in the next section.

3. Proposed ELV-CP and MS-DRV

Figure 4 shows a block diagram of the proposed ELV-CP and its MS-DRV. The proposed circuits are based on the conventional one, except the DRV is modified to generate higher-boosted clock signals with adequate NOL period [26]. Note that a dual-input and dual-output CP as reported in [27] is used, and the output voltages of the CP change between \( V_{IN} \) and \( 2V_{IN} \) alternately, as shown in Fig. 5. A conventional rectifier (RECT) is used to obtain the output voltage \( V_{OUT} \) [27].

Differing from the conventional design, the proposed MS-DRV accepts output voltages of each CP to boost the control signals, as shown in Fig. 4. Voltage-boost ratio of the \( n \)-stage MS-DRV can therefore be increased to \( 2^n \), which is much higher than the conventional design of \( n + 1 \). In addition, each MS-DRV accepts the boosted clock signals \( \varphi_{Pn} \) and \( \varphi_{Nn} \) to improve the performance of the switch transistors in the MS-DRV.

Figure 6 shows a schematic of the first stage of the proposed MS-DRV. Input NOL signals \( \varphi_{P0} \) and \( \varphi_{N0} \) are applied to the MS-DRV, and boosted NOL signals \( \varphi_{P1} \) and \( \varphi_{N1} \) are
then generated. The output voltages of CP1 are applied to \( V_{\text{INP1}} \) and \( V_{\text{INN1}} \). They determine the voltage-boost ratio of \( \varphi_{\text{P1}} \) and \( \varphi_{\text{N1}} \). The boost ratio is determined by one of the two CP’s output voltages. In this design, we use a lower output voltage of the CP’s output voltages because the leakage loss increases when the higher output voltage is used. Boosted control signals \( \varphi_{\text{Pn}} \) and \( \varphi_{\text{Nn}} \) are applied to the MS-DRV in opposite-phase relation, as shown in Fig. 6.

Figure 7 illustrates operation of the proposed MS-DRV and its time chart. The operation principles are given as follows:

1. When input signals \((\varphi_{\text{P0}}, \varphi_{\text{N0}})\) are \((0, V_{\text{IN}})\), top potentials \( C_1 \) and \( C_2 \) are \( V_{\text{IN}} \) and \( 2V_{\text{IN}} \), respectively. The output signals \((\varphi_{\text{P1}}, \varphi_{\text{N1}})\) become \((0, 2V_{\text{IN}})\) because switch transistors M4 and M5 are turned on. The boosted signal \((\varphi_{\text{N1}} = 2 \times V_{\text{IN}})\) can be obtained (see Fig. 7(a)).

2. When input signals \((\varphi_{\text{P0}}, \varphi_{\text{N0}})\) are \((V_{\text{IN}}, 0)\), top potentials \( C_1 \) and \( C_2 \) are \( 2V_{\text{IN}} \) and \( V_{\text{IN}} \), respectively. The output signals \((\varphi_{\text{P1}}, \varphi_{\text{N1}})\) become \((2V_{\text{IN}}, 0)\) because switch transistors M3 and M6 are turned on. The boosted signal \((\varphi_{\text{P1}} = 2 \times V_{\text{IN}})\) can be obtained (see Fig. 7(b)).

3. When input signals \((\varphi_{\text{P0}}, \varphi_{\text{N0}})\) are \((0, 0)\), top potentials \( C_1 \) and \( C_2 \) are both \( V_{\text{IN}} \). The output signals \((\varphi_{\text{P1}}, \varphi_{\text{N1}})\) become \((0, 0)\) because reset transistors M5 and M6 are turned on. In this way, the NOL period can be obtained (see Fig. 7(c)).

Although operation of the proposed MS-DRV was explained by using the first stage of the MS-DRV as an example, the same discussion can be applied to the following drivers.

Note that it is important to point out the cold-start operation of the proposed MS-DRV. When the ELV-CP has not been charged yet during the cold-start period, the output voltage of the MS-DRV cannot be boosted. The output-voltage swing at the last stage of the MS-DRV is therefore given as \( V_{\text{IN}} \). However, the output voltage of the ELV-CP is increased by the clock signals, so the output voltage of the MS-DRV also increases. With the mutual relationship between the CPs and DRVs, the output voltage of the ELV-CP increases gradually even though the ELV-CP is not precharged.

4. Simulation results

The performance of the proposed ELV-CP and MS-DRV was evaluated by SPICE with a set of 180-nm CMOS process parameters. A three-stage CP and its driver were designed and evaluated. The ideal voltage-conversion ratio (VCR) of the CP was \( 8 \) (= \( 2^3 \)). All the capacitors were MIM (Metal-Insulator-Metal) capacitors. The charge-transfer capacitors of the first, second, and third CP were set to 55.0, 27.5, and 13.8 pF, respectively. All the capacitors in the DRV and output capacitors were set to 28.8 and 36 pF, respectively. To generate NOL clock signals from \( V_{\text{IN}} \), a ring oscillator (ROSC) and an NOL clock generator capable of extremely low-voltage operation were used and designed [17], [28]– [31]. In the simulations, \( V_{\text{IN}} \) was set to 60 mV for waveforms and 100 mV for other simulations. The output resistance was set to 5 Ω.

Figures 8(a) and 8(b) show the simulated output waveforms of the proposed MS-DRV, \( \varphi_{\text{P3}} \) and \( \varphi_{\text{N3}} \), and their partial enlarged view, respectively. The voltage swings were 712.6 mV. It is clear that the boosted clock signals were successfully obtained. As shown in Fig. 8(b), they also have enough NOL time. However, the voltage swings were

![Fig. 7 Operation of the driver: (a) \((\varphi_{\text{P0}}, \varphi_{\text{N0}}) = (0, V_{\text{IN}})\), (b) \((\varphi_{\text{P0}}, \varphi_{\text{N0}}) = (V_{\text{IN}}, 0)\), (c) \((\varphi_{\text{P0}}, \varphi_{\text{N0}}) = (0, 0)\), and (d) its time chart. Switch transistors colored in gray represent off transistors.](image)

![Fig. 8 (a) Simulated waveforms of proposed DRV and (b) its partial enlarged view. \( V_{\text{IN}} \) was set to 100 mV (©2022 IEEE [24]).](image)
slightly lower than the ideal voltage swings of 800 mV. This was because of the leakage currents of the switch transistors in the ELV-CP and MS-DRV.

Figure 9 shows the simulated transient waveform of the ELV-CP’s output voltage under no load. The output voltage increased gradually and settled to 702.5 mV in a steady state.

Figure 10 shows the simulated load-current dependence of output voltage of the ELV-CP at different process corners. In the simulation, we considered typical-typical, fast-fast, and slow-slow (TT, FF, and SS) corners. Slow-fast and fast-slow (SF and FS) corners were not taken into account because it is well known that low-voltage CMOS circuits are hard to operate at the corners [20]. Output voltage decreased as the load current increased. The load-current ranges that can supply output voltage of more than 400 mV at the SS, TT, and FF corners were limited to less than 4, 10, and 44 nA, respectively. This was because the charge transport capability of the ELV-CP depended on the frequency of the ROSC and the frequency changed according to the process corners. As for this cold-start application, the load range is considered acceptable because it is assumed that the generated voltage is used as the supply voltage for the pulse generator [16], [17].

Figure 11 shows the power conversion efficiency (PCE) as a function of $I_{\text{load}}$ at different process corners. The power dissipation of the ROSC and NOL clock generators was also taken into account. Maximum PCEs at TT, FF, and SS corners were 22.8, 17.4, and 24.5% at 100-mV input voltage and 19.4-, 68.1- and 4.2-nA load current, respectively. As the load current increased, the PCEs decreased due to the on-resistance of the transistors. PCE can also be improved by using larger capacitors in the CP.

Figure 12 shows the VCR as a function of input voltage at different process corners. VCRs at TT, FF and SS corners were higher than 5 when input voltage was higher than 42, 48 and 41 mV, respectively. However, VCR dropped steeply below these voltages, because the open-loop-voltage gain through ELV-CP and MS-DRV decreased to less than 1.

5. Measurement Results

We fabricated a proof-of-concept chip of our proposed ELV-CP and MS-DRV using a 180-nm, 1-poly, 6-metal CMOS technology with a deep n-well option. Figure 13 shows a micrograph of our chip. The area including our proposed
ELV-CP, MS-DRV, and peripheral circuits, is 0.36 mm$^2$.

Figure 14 shows the measured waveform of the MS-DRV when the $V_{IN} = 100$ mV. In this measurement, we used a mixed signal oscilloscope (Keysight: MSO9254A) and on-chip source follower buffers to drive the parasitic resistance and capacitance. As can be seen, we obtained two non-overlapping clock signals with enough NOL period. The amplitude of the output signals of the MS-DRV was 607 mV. Figure 15 shows the measured waveform when the $V_{IN} = 60$ mV. We confirmed the low-voltage operation of the MS-DRV. The amplitude of the output signals was 350 mV.

Figure 16 shows the measured output voltage of the ELV-CP. In the measurement, we applied a pulse voltage to the input and monitored the output voltage by the semiconductor device parameter analyzer (Keysight: B1500A). The amplitude of the input voltage was set to 100 mV. The output voltage was settled to 620 mV with a 11-ms settling time. The measured output voltage was lower than that of the simulation. The reason for this could be the process variation and leakage current of MOSFETs. As shown in Fig. 12, the simulated VCR decreased as the threshold voltage decreased. Therefore, the threshold voltage condition in our chip might be lower than the TT condition, resulting in the output voltage reduction. The settling time was longer than that of the simulated one. This was because the clock frequency of the ROSC was lower than expected.

Figure 17 shows the measured load-current dependence of the output voltage of the ELV-CP when the $V_{IN}$ was set to 50 to 100 mV. The output voltage decreased as the load current increased. The lower the $V_{IN}$, the narrower the output current range. This is because the input power and the
frequency of the ROSE decreased as the \( V_{IN} \) decreased.

Figure 18 shows the measured power conversion efficiency of the ELV-CP when the \( V_{IN} \) was set to 50 to 100 mV. The maximum efficiency was 10.7% at \( V_{IN} = 100 \) mV and \( I_{load} = 8.0 \) nA. The efficiency also degraded as the simulated results. We consider the difference came from the process variation and parasitic loss. As shown in Fig. 11, the PCEs at FF corner were lower than those at TT corner. As discussed in Fig. 16, the threshold voltage in our chip might be slightly lower than the TT condition. In addition, we obtained Fig. 11 by SPICE simulation. The parasitic loss was not taken into consideration. Therefore, the PCEs were lower than the simulated results.

Figure 19 shows the measured VCRs of the ELV-CP as a function of the input voltage. The results for 10 sample chips were depicted. The simulation results were also plotted for comparison. All 10 chips achieved the VCR above 50 mV at \( V_{IN} = 100 \) mV. The VCR degraded compared to the simulated one. This was because of the process variation and parasitic capacitance.

Table 1 gives the measured number of chips that operated successfully at different \( V_{IN} \). We counted the number of chips when the VCR exceeds 4 at given \( V_{IN} \). All chips operated successfully with \( V_{IN} \) above 56 mV. Even though the voltage was slightly higher than that of simulation results, our proposed circuit achieved extremely low cold-start voltage.

Table 2 summarizes a performance summary and comparison of our proposed circuit and others [16]–[19], [21], [27], [32]. In the table, we used “settling time” for the charge pump circuits and “startup time” for the boost converters, because the charge pump circuit is part of the boost converter. All circuits demonstrate low cold-start voltages. However, [19] is relatively high cold-start voltage compared with others, and [21], [27] need an off-chip external clock signal. Our proposed fully-integrated circuit achieved comparable cold-start voltages to others [16]–[18], [32] with the fastest settling time. Thus, our proposed circuit is efficient and useful for low-voltage thermometric energy harvesting systems.

6. Conclusion

Capable of extremely low-voltage operation for sub-60-mV energy-harvesting applications, an extremely low-voltage charge pump (ELV-CP) and its dedicated multi-stage driver (MS-DRV) were proposed. Although the proposed ELV-CP and driver are based on conventional ones, they are modified so that the output voltage of the proposed MS-DRV is maximized. The proposed MS-DRV utilizes the output voltages of each stage of the CP to efficiently boost the control signals. The boosted control clock signals are used as switching signals for each CP and DRV to turn the switch transistors on or off. Moreover, reset transistors are added to the DRV to ensure an adequate non-overlapping period between switching signals. Measured results demonstrated that the proposed MS-DRV can generate boosted clock signals of 350 mV from input voltage of 60 mV. The ELV-CP can boost the input voltage of 100 mV with 10.7% peak efficiency at \( I_{load} = 8.0 \) nA. The proposed CP and DRV can boost the low input voltage of 56 mV.

Acknowledgment

This work was supported through the activities of VDEC, the University of Tokyo, in collaboration with Cadence Design Systems and Mentor Graphics. This work was also partly supported by JSPS KAKENHI Grant Numbers JP20H00606, JP22H03558, and JP23H03364.

References

### Table 2: Performance summary and comparison.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work</th>
<th>[21]</th>
<th>[27]</th>
<th>[17]</th>
<th>[18]</th>
<th>[16]</th>
<th>[19]</th>
<th>[32]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>180 nm</td>
<td>28 nm</td>
<td>350 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>65 nm</td>
<td>55 nm</td>
</tr>
<tr>
<td>Type</td>
<td>CP</td>
<td>CP</td>
<td>CP</td>
<td>CP + PG</td>
<td>CP + PG</td>
<td>BC</td>
<td>BC</td>
<td>BC</td>
</tr>
<tr>
<td>Cold-start voltage (mV)</td>
<td>56</td>
<td>50</td>
<td>80</td>
<td>57</td>
<td>60</td>
<td>50</td>
<td>210</td>
<td>83</td>
</tr>
<tr>
<td>Cold-start integration</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Settling time (ms)</td>
<td>11</td>
<td>0.4</td>
<td>80</td>
<td>11</td>
<td>20</td>
<td>21</td>
<td>5000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>@100 mV</td>
<td>@50 mV</td>
<td>@50 mV</td>
<td>@57 mV</td>
<td>@60 mV</td>
<td>@100 mV</td>
<td>@68 mV</td>
<td>@83 mV</td>
</tr>
<tr>
<td>Startup time (ms)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>135</td>
<td>20</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>@57 mV</td>
<td>@60 mV</td>
<td>@100 mV</td>
<td>@68 mV</td>
<td>@83 mV</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.36</td>
<td>0.012</td>
<td>0.51</td>
<td>0.56</td>
<td>0.42</td>
<td>1.02</td>
<td>4.6</td>
<td>2.6</td>
</tr>
</tbody>
</table>

1) charge pump, 2) charge pump with pulse generator, 3) switching boost converter
Hikaru SEBE received the B.S. and M.S. degrees in the Division of Electrical, Electronic and Information Engineering from Osaka University, Osaka, Japan, in 2020 and 2022, respectively. He is currently working toward the Ph.D. degree at the same university. His current research interests are in ultra-low-power and ultra-low-voltage CMOS circuits design.

Daisuke KANEMOTO received the B.S. degree in Electronics and Information Science from Kyoto Institute of Technology, Kyoto, Japan, in 2004 and received the M.S. and Ph.D. degrees in Electronic Engineering from Osaka University, Osaka, Japan, in 2006, 2011. From November 2010 to 2013, he was an assistant professor at the Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka, Japan. From April 2013, he has been an associate professor at the Department of Research Interdisciplinary Graduate School of Medicine and Engineering, University of Yamanashi, Yamanashi, Japan. From May 2015, he has been a visiting assistant professor at the Department of Electrical Engineering, Stanford University, Stanford, USA. From June 2019, he has been a professor with the Graduate School of Engineering, Osaka University, Osaka, Japan. His research interests include analog circuits, mixed-signal integrated circuits and compressed sensing. He is an IEEE member.

Tetsuya HIROSE received B.S., M.S., and Ph.D. degrees from Osaka University, Osaka, Japan, in 2000, 2002, and 2005, respectively. From 2004 to 2008, he was a Research Associate with the Department of Electrical Engineering, Hokkaido University, Sapporo, Japan. From 2009 to 2019, he has held an Associate Professor with the Department of Electrical and Electronic Engineering, Kobe University, Kobe, Japan. Since 2019, he has been a Professor with the Division of Electrical, Electronic and Information Engineering, Graduate School of Engineering, Osaka University, Suita, Japan. He has authored or co-authored over 200 journal and conference papers. His current research interests are extremely low-voltage and low-power analog/digital mixed-signal integrated circuit design and smart sensor systems. Dr. Hirose is a senior member of the Institute of Electrical and Electronics Engineers (IEEE), and a member of the Institute of Electronics, Information and Communication Engineers (IEICE), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the 10th Joint Research Award of the Semiconductor Technology Academic Research Center (STARC) in 2013, the Marubun Research Encouragement Awards in 2017, the IEICE Best Invited Paper Award in 2022, and more than 30 other international and domestic awards. He served as a Technical Program Committee member of the International Conference on Solid-State Devices and Materials from 2010 to 2013, the Asian Solid-State Circuits Conference from 2011 to 2022, an Associate Editor for the IEICE Electronics Express from 2012 to 2015, the Chapter Secretary of the IEEE SSCS Kansas Chapter from 2015 to 2016, and a Guest Associate Editor for the special issues of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and on Electronics from 2010 to 2023.