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PAPER

Computer-aided Design of Cross-voltage-domain Energy-optimized Tapered Buffers

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SUMMARY This paper introduces a computer-aided low-power design method for tapered buffers that address given load capacitances, output transition times, and source impedances. Cross-voltage-domain tapered buffers involving a low-voltage domain in the frontier stages and a high-voltage domain in the posterior stages are further discussed which breaks the trade-off between the energy dissipation and the driving capability in conventional designs. As an essential circuit block, a dedicated analytical model for the level-shifter is proposed. The energy-optimized tapered buffer design is verified for different source and load conditions in a 180-nm CMOS process. The single-V_{DD} buffer model achieves an average inaccuracy of 8.65% on the transition loss compared with Spice simulation results. Cross-voltage tapered buffers can be optimized to further remarkably reduce the energy consumption. The study finds wide applications in energy-efficient switching-mode analog applications.

key words: *Tapered buffer, level-shifter, analytical model, low-power circuit, switching-mode, gate driver, short-circuit power.*

1. Introduction

Rail-to-rail tapered buffers are extensively applied as gate drivers in a variety of switching-mode circuits such as power amplifiers (PAs)[1][2][3][4], and DC-DC converters[5][6][7][8].

While tapered buffers in digital applications emphasize energy and delay [9][10], gate drivers focus on the energy dissipation for a given drive capability. Research on digital buffers sheds valuable insights into the design of analog gate drivers. For example, Cherkauer et al. provided analytical expressions for the propagation delay, the power dissipation, the physical area, and the system reliability of tapered buffers with fixed ratios between successive stages[11]. In addition, it has been shown that the minimal delay buffer design is contradictory to the purpose of minimizing energy consumption alone[12][13][14].

The driving strength of tapered buffers is manifested by the output transition time, τ_{tb}, for a certain load. And the total energy dissipation of tapered buffers during transition (denoted as E_{tot}) consists of the dynamic losses and the short-circuit losses of each stage (denoted as E_{dyn} and E_{sc}, respectively). While the former can be easily calculated by the corresponding load capacitance, the estimation for E_{sc} is extremely difficult [15][16]. Although it is claimed that tapered buffers with fixed tapering factors feature relatively low total E_{sc}[15][17], variably changing the dimensions of each buffer stage can further reduce the energy consumption. E_{dyn} and E_{sc} decrease with a lower supply voltage, which implies the use of a lower V_{DD} domain for power constraint applications. Kursun et al. introduced a low-voltage-swing gate drive technique for the tapered buffer to reduce E_{dyn} [18]. In a buck converter with a 660 MHz switching frequency, a half-rail swing technique for the tapered buffer is employed to reduce the switching losses[19]. While at the same power supply, Frustaci et al. proposed the tapered-V_{TH} buffer design involving transistors with different V_{THs}. While high-V_{TH} devices in the front-end stages reduces the leakage and dynamic power, low-V_{TH} devices in the back-end stages favors the driving capabilities[20]. The applications of tapered buffers often involve different voltage domains in which the frontier and posterior stages operate at different voltages. For example, in DC-DC converters and power amplifiers, the digital control systems are typically powered at a relatively low voltage supply for power reduction and the final stage at a high voltage supply for enhanced driving capabilities. Therefore, a tapered buffer operating at multiple voltage domains is expected to strike a balance between the power consumption and the driving capability.

The analytical model of tapered buffers enables the estimation of its performance, and optimization can be achieved through computer-aided computation methods. For example, Liu et al. applied an iterative optimization algorithm for to improved design metrics such as area, delay, and power[21]. Overeem et al. generated a large quantity of random solutions and select the optimal one[22].

This work aims for the energy-optimized tapered buffer (EOTB) design that meets the output transition time specification (denoted as $\tau_{tb,spec}$) for a given load capacitance, while consuming minimal energy consumption. Cross-V_{DD} energy-optimized tapered buffers (CV-EOTBs) are carefully studied, which consists of two V_{DD} domains and a level-shifter. A computer-aided traversal optimization scheme is proposed to achieve the optimal solution.

The rest of the paper is organized as follows. Section 2 proposes the analytical models of the output transition time (denoted as τ_{out}) and E_{sc} of CMOS inverters. Section 3 introduces the analytical models of τ_{out} and E_{sc} of level-shifters, which serve as a crucial step for CV-EOTB designs. Section 4 presents the design strategy for single-V_{DD} EOTBs based on the proposed analytical models. Section 5 discusses

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the design of CV-EOTBs. Section 6 summaries the performances of the tapered buffers achieved through the proposed optimization procedures. Finally, section 7 concludes the paper. In addition, Appendix A presents the parameter values of the analytical inverter models of the inverter. Appendix B presents four design cases of single-V_{DD} EOTBs(Case #B1, Case #B2, Case #B3, Case #B4).

2. Transition Time and Short-circuit Energy of Inverters

Fig.1 shows the circuit schematic of a CMOS inverter. The transition time is defined as the duration of the voltage transition between 10% V_{DD} and 90% V_{DD}. An accurate inverter model for τ_{out}, should involve the input transition time, τ_{in}, the load capacitance, C_L, and the transistor sizes. It has been pointed out that the τ_{out} models without considering τ_{in} are not accurate, especially for slow input transitions[23]. Thus, Dutta et al. propose a general formulation of τ_{out} involving τ_{in} by curve fitting between the infinitely fast and slow input scenarios[23]. Maurine et al. derive an explicit model of τ_{out} for fast and slow input cases, respectively[24]. It indicates that τ_{out} with slow inputs is proportional to the square root of τ_{in}.

The switching loss of inverters consists of E_{dyn} and E_{sc}[16][25][26][27][28] which are illustrated in Fig.2(a) and (b), respectively. When the output voltage of the inverter flips from low to high, the dynamic energy loss equals $\frac{1}{2}C_L V_{DD}^2$ as shown in Fig.2(a). On the other hand, during the input transition, there is a phase when both the NMOS and PMOS transistors conducts (indicated by the blue line). The associated energy loss is refered to as E_{sc}. Veendrick et al. derived an approximate expression of E_{sc} for an unloaded inverter and investigate the impact of C_L. The study assumed that with equal τ_{in} and τ_{out}, E_{sc} would only be a small portion (typically less than 20%) of the total transition loss of an inverter. Thus, it proposed fixed-ratio tapered buffer (FTB) designs which feature equalized τ_{in} and τ_{out}. However, the study has not considered variable gate lengths. For inputs with different τ_{in}, transistors in an inverter will experience different operating regions. Therefore, Bisdounis et al. classified four catagories of input ramps and constructed E_{sc} models respectively [29]. Concise models of an inverter is extremely desirable for EOTB designs.

2.1 Analytical Model for Inverter Output Transition Time

The proposed analytical model for τ_{out} is dependent on C_L, τ_{in} and transistor sizes. It is assumed that while NMOS and PMOS transistors have the same gate length, L, the widths of the PMOS transistor, W_p, and NMOS transistor, W_n, enjoy a fixed ratio S, i.e.,

$$W_p = SW_n \tag{1}$$

It is also assumed that $|V_{TH,p}| = V_{TH,n} = V_{TH}$. The propagation delay of the inverter, t_d, can be employed as an intermediary variable that correlates τ_{in} and τ_{out} which is

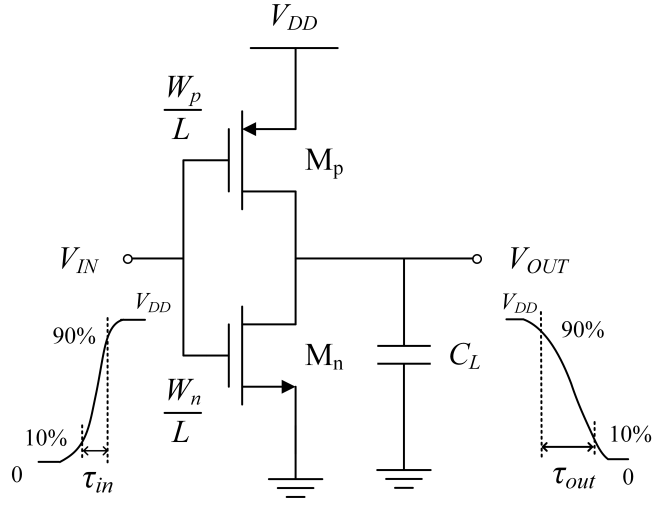

Fig. 1 CMOS inverter.

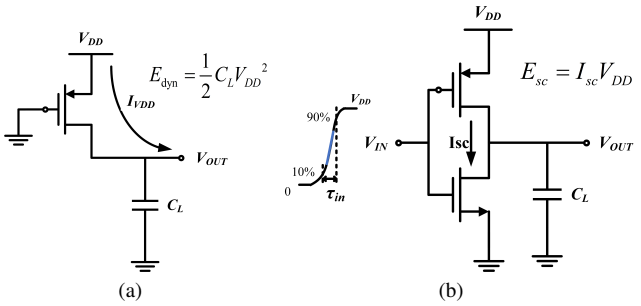

Fig. 2 Illustration of (a) E_{dyn} and (b) E_{sc}.

expressed as follows [30],

$$t_d = \left(\frac{1}{2} - \frac{1-\nu_{TH}}{1+\alpha}\right)\tau_{in} + \frac{C_L V_{DD}}{2I_{D0}}, \nu_{TH} = \frac{V_{TH}}{V_{DD}} \tag{2}$$

where α is the speed saturation index, and I_{D0} is the saturation current for $V_{GS} = V_{DS} = V_{DD}$.

t_{ds} is the step response of an inverter and is expressed as,

$$t_{ds} = \frac{C_L}{\mu C_{ox}(W_n/L)} \cdot \frac{2V_{DD}}{7/4V_{DD}^2 + V_{TH}^2 - 3V_{DD}V_{TH}} \tag{3}$$

For a given τ_{in}, τ_{out} can be derived as follows[31],

$$\tau_{out} = 2t_{ds}\frac{1-\nu_{TH}}{0.5 + \frac{t_d}{\tau_{in}} - \nu_{TH}} \tag{4}$$

Therefore, by combining Eqs.(2), (3) and (4), τ_{out} can be expressed as follows,

$$\tau_{out} = \frac{C_L \tau_{in}}{p_1(\frac{W_n}{L})\tau_{in} + p_2 C_L} \tag{5}$$

where p_1 and p_2 are the composite fitting parameters depending on V_{TH}, α and V_{DD}, etc. The unit of p_1 is fF/ns and p_2 is unitless. Units of all quantities used in the proposed

Table 1 Units of Quantities in the Analytical Models

Qiantities	Units
Transition time	ns
Capacitance	fF
Energy	pJ
Transistor Size	μm

analytical models are listed in Table 1.

2.2 Analytical Model for Inverter Short-circuit Energy

E_{sc} exists due to the direct current path from V_{DD} to V_{SS} during the transition. Previous research has revealed that τ_{in}, C_L, and transistor sizes directly affect E_{sc}, therefore, are involved in the E_{sc} model.
According to[32], a simplified E_{sc} formula for inverters with relatively slow inputs is expressed as follows,

$$E_{sc}(\tau_{in} \gg \tau_{out}) = k_{sc1}(\frac{W_n}{L})\tau_{in} \tag{6}$$

where k_{sc1} is a composite model parameter which is determined according to V_{DD} and the normalized drain saturated voltage.
For inverters with fast inputs, the E_{sc} model is expressed as,

$$E_{sc}(\tau_{in} \ll \tau_{out}) = \frac{k_{sc2}(\frac{W_n}{L})^2}{C_L}\tau_{in}^2 \tag{7}$$

where k_{sc2} is a composite model parameter determined by V_{TH} and α[32].
A modified E_{sc} model is proposed by combining Eqs.(6) and (7) as follows.

$$E_{sc} = \frac{1}{1/E_{sc}(\tau_{in} \ll \tau_{out}) + 1/E_{sc}(\tau_{in} \gg \tau_{out})} \tag{8}$$

It is simplified as,

$$E_{sc} = \frac{(\frac{W_n}{L})^2\tau_{in}^2}{k_1 C_L + k_2(\frac{W_n}{L})\tau_{in}} \tag{9}$$

where k_1 and k_2 are composite fitting parameters. Their units are ns^2/pJ/fF and ns/pJ, respectively.

2.3 Sub-models and Parameter Extraction

As pointed out by previouts research [29][31], τ_{out} and E_{sc} vary significantly for different τ_{in}. Therefore, it is necessary to split the models into sub-models according to τ_{in} for more accurate evaluations. These sub-models are denoted as $M_{0.1,1}, M_{1,10}, M_{10,100}, M_{100,1000}, M_{1000,10000}, M_{10000,100000}$, respectively, where the subscripts represent their respective ranges of τ_{in} in ns. Each sub-model enjoys the same expression but with different model parameters. All the sub-model parameters are extracted through curve-fitting based on SPICE simulations. The results are listed in Appendix A.

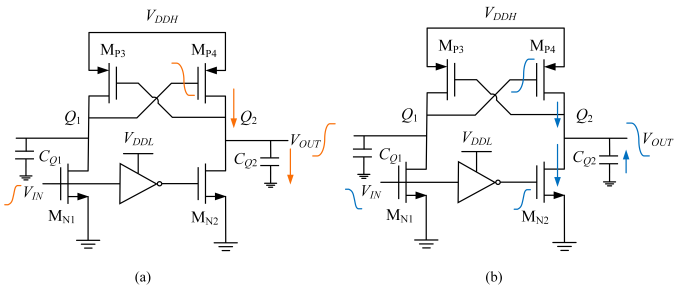

Fig. 3 The operation of a cross-coupled level-shifter upon (a) an input rising transition (b) an input falling transition.

3. Transition Time and Short-circuit Energy Models of Level-Shifters

Fig.3(a) shows the schematic of a cross-coupled level-shifter between the low V_{DD} domain, V_{DDL} , and the high V_{DD} domain, V_{DDH}. As the input signal V_{IN} turns from V_{SS} to V_{DDL}, M_{N1} switches on so that node Q_1 is pulled down. Thereafter, M_{P4} gradually turns on to pull up node Q_2 to V_{DDH}, so that M_{p3} is switched off. An input falling transition leads to a similar operation process as shown in Fig.3(b). To ensure the successful operation, NMOS transistors should have a larger driving strength than PMOS transistors at the rising input (Fig.3(a)). Therefore, the aspect ratio of NMOS transistors is larger than that of the PMOS transistor.
To model the output transition time ($\tau_{out,ls}$)and the transition loss of a level-shifter, the following assumptions are made.
(a) The input signal for the level-shifter features an identical rising and falling transition time denoted as $\tau_{in,ls}$.
(b) M_{N1} and M_{N2} have an identical gate width of $W_{n,ls}$ and M_{P3} and M_{P4} have an identical gate width of $W_{p,ls}$. Both NMOS and PMOS transistors feature an identical gate length of L_{ls}.
(c)The internal inverter in the level-shifter is assumed to perform an ideal inversion, i.e., the input waveforms of M_{N1} and M_{N2} are completely symmetric with opposite phases.
(d) The level-shifter is assumed to be open-loaded since it seldom directly drives the actual load.
These assumptions can greatly simplify the analysis and renders CV-EOTBs to satisfy the engineering requirement.

3.1 Output Transition Time Balancing Scheme

A primary requirement for level-shifter designs is to achieve equalized output rising and falling transition times, i.e., $\tau_{r,ls} = \tau_{f,ls}$. Fig.3(a) shows the operation upon an input rising transition. The arrows indicate the transient current flow directions. Since M_{N2} is turned off before M_{P4} is turned on, there is no contention and the output rising transition is calculated as,

$$C_{Q2}\frac{\mathrm{d}V_{Q2}}{\mathrm{d}t} = I_{MP4} \tag{10}$$

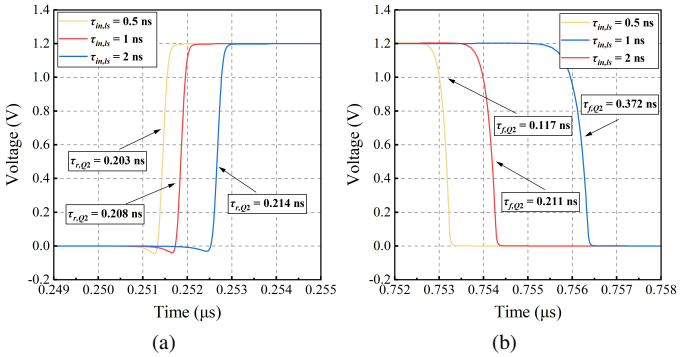

Fig. 4 The uneven impacts on the output transition times due to input transition time variations. Output (a) rising and (b) falling waveforms

where C_{Q2} is the capacitance at node Q_2.
Fig.3(b) shows the operation of the level-shifter upon an input falling transition. In this case, there is a contention between M_{P4} and M_{N2}. Hence, the output voltage satisfies the following relationship,

$$I_{MN2} + C_{Q2}\frac{\mathrm{d}V_{Q2}}{\mathrm{d}t} = I_{MP4} \tag{11}$$

It is observed from equations and that $\tau_{in,ls}$ has uneven impacts on $\tau_{r,ls}$ and $\tau_{f,ls}$. Fig.4 and 5 demonstrate a set of exemplary simulation results, where $V_{DDL} = 0.9V, V_{DDH} = 1.2V, W_{n,ls} = 2.8\mu m, W_{p,ls} = 0.22\mu m$,and $L_{ls} = 0.18\mu m$. When $\tau_{in,ls}$ varies from 0.5 ns to 2 ns, $\tau_{f,ls}$ changes from 0.117 ns to 0.372 ns (Fig. 4(b)), while $\tau_{r,ls}$ only experiences a relatively small change from 0.203 ns to 0.214 ns (Fig.4(a)).
Fig.5 summarizes the dependence of output transition times on $\tau_{in,ls}$. It shows that $\tau_{f,ls}$ features a linear dependence on $\tau_{in,ls}$, while $\tau_{r,ls}$ shows a relative independency. As $\tau_{in,ls}$ increases, level-shifter sizes must be adjusted accordingly to guarantee $\tau_{r,ls} = \tau_{f,ls}$. It is achieved by increasing $W_{n,ls}/W_{p,ls}$. The relationship between $W_{n,ls}/W_{p,ls}$ and $\tau_{in,ls}$ can be concluded as,

$$\frac{W_{n,ls}}{W_{p,ls}} = s_1\tau_{in,ls} + s_2 \tag{12}$$

where $s_1(ns^{-1})$ and s_2 are the fitting parameters which can be obtained from SPICE simulations.
It is also empirically observed that the $W_{n,ls}/W_{p,ls}$ ratio is inversely proportional to L_{ls}. Therefore, a sizing factor, β, is proposed as follows,

$$\beta = \frac{W_{n,ls}L_{ls}}{W_{p,ls}L_{min}} = s_1\tau_{in,ls} + s_2 \tag{13}$$

Table 2 enlists the values of s_1 and s_2 for different V_{DDL} and V_{DDH}.

3.2 Short-circuit Energy Model

The switching loss of a level-shifter comprises the dynamic

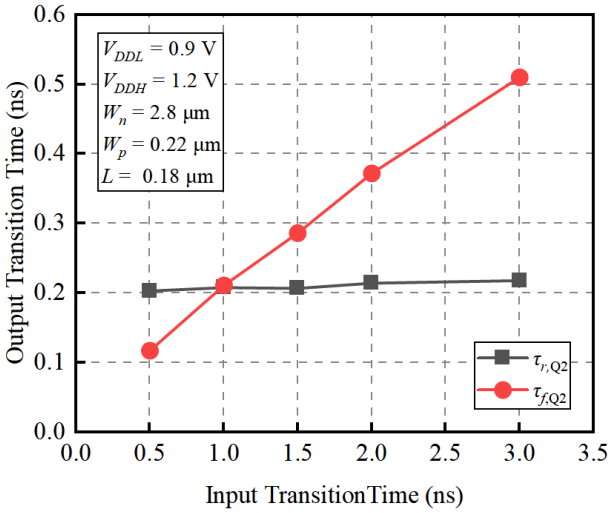

Fig. 5 Output transition times with varying input transition times.

Table 2 Parameters for the Sizing Factor Model at Different V_{DDL} and V_{DDH} Conbinations

$V_{DDH}(V)$	$V_{DDL}(V)$	$s_1(ns^{-1})$	s_2
1.8	1.5	6.389	6.278
1.8	1.2	14.167	4.056
1.5	1.2	9.722	2.778
1.8	0.9	12.89	7.629
1.5	0.9	14.167	4.444
1.2	0.9	10.278	0.167

and the short-circuit energies. While the dynamic energy has a similar form as that of an inverter, its short-circuit energy, $E_{sc,ls}$, is heavily dependent on $\tau_{in,ls}$ and transistor sizes. The impact of $\tau_{in,ls}$ is proportional to the aspect ratio of the PMOS transistors. Therefore, a scale factor, k, is introduced as follows,

$$k = \frac{W_{p,ls}/L_{ls}}{W_{p,min}/L_{min}} \tag{14}$$

where $W_{p,min}$ is the minimum width of PMOS transistors. $E_{sc,ls}$ features its linear dependence on the product of $\tau_{in,ls}$ and k, and is modeled as follows,

$$E_{sc,ls} = r_1 k\tau_{in,ls} + r_2 \tag{15}$$

where $r_1(pJ/ns)$ and $r_2(pJ)$ are curve-fitting parameters. Table 3 lists the values of r_1 and r_2 for different V_{DDL} and V_{DDH}. The accuracies of the fitting models in Eqs.(13) and (15) are intuitively illustrated in Fig.6, which shows the fitting results for $V_{DDH} = 1.8V$ and $V_{DDL} = 0.9V$. The fitting functions are remarkably close to the SPICE simulation results.
$\tau_{out,ls}$ can be calculated as either the rising or the falling transition times since they are equal. The output resistance can be expressed as,

$$R_{eq,p} = R_{eq,p0}/k \tag{16}$$

where $R_{eq,p0}$ is the output resistance of the PMOS transistor

Table 3 Parameters for $E_{sc,ls}$ model at Different V_{DDL} and V_{DDH} Conbinations

$V_{DDH}(V)$	$V_{DDL}(V)$	$r_1(pJ/ns)$	$r_2(pJ)$
1.8	1.5	0.1096	0.00029
1.8	1.2	0.0878	−0.00143
1.5	1.2	0.0346	0.021
1.8	0.9	0.0459	0.1233
1.5	0.9	0.0342	0.0328
1.2	0.9	0.01292	0.0222

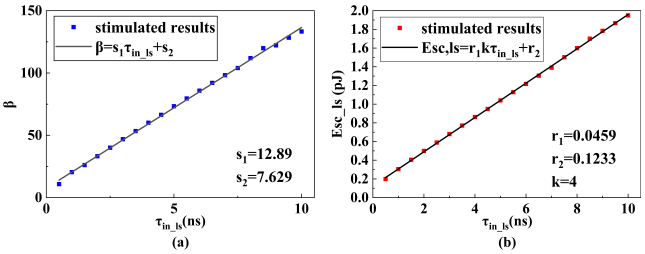

Fig. 6 Comparisons between the SPICE simulation results of (a) β and (b) $E_{sc,ls}$ with the fitting functions for $V_{DDH} = 1.8V$ and $V_{DDL} = 0.9V$.

with $W_{p,min}$ and L_{min}. The output transition time of the level-shifter is proportional to $R_{eq,p}C_{Q2}$. For example, the transition time from 10% V_{DDH} and 90% V_{DDH} takes about $2.2R_{eq,p}C_{Q2}$.

4. Design Strategy for Single-V_{DD} EOTBs

Performance evaluation of tapered buffers relies on the estimation of the equivalent load capacitances of each stage as shown in Fig.7. In a tapered buffer, the load capacitance of the i-th stage ($i \geqslant 1$), C_i, is composed of the output capacitance of the i-th stage, $C_{out,i}$, and the input gate capacitance of the (i+1)-th stage, $C_{g,i+1}$. For each stage, a fixed process-dependent ratio, γ, exists between the output and input capacitances, i.e., $C_{out,i} = \gamma C_{g,i}$.
Therefore, C_i can be expressed as[32],

$$C_i = (1+S)(W_{n,i+1}L_{i+1} + \gamma W_{n,i}L_i)C_{ox} \tag{17}$$

where the widths of the NMOS and PMOS transistors in the i-th stage are represented as $W_{n,i}$ and $W_{p,i}$, respectively, with a ratio of S. Their gate lengths are denoted as L_i.
Fig.7 shows the circuit schematic of a single-V_{DD} N-stage tapered buffer where R_s is the source resistance and $C_{L,tb}$ is the load capacitance. The output transition time and short-circuit energy of each stage can be calculated according to Eqs.(5) and (9). The design of a single-V_{DD} EOTB is essentially to minimize the overall transition loss, E_{tot}, while meeting the output transition time specification, $\tau_{tb,spec}$, i.e.,

$$\begin{cases} E_{eotb} & = \min E_{tot} = \min \sum_{i=1}^{N}(E_{dyn,i} + E_{sc,i}) \\ \tau_{tb} & = \tau_N \in [\tau_{tb,spec} - \Delta\tau, \tau_{tb,spec} + \Delta\tau] \end{cases} \tag{18}$$

where E_{eotb} is the total energy dissipation of the EOTB,

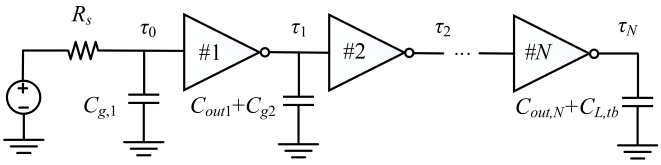

Fig. 7 Circuit model of a single-V_{DD} N-stage tapered buffer.

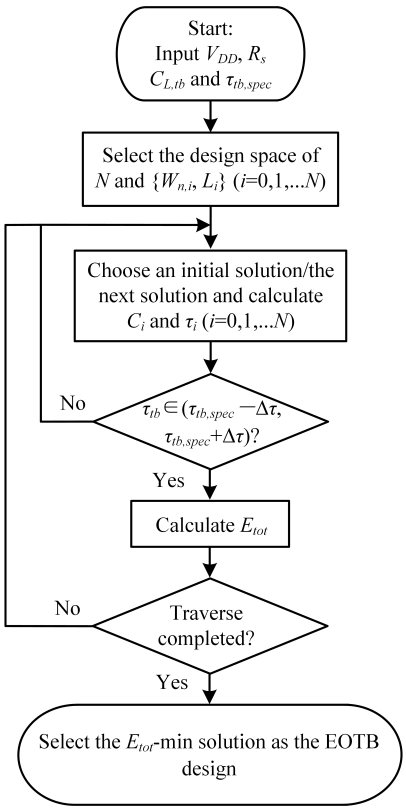

Fig. 8 Traversal algorithm for the EOTB design.

while $E_{dyn,i}$ and $E_{sc,i}$ represent the dynamic and short-circuit energy dissipation of the i-th stage in the tapered buffer, respectively. τ_N is the output transition time of the N-th stage, and $\Delta\tau$ is the acceptable error margin of the output transition time, τ_{tb}. A computer-aided traversal algorithm is proposed accordingly as shown in Fig.8. $\tau_{tb,spec}$ is determined according the application requirements, i.e., the driving capability of the tapered buffer. And, E_{eotb} is the minimum energy consumption among that of all feasible designs that satisfy $\tau_{tb,spec}$. It is worth mentioning that the ideality of the optimal design is determined by the range of the design set and the step size of the travesal algorithm. There is a trade-off between the accuracy and the algorithm execution time.

5. Design Strategy of CV-EOTBs

As E_{sc} increases with V_{DD}[33], it is favorable to adopt a lower V_{DD} at the front-end stages of tapered buffers to reduce power consumption and a higher V_{DD} at the back-

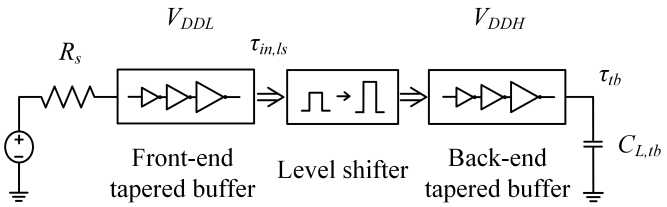

Fig. 9 Circuit schematic of a cross-V_{DD} tapered buffer.

end stages to ensure driving capabilities as depicted in the circuit schematic in Fig.9. Such implementations require cross-V_{DD} level-shifters and are referred to as CV-EOTBs in this work.

5.1 CV-EOTB Design

The CV-EOTB design should start from the sizing of the level-shifter as it influences the load capacitance of the front-end buffer (denoted as $C_{L,fe}$) and the source resistance of the back-end buffer (denoted as $R_{s,be}$). $C_{L,fe}$, i.e., input capacitance of the level-shifter, is calculated as follows,

$$C_{L,fe} = W_{n,ls} L_{ls} C_{ox} \tag{19}$$

$R_{s,be}$, i.e., $R_{eq,p}$ of the level-shifter, is determined by k. $\tau_{in,ls}$ and k determine $E_{sc,ls}$ according to Eqs.(15). It also partially determines the size of the NMOS transistor according to Eqs.(13). To simplify the algorithm, when $k > 1$, L_{ls} is chosen to be the minimum size and $W_{p,ls}$ is increase to satisfy k. Conversely, when $k < 1$, $W_{p,ls}$ is chosen as the minimum size and L_{ls} is increased.
Therefore, a traversal algorithm based on $\tau_{in,ls}$ and k is employed to achieve the optimized CV-EOTBs design. The algorithm flow is shown in Fig.10. As $C_{L,fe}$ and $R_{s,be}$ can be calculated for any combination of $\tau_{in,ls}$ and k, the CV-EOTB design problem is transformed to the low-energy design of the front-end and back-end buffers, respectively. Their switching losses are is denoted as $E_{fe,eotb}$ and $E_{be,eotb}$, respectively, while that of the level-shifter is denoted as E_{ls}. The design constraints for front-end and back-end EOTBs are summarized in Table 4.

5.2 CV-EOTB Design Example

A design case (CV-EOTB Design #1) is presented to exemplify the proposed CV-EOTB design procedure. The design constraints are the following: $V_{DDL} = 1.2V, V_{DDH} = 1.8V, R_s = 100M\Omega, C_{L,tb} = 200fF$,and $\tau_{tb,spec} = 1ns$. Through the optimization algorithm, k and $\tau_{in,ls}$ are determined to be 0.123 and 1 ns, respectively. β is calculated to be 18.22 according to Eqs.(13). Therefore, $W_{n,ls}, W_{p.ls}$ and L_{ls} are determined to be 0.49 μm,0.22 μm and 1.47 μm, respectively. The front-end and back-end EOTB designs are obtained according to the EOTB design procedure in Fig.8. The optimized solutions are presented in Table 5 and Table 6, respectively.

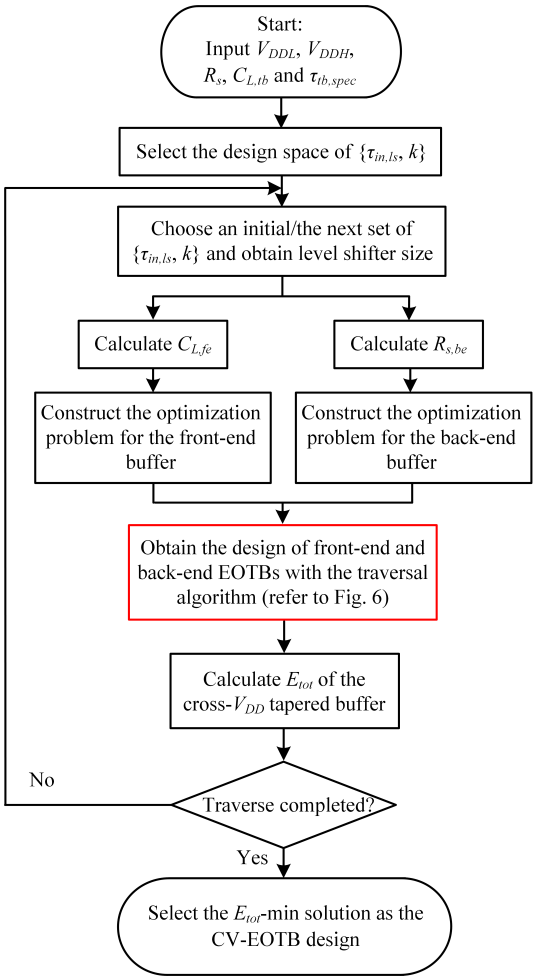

Fig. 10 Optimization flow of the CV-EOTB.

In this design, $E_{fe,eotb}, E_{be,eotb}$ and E_{ls} are estimated to 0.51 pJ, 0.71 pJ, and 0.06 pJ, respectively, which sum to be 1.28 pJ(denoted as $E_{cv,eotb}$). In contrast, transistor-level SPICE simulation leads to $E_{fe,eotb}, E_{be,eotb}$ and E_{ls} of 0.86 pJ, 0.77 pJ and 0.09 pJ, respectively, which sum to be 1.72 pJ. Both results are remarkably close which validates the proposed design procedure.

6. Performances of EOTBs and CV-EOTBs

The proposed single- V_{DD} EOTB design strategy is applied in four design cases(Case #B1, Case #B2, Case #B3, Case #B4) each with different design constraints as listed in Appendix B. The estimated τ_{tb} and E_{eotb} results are compared with those obtained from SPICE simulations, and the average errors of this four cases are only 16.43% and 8.65%,

Table 4 Design Constraints for Front-end and Back-end EOTBs in a CV-EOTB Design

External conditions	Front-end EOTB	Back-end EOTB
Source resistance	R_s	$R_{s,be}$
Load capacitance	$C_{L,fe}$	$C_{L,tb}$
Output transition time specification	$\tau_{in,ls}$	$\tau_{tb,spec}$

Table 5 Front-end EOTB Design in CV-EOTB Design #1

i	$W_{n,i}\,(\mu m)$	$L_i\,(\mu m)$
1	0.22	0.5
2	0.3	0.5
3	0.4	0.58

Table 6 Back-end EOTB Design in CV-EOTB Design #1

i	$W_{n,i}\,(\mu m)$	$L_i\,(\mu m)$
1	0.22	0.4
2	0.3	0.3
3	0.6	0.18

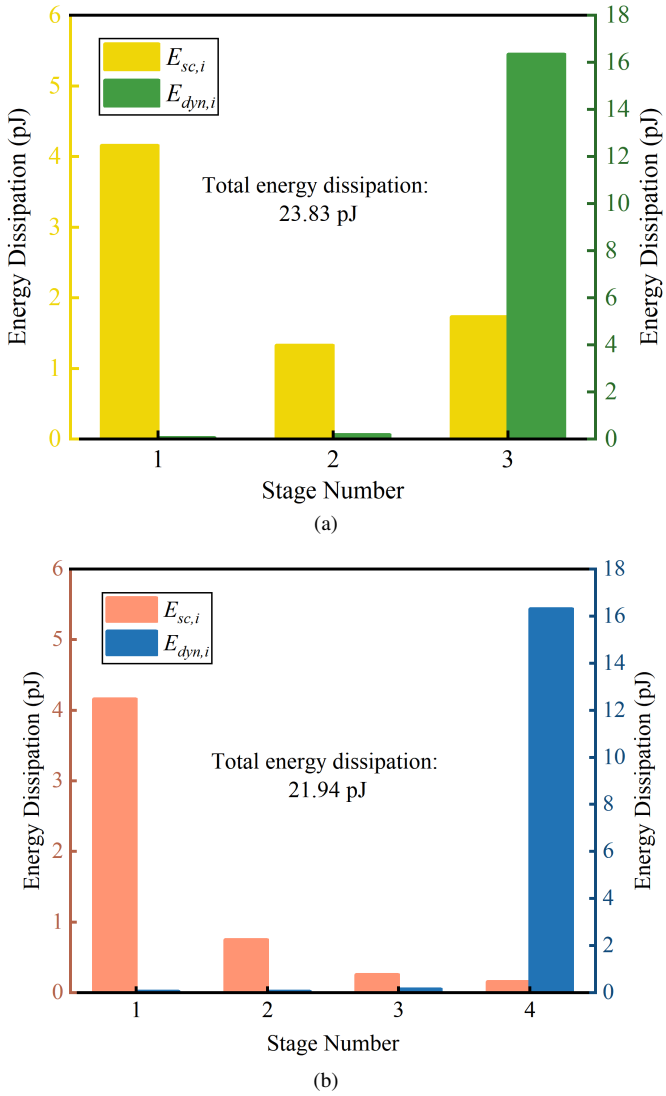

Fig. 11 Energy distribution in EOTBs (a) The 3-stage EOTB design. (b) the 4-stage EOTB design.

respectively. These four examples encompass V_{DD} from 0.9V to 1.8V, R_s from 30MΩ to 1GΩ, C_L from 0.5pF to 5pF, and $\tau_{tb,spec}$ from 1ns to 20ns, which are typical values in practical applications.

As a key variable in the optimization procedure, the effect

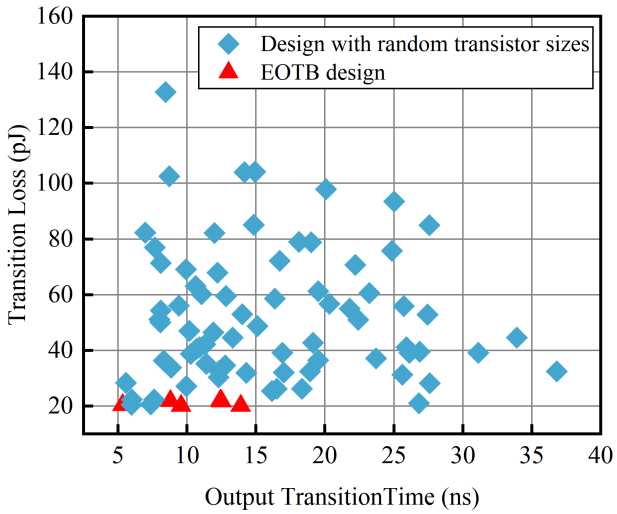

Fig. 12 Performance of the EOTB design compared to the design with random gate sizes.

of N is demonstrated in an example in Fig.11. For $V_{DD} = 1.8V, R_s = 50M\Omega, C_{L,tb} = 5pF$, and $\tau_{tb,spec} = 8ns$, the design of EOTBs for $N = 3$ and $N = 4$ are shown in Fig.11(a) and 11(b), respectively. The 4-stage EOTB achieves a lower E_{eotb} thanks to the reduction of E_{sc}. It is also worth noting that, for an N-stage EOTB, E_{sc} of the first stage and E_{dyn} of the last stage usually take a dominant part.

Fig.12 plots the optimized designs of a 3-stage EOTB for $V_{DD} = 1.8V, R_s = 100M\Omega, C_{L,tb} = 3pF$ and $\tau_{tb,spec} \in (5ns, 15ns)$. Tapered buffers with random optimized sizes are demonstrated for comparison, in which the gate widths and lengths have been randomly modified (always with $W_{n,1} < W_{n,2} < W_{n,3}$). For any $\tau_{tb,spec}$, the EOTB design achieves the lowest transition loss.

Fig.13(a) and 13(b) displays the size, E_{sc}, and E_{dyn} of each stage of an optimized single-V_{DD} EOTB design, where $V_{DD} = 1.8V, R_s = 100M\Omega, C_{L,tb} = 3pF, \tau_{tb,spec} = 5ns$. Fig.13(c) and 13(d) demonstrate the corresponding transient voltage and the transient current waveforms, respectively.

Based on the accurate modeling of EOTBs, the design of CV-EOTBs is transformed to the that of the front-end and back-end EOTBs along with a level shifter. Fig.14 displays the transition losses of CV-EOTB-design #1 and the single-V_{DD} EOTB design assuming the same constraints and the supply of V_{DDH}. For the single-V_{DD} EOTB, E_{sc} alone is estimated to be 10.68 pJ, according to SPICE simulations and E_{eotb} is estimated to be 11.35 pJ. In contrast, CV-EOTB-design #1 reduces the transition loss by 84.8%. Corner simulations are performed for CV-EOTB-design #1. It shows that the effects of potential process variations are limited. Table 7 enlists $E_{cv,eotb}$ and τ_{tb} of CV-EOTB-Design #1 with different process corners.

7. Conclusion

The low-power design of taper buffers is crucial for a series of switch-mode analog applications. This paper proposes the

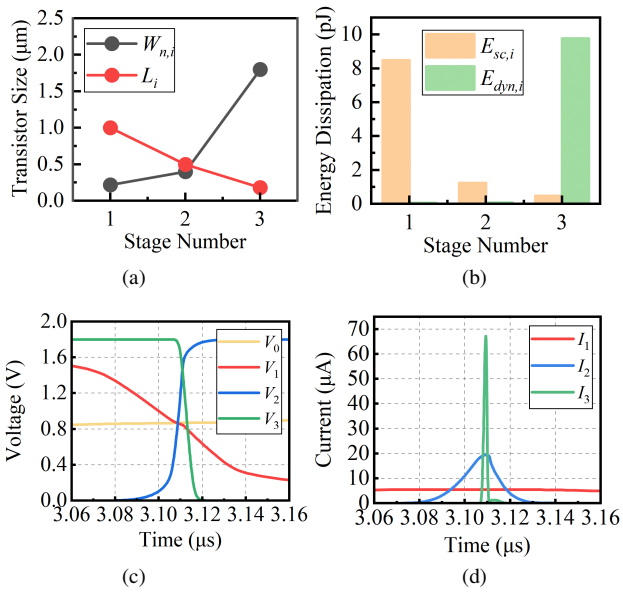

Fig. 13 A 3-stage EOTB design. (a) Buffer sizes. (b) Short-circuit and dynamic energy dissipation of all stages. (c) Transient voltage waveforms of all stages. (d) Transient current waveforms of all stages.

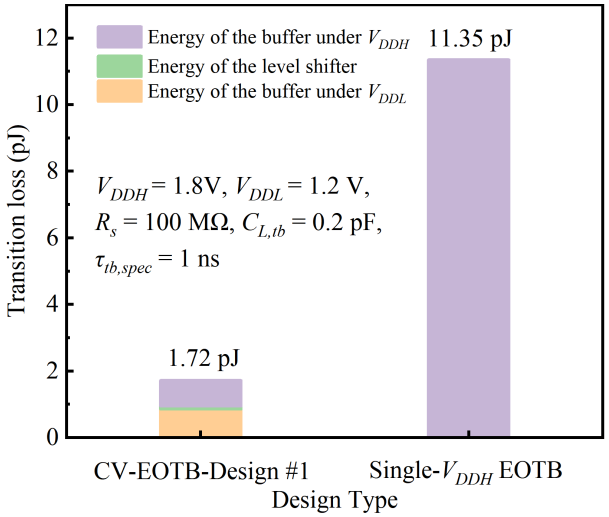

Fig. 14 Transition losses in CV-EOTB-Design #1 and the single-V_{DD} EOTB.

optimization procedure for taper buffers based on analytical models of τ_{out} and E_{sc} of CMOS inverters and level-shifters. Computer-aided traversal algorithms for the single-V_{DD} EOTB and CV-EOTB optimization are proposed with the latter being transformed to the front-end and back-end single-V_{DD} designs, respectively. The proposed design procedures are validated against SPICE simulation results manifesting their effectiveness in addressing practical engineering problems.

Table 7 Process corner simulations of CV-EOTB-Design #1

Process corner	TT	SS	FF	SF	FS
$E_{cv,eotb}(pJ)$	1.72	1.26	2.65	1.78	1.75
$\tau_{tb}(ns)$	0.87	0.99	0.77	0.88	0.87

Appendix A: Sub-model Parameters of Inverters

Table A· 1 Sub-model Parameters With 1.8 V V_{DD} and 180-nm Technology

Sub-model	$p1$	$p2$	$k1$	$k2$
$M_{0.1,1}$	14.163	1.601	0.0896	1.9094
$M_{1,10}$	19.2	0.868	0.1202	2.0268
$M_{10,100}$	0.892	6.91	0.1202	2.0268
$M_{100,1000}$	0.366	5.718	1.2884	1.7576
$M_{1000,10000}$	−0.0025	14.606	0	42.373
$M_{10000,100000}$	0.00017	14.116	0	42.373

Table A· 2 Sub-model Parameters With 1.5 V V_{DD} and 180-nm Technology

Sub-model	$p1$	$p2$	$k1$	$k2$
$M_{0.1,1}$	13.395	1.425	−0.1028	5.8222
$M_{1,10}$	18.536	0.745	0.324	7.2744
$M_{10,100}$	1.409	6.612	1.9342	5.7942
$M_{100,1000}$	0.613	4.933	4.8886	5.7568
$M_{1000,10000}$	−0.001	27.526	0	142.86
$M_{10000,100000}$	0.0003	25.92	0	142.86

Table A· 3 Sub-model Parameters With 1.2 V V_{DD} and 180-nm Technology

Sub-model	$p1$	$p2$	$k1$	$k2$
$M_{0.1,1}$	11.68	1.23	−0.6332	18.7282
$M_{1,10}$	16.998	0.586	25.336	27.9666
$M_{10,100}$	1.575	5.064	17.7742	39.4496
$M_{100,1000}$	0.752	4.13	36.3968	35.4432
$M_{1000,10000}$	0.02	30.129	0	555.56
$M_{10000,100000}$	−0.0002	16.747	0	555.56

Table A· 4 Sub-model Parameters With 0.9 V V_{DD} and 180-nm Technology

Sub-model	$p1$	$p2$	$k1$	$k2$
$M_{0.1,1}$	12	0.5199	−1.2254	32
$M_{1,10}$	14.88	0.2582	140.88	−577.2
$M_{10,100}$	0.6946	3.651	−3571.4	1313.2
$M_{100,1000}$	0.3676	3.163	−219.6	947.8
$M_{1000,10000}$	0.01611	8.838	0	8333
$M_{10000,100000}$	−0.006087	32.33	0	8333

Appendix B: Single-V_{DD} EOTB Design Cases

Table B· 1 Case #B1:180-nm Technology, V_{DD}=1.8 V, R_s=100 MΩ, $C_{L,tb}$=1 pF, $\tau_{tb,spec}$=2 ns

i	$W_{n,i}(\mu m)$	$L_i(\mu m)$	$\tau_{i-1,est}(ns)$	$\tau_{i-1,sim}(ns)$	$E_{i,est}(pJ/op)$	$E_{i,sim}(pJ/op)$
1	0.22	0.9	1647	1552	9.6	8.68
2	0.3	1	113	170	0.102	0.54
3	0.4	0.7	18	9.08	0.0836	0.11
4	1	0.18	2.41	1.12	3.31	3.31
			2.14	2.69	13.1	12.6

Table B· 2 Case #B2:180-nm Technology, V_{DD}=1.5 V, R_s=1 GΩ, $C_{L,tb}$=0.5 pF, $\tau_{tb,spec}$=5 ns

i	$W_{n,i}(\mu m)$	$L_i(\mu m)$	$\tau_{i-1,est}(ns)$	$\tau_{i-1,sim}(ns)$	$E_{i,est}(pJ/op)$	$E_{i,sim}(pJ/op)$
1	0.22	0.5	7323	7259	28.2	38
2	0.3	0.8	302.4	907	0.191	2
3	0.5	0.3	30.67	34.95	0.153	0.305
4	4	0.18	3.474	3.223	1.508	1.538
			1.001	0.958	30.07	41.87

Table B· 3 Case #B3:180-nm Technology, V_{DD}=1.2 V, R_s=30 MΩ, $C_{L,tb}$=5 pF, $\tau_{tb,spec}$=10 ns

i	$W_{n,i}(\mu m)$	$L_i(\mu m)$	$\tau_{i-1,est}(ns)$	$\tau_{i-1,sim}(ns)$	$E_{i,est}(pJ/op)$	$E_{i,sim}(pJ/op)$
1	0.22	1.1	604.1	501.9	0.142	0.21
2	0.3	0.5	57.3	31.5	0.0277	0.052
3	2	0.18	7.23	4.25	7.22	7.25
			8.42	10.04	7.39	7.51

Table B· 4 Case #B4:180-nm Technology, V_{DD}=0.9 V, R_s=200 MΩ, $C_{L,tb}$=2 pF,$\tau_{tb,spec}$=20 ns

i	$W_{n,i}(\mu m)$	$L_i(\mu m)$	$\tau_{i-1,est}(ns)$	$\tau_{i-1,sim}(ns)$	$E_{i,est}(pJ/op)$	$E_{i,sim}(pJ/op)$
1	0.22	1.2	4394	3204	0.178	0.119
2	0.4	0.8	466	171.7	0.0168	0.04
3	3	0.38	63.9	27.1	1.63	1.65
			16.7	13.4	1.82	1.81

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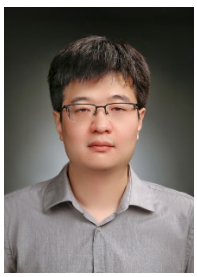

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