Digital/Analog-Operation of Hf-based FeNOS Nonvolatile Memory utilizing Ferroelectric Nondoped HfO$_2$ Blocking Layer

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SUMMARY

In this research, we investigated the digital/analog-operation utilizing ferroelectric nondoped HfO$_2$ (FeND-HfO$_2$) as a blocking layer (BL) in the Hf-based metal/oxide/nitride/oxide/Si (MONOS) nonvolatile memory (NVM), so called FeNOS NVM. The Al/HfN$_{0.5}$/HfN$_{1.1}$/HfO$_2$/p-Si(100) FeNOS diodes realized small equivalent oxide thickness (EOT) of 4.5 nm with the density of interface states ($D_{it}$) of $5.3 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ which were suitable for high-speed and low-voltage operation. The flat-band voltage ($V_{FB}$) was well controlled as 80-100 mV with the input pulses of $\pm 3$ V/100 ms controlled by the partial polarization of FeND-HfO$_2$ BL at each 2-bit state operated by the charge injection with the input pulses of $\pm 8$ V/1-100 ms.

**key words:** ferroelectric nondoped HfO$_2$, metal/oxide/nitride/oxide/Si, nonvolatile memory, partial polarization, charge trap

1. Introduction

Metal-oxide-nitride-oxide-Si (MONOS) nonvolatile memories (NVM) are widely investigated not only for storage memory but for in-memory computing applications [1, 2]. Utilizing the high-k (HK) thin films in MONOS NVM is effective to reduce the operation voltage and improve the operation speed [3, 4]. The memory window (MW) of MONOS NVM is necessary to be increased even when the operation voltage is decreased. In order to increase the MW, metal-ferroelectrics-nitride-oxide-Si (MFNOS) structure was proposed utilizing Sr$_{0.7}$Bi$_{2.3}$Nb$_2$O$_9$ (SBN) as a ferroelectric blocking layer (BL) for further improvement of memory characteristics of MONOS NVM [5]. However, the thickness of SBN was 100 nm to obtain the ferroelectric characteristics, and it was hard to be scaled although the relative dielectric constant ($\epsilon_r$) was high as 1000.

Since the HfO$_2$ thin film crystallized in the metastable orthorhombic phase was reported to show ferroelectric characteristics [6], the applications of ferroelectric HfO$_2$ in the MONOS structure have been attracting much attention because of its Si process compatibility, and the HfO$_2$ shows ferroelectric characteristics even bellow the thickness of 10 nm which is suitable for device scaling [7, 8]. The ferroelectric HfO$_2$ is effective to increase MW which is similar to the Ref. 3.

Fig. 1  (a) Schematic cross-section of the FeNOS NVM and (b) schematics of $V_{th}$ control in FeNOS NVM. The partial polarization of FeND-HfO$_2$ BL realizes the analog control of $V_{th}$ (dotted lines) along with the multi-bit/cell operation of the charge trap in the HfN$_{1.1}$ CTL (solid lines).

We have proposed the digital/analog-operation utilizing ferroelectric nondoped HfO$_2$ (FeND-HfO$_2$) as a BL in the Hf-based MONOS structure, which is called FeNOS NVM, as shown in Fig. 1(a) [9-12]. The FeND-HfO$_2$ was able to be formed when the nitrogen concentration of HfN$_x$ CTL was $x=1.1$. The Hf-based FeNOS stacked structures from the HK-HfO$_2$ tunneling layer (TL) to the HfN$_{0.5}$ gate electrode layer are able to be deposited in a sputtering chamber by reactive sputtering process without exposing to the air. The FeNOS NVM is expected to realize the analog control of threshold voltage ($V_{th}$) by the partial polarization of FeND-HfO$_2$ BL along with the multi-bit/cell operation by the charge trap in the HK-HfN$_{1.1}$ CTL through a HK-HfO$_2$ TL as shown in Fig. 1(b). The polarization switching is able to be controlled at low-voltage and the switching speed is quite fast, while the charge trap and detrap operations are performed at high-voltage.

In this paper, we have investigated the fabrication process of Hf-based FeNOS diode, and the digital/analog-operation of Hf-based FeNOS diode was examined by controlling the pulse input conditions [13].

2. Experimental Procedure

Figure 2 shows the fabrication process for the FeNOS diodes. The schematic cross-sections and the plane-view of the fabricated FeNOS diodes are also shown.

For the fabrication of FeNOS diodes, lightly doped p-
Si(100) (10−30 Ωcm) substrates were cleaned by sulfuric-peroxide mixture (SPM) and diluted HF (DHF) solutions. After the 100 nm thick field SiO₂ formation on p-Si(100) substrates, active area was patterned. Some of the FeNOS diodes were fabricated without field oxide. Then, the Hf-based FeNOS structures of HfN₀.₅ (gate electrode, 10 nm)/FeₙD-HfO₂ (10-15 nm)/HfN₁.₁ (3 nm)/HK-HfO₂ (2 nm)/Si(100) were in-situ deposited by the electron cyclotron resonance (ECR)-plasma sputtering at room temperature (RT) followed by the post-metallization annealing (PMA) at 350 °C/1-10 min in N₂ ambient. For the HK-HfO₂ TL deposition, the Ar/O₂ flow ratio was 23/4.6 sccm, while it was 16/2.4 sccm for the FeₙD-HfO₂ BL deposition. The Ar/N₂ flow ratio for HfN₁.₁ CTL was 8/6 sccm, while it was 10/0.2 sccm for the HfN₀.₅ gate electrode deposition. Next, Al top contact was evaporated, and the gate electrode was patterned by wet etching with the size of 100 × 100 μm².

The FeNOS diode structures were evaluated by C-V, J-V, and program/erase (P/E) measurements utilizing HP 4284A and Agilent 4156C, respectively. The density of interface states (Dᵢ) was extracted by Terman method at midgap [14]. The equivalent oxide thickness was extracted from the C-V measurement considering the quantum effect [15]. The charge centroid (Zₑᵢ) for the charge trap operation was evaluated utilizing HP8110A, Keithley6517A, and KEYSIGHT DAQ970A [16]. The crystallinity was evaluated by the x-ray diffraction (XRD).

3. Results and Discussion

Figure 3 shows the PMA duration dependence of the C-V and J-V characteristics for the Al/HfN₀.₅/HfNₙ₁.₁(10 nm)/HfO₂/p-Si(100) FeNOS diodes. As shown in Fig. 3(a), the minimum EOT of 4.5 nm was obtained with negligible hysteresis by the PMA at 350°C/5 min. The Dᵢ was extracted as 5.3 × 10¹⁰ eV/cm². The leakage current was decreased to 1 × 10⁻⁸ A/cm² at Vₑ = −1 V by the PMA at 350°C/5 min compared to the PMA at 350°C/1 min.
The leakage current was increased in case of the PMA at 350 °C/10 min so that the PMA with long duration seemed to degrade the film quality even at the low annealing temperature such as 350 °C. Figure 4 shows the XRD patterns of FeNOS structures. The peak intensity of orthorhombic HfO2(111) was found to be increased by the PMA at 350 °C/5 min, while it was decreased by the PMA at 350 °C/10 min. Therefore, the 350 °C for 5 min seemed to be the optimum PMA condition for the FeNOS structures.

Figure 5 shows the retention characteristic for charge trap operation of FeNOS diode with PMA at 350 °C/5 min. The input pulses were ±8 V/100 ms for charge trap operation.

The charge centroid (Z_{eff}) was evaluated by changing the program pulses as V_{PGM}/t_{PGM} : 8 V/1-100 ms. Figure 6 shows the pulse width dependence on the Z_{eff} of FeNOS diode. The Z_{eff} was extracted utilizing the following equation,

\[ Z_{eff} = \frac{\varepsilon_{ox} \Delta V_{FB}}{\int_{V_{FB}}^{0} C(V) dV + Q_m} \]

where Q_m is the measured charge, \( \varepsilon_{ox} \) is the dielectric constant of HfO2 BL, and V_{FB} is the flat-band voltage.

As shown in Fig. 6, the Z_{eff} was located at the interface of FeN_{0.5}-HfO_{2.4} HfN_{1.1} CTL even for the program pulse of V_{PGM}/t_{PGM} : 8 V/1 ms. Interestingly, the Z_{eff} was not markedly changed for the longer pulse such as V_{PGM}/t_{PGM} : 8 V/100 ms. This is probably because the density of trap sites in the HfN_{1.1} CTL is large enough to accept the charge injection by the program conditions.

Finally, the charge trap and partial polarization operations were examined utilizing Al/HfN_{0.5}/HfN_{1.1}(15 nm)/HfO_{2}/p-Si(100) FeNOS diodes. Figure 7 shows the charge trap operation utilizing program pulse of V_{PGM}/t_{PGM} = 8 V/1 ms - 1 s. The C-V characteristics were measured at 100 kHz. The schematic measurement sequence was also shown. The P/E input pulses, V_{PGM}/t_{PGM} and V_{ERS}/t_{ERS}, were V_{PGM}/t_{PGM} : 8 V/100 ms and V_{ERS}/t_{ERS} : −8 V/100 ms, respectively. The measurements were carried out until 10^4 s. The initial MW of 2.5 V was observed after P/E input pulses were applied. The estimated MW of 1.1 V after 10 years was obtained which was 44% compared with the initial MW of 2.5 V. This result suggested that reliability of the obtained memory characteristics was good enough even though the annealing temperature was low as 350 °C.

Next, the charge centroid (Z_{eff}) was evaluated by changing the program pulses as V_{PGM}/t_{PGM} : 8 V/1-100 ms. Figure 6 shows the pulse width dependence on the Z_{eff} of FeNOS diode. The Z_{eff} was extracted utilizing the following equation,
charge trap operation utilizing program pulses of $V_{\text{PGM}}/V_{\text{PGM}}$: 8 V/1 ms - 1 s. As shown in Fig. 7, 2 bit/cell operation was demonstrated by the input pulses of $V_{\text{PGM}}/V_{\text{PGM}}$: 8 V/1-100 ms after the initialization by the input pulse of $V_{\text{ERS}}/V_{\text{ERS}}$: -8 V/100 ms with the maximum MW of 1.85 V. Negligible hysteresis was observed for each C-V characteristic after the P/E operations. When the input pulse of 8 V/1 s was applied, the MW was almost same with that of after 8 V/100 ms was applied so that the maximum available charge densities in the HfN$_{1.1}$ CTL was estimated as 0.94 μC/cm$^2$. From the obtained results, the margin of $V_{\text{FB}}$ between each state is large enough so that the further multi-bit/cell operation such as 3 bit or 4 bit/cell operation seems to be available for the FeNOS fabrication fabricated in this research.

Next, the $V_{\text{FB}}$ control by the partial polarization of FeND-HfO$_2$ BL was examined utilizing P/E pulses of $V_{\text{PGM}}/V_{\text{PGM}}$: -3 V/100 ms and $V_{\text{ERS}}/V_{\text{ERS}}$: 8 V/100 ms at ‘11’ and ‘01’ states of charge trap operations. Figure 8 clearly shows that the precise $V_{\text{FB}}$ control by the partial polarization. The erase pulse caused the negative $V_{\text{FB}}$ shift at each state, while the program pulses made $V_{\text{FB}}$ shifted to the positive direction. The $V_{\text{FB}}$ shift was approximately 80-100 mV. The MW of charge trap operation is 1.8 V so that 18-22 states control would be realized by the partial polarization operation.

4. Conclusions

In this paper, we have investigated the digital/analog-operation of Hf-based FeNOS diode. The low-voltage input pulse operation was found to control the partial polarization, and the $V_{\text{FB}}$ shifts of approximately 80-100 mV were realized without causing the charge trap and/or detrapping in the HfN$_{1.1}$ CTL. The $V_{\text{FB}}$ control by the partial polarization is also applicable for the $V_{\text{TH}}$ adjustment after the NVM fabrication. In conclusion, Hf-based FeNOS NVM is a promising memory device not only for storage memory but also for in-memory computing applications.

Acknowledgments

This work was partially supported by JSPS KAKENHI Grant Number 19H00758, NEDO, JST, and CASIO Foundation. The author thanks Mr. W. Zhang and Mr. E.K. Hong for their help in this research.

References


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