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Variable-Gain Phase Shifter with Phase Compensation Using Varactors

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SUMMARY This paper demonstrates a phase compensation technique using varactors for variable-gain phase shifters (VGPSs). The VGPS consists of an I/Q generator and I/Q variable gain amplifiers (I/Q VGAs). I/Q VGAs based on common-emitter stages are enabled to control the gain by adjusting the collector current of the transistor. However, the phase control performance degenerates because the input capacitance varies with the collector current. The proposed phase compensation technique reduces the variation in the insertion phase of the I/Q VGA by adjusting the voltage of the varactor provided at its input and maintaining the input capacitance constant in any gain state. As a result, the VGPS can provide a low phase and amplitude error under phase control. A Ka-band VGPS with the proposed phase compensation technique, fabricated in a 130-nm SiGe BiCMOS process, demonstrates a 0.73° and 0.06 dB improvement in the RMS phase and amplitude error compared with the case without the compensation technique. The VGPS achieves measured RMS amplitude and phase errors of less than 0.19 dB and 0.75°, respectively, in an amplitude control range of more than 20 dB with a frequency range of 28 to 32 GHz.

key words: *vector-sum, variable-gain, phase shifter, phase compensation*

1. Introduction

Recently, active phased array antennas (APAAs), which generate directional beam patterns by electrically controlling the phase and amplitude, have been widely used in 5G communication [1]–[4], satellite communication systems [5]–[7], and radar applications [8], [9]. Massive APAAs, which require a large number of front-end integrated circuits (FE-ICs), have been proposed in silicon technologies, such as CMOS and SiGe BiCMOS, because of their low cost and high integration [10]–[15]. An accurate phase control is required for phase shifters to enable precise beam steering. Generally, vector-sum phase shifters (VSPSs) are suitable circuits for APAA systems because of their ability to provide insertion gain, low phase-shift errors, and a compact area in silicon technology [16]–[22]. Precise amplitude control is also essential for low sidelobe levels to avoid interference from unwanted directions [23]. Variable-gain amplifiers (VGAs), which use current steering or varying transconductances of transistors, have been proposed to control the amplitude [24]–[27]. Conventional methods that use VSPSs and VGAs require a large chip area and high power consumption because they include two functional circuits. Therefore, variable-gain phase shifters (VGPSs) have been proposed to reduce power consumption and area by controlling the phase and amplitude with a single block [14], [23], [28]–[30].

A VGPS, which is based on a VSPS, consists of an I/Q generator and I/Q VGAs. I/Q VGAs can control the amplitude by adjusting the current of the transistor and require that the insertion phase remains constant at any amplitude state to control the phase and amplitude precisely in APAA systems [27]. However, the insertion phase of the I/Q VGA varies owing to the variation in the input capacitance according to amplitude control [28], [31]. This results in the degeneration of the phase and amplitude control performance as VGPS or VSPS. To avoid them, various types of techniques were proposed such as a compensation of the insertion phase variation of VGAs, and calibration of the phase and amplitude control performance as VSPSs. For VGA, it was proposed by adding phase compensation devices such as varactors or current injection elements at output terminals or cascode stages [26], [32], [33]. For VSPS, it was proposed that IQ-VGA characteristics were measured in advance by detection devices on/off-chip, and the optimum control values of IQ-VGA stored in look-up tables (LUTs) or memory are used [34]–[36]. The circuit area and power consumption increase due to detection circuits, LUTs, memory, and complex digital control circuits, although precise phase control can be achieved.

In this paper, we propose a simple phase compensation technique using varactors for the VGPS based on a common emitter-based linear VGA. First, the insertion phase and gain variation of the VGA with respect to the variation in the input capacitance according to amplitude control is analyzed. Then, the amplitude and phase errors of the VGPS by the variations of the VGA are also analyzed. After that, a phase compensation technique derived from the analysis is proposed, in which a varactor is placed at the VGA input terminal and the varactor voltage is controlled linearly to the control voltage of the VGA. The proposed technique reduces the variation in the insertion phase of the VGA by maintaining a constant input capacitance in any phase state without any detection circuits, LUTs, memory, and complex digital control circuits. As a result, the proposed technique can provide low phase and amplitude errors for the VGPS with a small circuit size and low power consumption.

The proposed phase compensation technique for the

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VGPS is described in Sect. 2. The circuit implementation and measurement results of a Ka-band VGPS with the proposed phase compensation technique in a 130-nm SiGe BiCMOS are presented in Sects. 3 and 4, respectively. Finally, the paper is summarized and concluded in Sect. 5.

2. Proposed Phase Compensation Technique for the VGPS and VSPS

This section discusses the proposed phase compensation technique for the VGPS. This technique can be applied to a VSPS and VGPS using VGAs based on common-emitter stages.

2.1 Circuit Configuration

Figure 1 shows the configuration of the proposed VGPS. The VGPS consists of an I/Q generator and I/Q VGAs. The I/Q VGAs are used for phase control with current digital-to-analog converters (DACs) and amplitude control with voltage DACs. In addition, voltage DACs for varactors are used to compensate for the insertion phase of the I/Q VGAs.

The configuration of the VGA is shown in Fig. 2. The VGA consists of two stacked amplifiers composed of common-emitter stages for phase control using IREFP/IREFN and common-base stages for amplitude control using CNTP/CNTN to separate the phase and amplitude control functions in the VGPS.

In the common-emitter stage, amplitude and polarity control for phase control is realized using the collector currents of transistors IP and IN using current DACs. The gain of the common-emitter G_{VGA_CE} is proportional to the difference in current between Q1 (Q4) and Q2 (Q3), as expressed by

$$G_{VGA\_CE} = IP - IN \propto IREFP - IREFN. \tag{1}$$

IP and IN are controlled to maintain a constant I_{total} using the current DACs. I_{total} is the sum of IREFP in Q1 (Q4) and IREFN in Q2 (Q3) as follows:

$$I_{total} = IP + IN \propto IREFP + IREFN. \tag{2}$$

In the common-base stage, the gain for the amplitude control is controlled using V_c, which is the voltage between the base of transistors Q5/Q8 and Q6/Q7. The relationship between the gain of the common-base stage G_{VGA_CB} and V_c is expressed as

$$G_{VGA\_CB} \propto \frac{e^{\frac{V_c}{V_t}}}{e^{\frac{V_c}{V_t}} + 1}, \tag{3}$$

where V_t denotes the thermal voltage. When $V_c = 0$, the insertion gain of the base stage is 1/2 (−6 dB) from the maximum gain. Moreover, the gain is dB-linear with respect to V_c when the insertion gain is small [37]. The common-base stage is suitable for amplitude control in the VGPS because it has a high resolution and wide gain range. The variable transconductance range of the common-base transistors

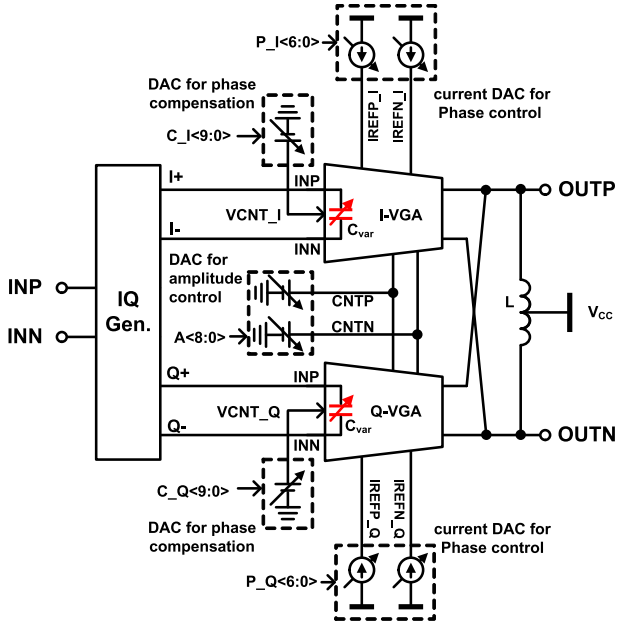


Fig. 1 Configuration of the proposed VGPS.

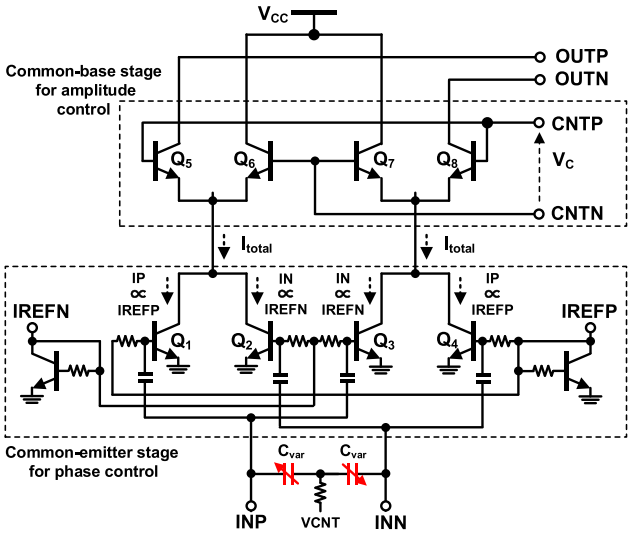


Fig. 2 Configuration of the VGA.

Q5/Q7 and Q6/Q8 is invariant at any phase state because the phase is controlled to maintain a constant I_{total}. Therefore, the gain of the common-base stage can be controlled independently of that of the common-emitter stage.

2.2 Insertion Phase and Gain Variation of VGA with Amplitude Control

In VGPSs or VSPSs, the gain of I/Q VGAs is controlled according to the phase states. The common-emitter VGA is suitable for high-frequency operations because it consists of only four transistors [19], [21], [23], [24]. However, the variation in the input impedance of the I/Q VGAs according to the amplitude control degenerates the phase control per-

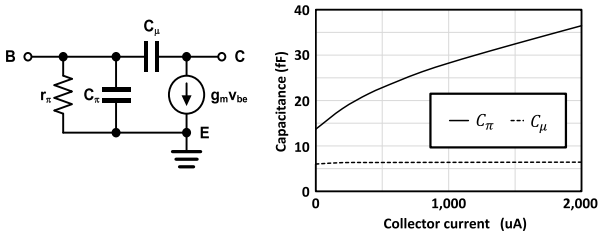


Fig. 3 Equivalent circuit of the bipolar transistor (left) and the simulation results of the collector current dependence of the parasitic capacitances (right), where the transistor size is 0.12 μm/4 μm and the current range is from 0 to 2000 μA.

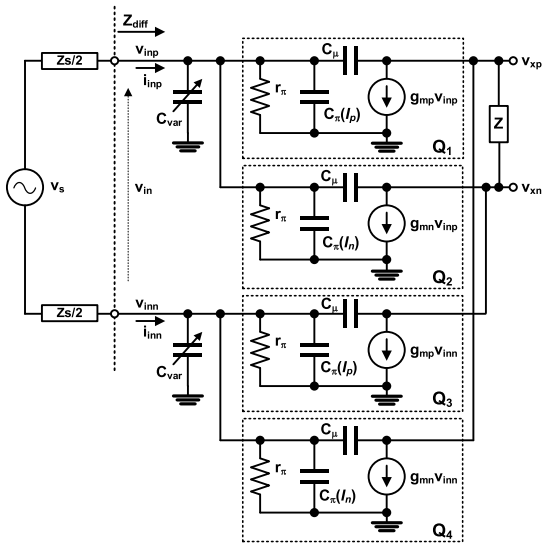


Fig. 4 Small signal equivalent circuit of the common-emitter stage of the VGA.

formance [26], [28], [31]. In VGAs using bipolar transistors, the capacitance between the base and emitter varies depending on the collector current. Figure 3 shows the equivalent circuit of the bipolar transistor and the simulation results of the collector current dependence of the parasitic capacitances, where the transistor size is 0.12 μm/4 μm, and the current range is from 0 to 2000 μA. The parallel capacitance C_π varies from 13.7 to 36.5 fF. This results in the variation in the insertion phase of the VGA, and the insertion phase variation of the VGA results in the degeneration of the phase control performance of the VGPS.

To prevent variation in the insertion phase of the VGA, we propose a phase compensation technique with a varactor C_{var} connected in parallel with the base terminal (Fig. 2). Figure 4 shows the small-signal equivalent circuit of the common-emitter stage of the VGA. The input impedance of the VGA is calculated using this circuit. We assume that the input signals of the VGA are differential ($v_{xp} = -v_{xn}$). The relationship between V_{in} and V_s is expressed as

$$V_{in} = \frac{Z_{diff}(I_p, I_n)}{Z_{diff}(I_p, I_n) + Z_s} V_s. \tag{4}$$

The differential input impedance is given by

$$Z_{diff}(I_p, I_n, V_{var}) \approx \frac{2}{\left(\frac{2}{r_\pi} + j\omega\Big(C_\pi(I_p) + C_\pi(I_n) + 2C_\mu + C_{var}(V_{var})\Big)\right)}, \tag{5}$$

where the capacitances between the base and collector of the differential transistor are assumed to be nearly equal ($C_\mu = C_{\mu p} \approx C_{\mu n}$) because they do not depend on the collector current (Fig. 3). V_{var} is the varactor control voltage. The variation in the input capacitance, that of the capacitance between the base and emitter, and that of the varactor capacitance according to the gain control are defined as ΔC_{in}, ΔC_π, and ΔC_{var}, respectively. The relationships among these capacitances are as follows:

$$\begin{aligned} &C_\pi(I_p) + C_\pi(I_n) = \Delta C_\pi(|I_p - I_n|) + C_{\pi 0}, \\ &C_{var}(V_{var}) = \Delta C_{var}(V_{var}) + C_{var0}, \\ &\Delta C_{in}(|I_p - I_n|, V_{var}) = \Delta C_\pi(|I_p - I_n|) + \Delta C_{var}(V_{var}), \end{aligned} \tag{6}$$

where $C_{\pi 0}$ is the capacitance at the initial bias current $I_{p0} - I_{n0}$, and $\Delta C_\pi(|I_{p0} - I_{n0}|)$ is 0. C_{var0} is the capacitance of the initial control voltage, and $\Delta C_{var}(0)$ is 0 at the initial control voltage. From Eqs. (5) and (6), the differential input impedance can be expressed as follows:

$$Z_{diff}(I_p, I_n, V_{var}) \approx 2\left|\left(\frac{2}{r_\pi} + j\omega\Big(C_{\pi 0} + C_{var0} + 2C_\mu + \Delta C_{in}(|I_p - I_n|, V_{var})\Big)\right)\right|. \tag{7}$$

The source impedance Z_s for input impedance matching is defined as follows:

$$Z_s = 2\left|\left(\frac{2}{r_\pi} - j\omega\Big(C_{\pi 0} + C_{var0} + 2C_\mu\Big)\right)\right|, \tag{8}$$

The insertion gain of the VGA $G(I_p - I_n, V_{var})$ after input matching using Z_s is given by

$$\begin{aligned} G(I_p - I_n, V_{var}) &= G_0 \cdot \frac{\frac{2}{r_\pi} - j\omega(C_{\pi 0} + C_{var0} + 2C_\mu)}{\frac{4}{r_\pi} + j\omega\Delta C_{in}(|I_p - I_n|, V_{var})}, \\ G_0 &= \frac{-2Z(g_{mp} - g_{mn})}{1 + 2j\omega C_u Z}, \end{aligned} \tag{9}$$

The input capacitance ΔC_{in} varies with the collector current, according to the gain. The relationship between the variation of the input capacitance and that of the insertion phase and gain is calculated using Eq. (9). The variations in the insertion gain ΔG, amplitude of insertion gain $|\Delta G|$ and insertion phase $\Delta\varphi$ are expressed as follows:

$$\Delta G = \frac{G(I_p - I_n, V_{var})}{G(I_{p0} - I_{n0}, 0)} = \frac{\frac{4}{r_\pi}}{\frac{4}{r_\pi} + j\omega\Delta C_{in}(|I_p - I_n|, V_{var})} \tag{10a}$$

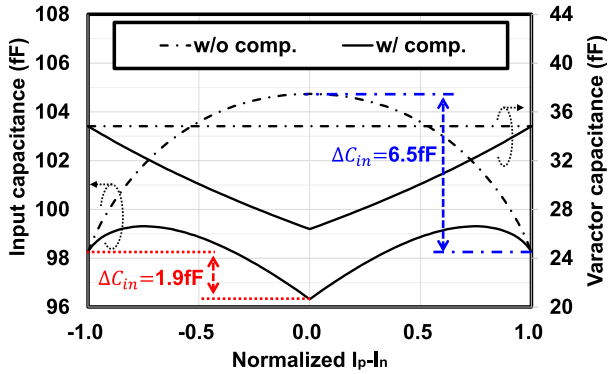


Fig. 5 Simulation results of the collector current dependence of the input capacitance.

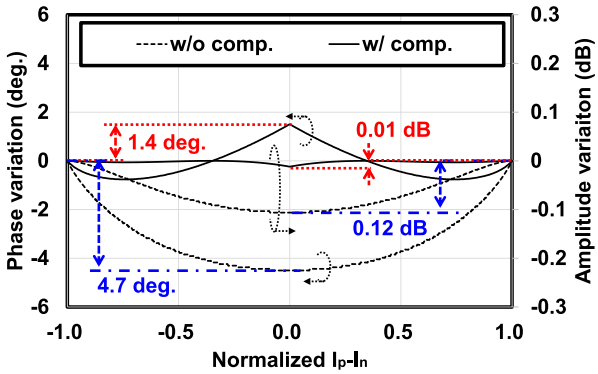


Fig. 6 Calculation results of the collector current dependence of the insertion phase and amplitude variation.

$$|\Delta G| = \frac{\left(\frac{4}{r_\pi}\right)}{\sqrt{\left(\frac{4}{r_\pi}\right)^2 + \left(\omega \Delta C_{in}(|I_p - I_n|, V_{var})\right)^2}}, \tag{10b}$$

$$\Delta\varphi = -\tan^{-1}\frac{\omega \Delta C_{in}(|I_p - I_n|, V_{var}) r_\pi}{4}, \tag{10c}$$

Equation (10b) indicates that the variation of $|\Delta G|$ is determined by the ratio of $\omega\Delta C_{in}$ to $4/r_\pi$. The influence of ΔC_{in} on $|\Delta G|$ can be small under the condition of $(4/r_\pi)^2 \gg (\omega\Delta C_{in}(|I_p - I_n|, V_{var}))^2$. For example, it is assumed that r_π and ΔC_{in} are 540 Ω and 6.5 fF, respectively. At 30 GHz, $(4/r_\pi)^2$, which is 5.5×10^{-5}, is significantly larger than $(\omega\Delta C_{in}(|I_p - I_n|, V_{var}))^2$, which is 1.5×10^{-6}. $|\Delta G|$ is approximately 1.3% (0.12 dB) under this condition. In contrast, Eq. (10c) shows that $\Delta\varphi$ is proportional to the arc tangent of $\omega\Delta C_{in}$ and r_π. For example, if r_π and ΔC_{in} are in the same conditions (r_π = 540 Ω, ΔC_{in} = 6.5 fF), $\Delta\varphi$ is approximately 4.7° at 30 GHz. From the above discussion, $\Delta\varphi$ of the VGA will have a greater influence on the phase and amplitude error of VGPS under the condition of $(4/r_\pi)^2 \gg (\omega\Delta C_{in}(|I_p - I_n|, V_{var}))^2$.

The insertion phase variation $\Delta\varphi$ is zero when the varactor voltage is controlled to maintain the input capacitance constant at any gain state. In this case, varactor voltage satisfies the following equation:

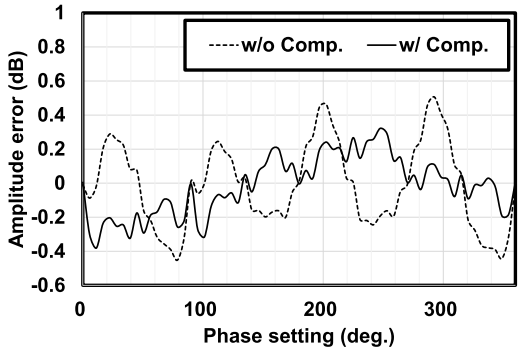
$$V_{var} = \Delta C_{var}^{-1}(-\Delta C_\pi(|I_p - I_n|)), \tag{11}$$

where ΔC_{var}^{-1} is the inverse function of ΔC_{var}.

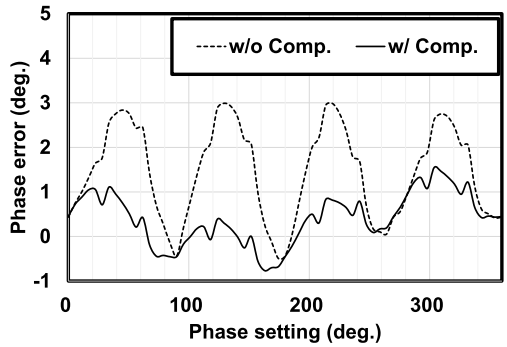
The collector current dependence of the input capacitance was simulated when the varactor voltage was controlled linearly with respect to the difference $I_p - I_n$, so that the change in the input capacitance was small. Figure 5 shows the simulation results of the collector current dependence of the input capacitance with and without the proposed compensation technique, where the varactor anode length and width were 1 and 15 μm, respectively. The varactor capacitance was constant without the compensation technique. In contrast, the varactor capacitance ranged from 27 to 34.5 fF with the compensation technique according to the normalized collector current $I_p - I_n$. The input capacitance was from 98.3 fF to 104.8 fF without the compensation technique. On the other hand, it was from 96.4 fF to 99.3 fF with the compensation technique. The maximum variation in the input capacitance from the initial condition (normalized $I_p - I_n = -1$ or 1, the initial input capacitance = 98.3 fF) was 1.9 fF with the compensation technique and 6.5 fF without the compensation technique. The proposed technique achieved a 4.6 fF improvement in the variation. The collector-current dependence of the insertion phase and amplitude variation calculated using Eq. (10) are shown in Fig. 6. In this calculation, the varactor capacitance control was the same as that shown in Fig. 5. r_π was 540 Ω, which was derived from the circuit simulation.

Figure 6 shows that the maximum variation from the initial condition in the insertion phase with and without the proposed technique was 1.4° and 4.7°, respectively. Also, the maximum variation from the initial condition in the insertion gain with and without the proposed technique was 0.01 dB and 0.12 dB, respectively. The proposed technique achieved 3.3° and 0.11 dB improvement in insertion phase variation $\Delta\varphi$ and amplitude of the gain variation $|\Delta G|$.

In the upper discussion, the varactor was assumed to be the ideal varactor without parasitic resistors as shown in Fig. 4. However, the actual varactor has parasitic resistors and the Q-factor is finite. Therefore, there are some cases to consider the influence of the varactor Q-factor. The r_π was calculated as the combined resistance of the equivalent parallel resistance of the bipolar (= 664 Ω constant) and the varactor (= 2.9 kΩ constant) by the simulation. Since the Q-factor and the equivalent parallel resistor of the varactors vary from 13.0 to 14.8 and from 2.0 kΩ to 2.9 kΩ according to frequency and the control voltage, the r_π varies approximately 7.5% from 501 Ω to 540 Ω with the variations of the varactors. The effect on amplitude and phase variations with the compensation technique in Fig. 5 (ΔC_{in} = 1.9 fF), which is calculated from 7.5 % variation of r_π and Eq. (10), are about 0.001 dB and 0.2° at 30 GHz. Thus, the influence of the varactor Q-factor must be considered depending on the target performance of the amplitude and phase variations, and the precise amplitude and phase variations must be confirmed by the circuits simulation.



(a)



(b)

Fig. 7 Calculation results of (a) the insertion amplitude and (b) phase errors of the VGPS.

2.3 Phase and Amplitude Error of the VGPS by the Phase and Amplitude Variation of VGA

The phase and amplitude errors of the VGPS based on the insertion phase and gain variations of the I/Q VGA according to amplitude control are expressed as follows:

$$\begin{aligned}
\varphi_{err,i} &= \tan^{-1}\left(\frac{Y_i}{X_i}\right) - \varphi_{ideal,i} \\
A_{err,i} &= \sqrt{{X_i}^2 + {Y_i}^2}\Big/A_{ideal,i} \\
Y_i &= (cos\,\varphi_{ideal,i} + \Delta G_{I,i})\, sin\,\Delta\varphi_{I,i} \\
&\quad + (sin\,\varphi_{ideal,i} \\
&\quad + \Delta G_{Q,i})\, cos\,\Delta\varphi_{Q,i} \\
X_i &= (cos\,\varphi_{ideal,i} + \Delta G_{I,i})\, cos\,\Delta\varphi_{I,i} \\
&\quad - (sin\,\varphi_{ideal,i} + \Delta G_{Q,i})\, sin\,\Delta\varphi_{Q,i}
\end{aligned} \tag{12}$$

where $\varphi_{ideal,i}$, $A_{ideal,i}$ denotes the ideal phase shift and amplitude. The phase and amplitude errors of the VGPS were calculated with and without the proposed technique at 30 GHz using Eq. (12), and a comparison of the calculation results of is shown in Fig. 7. In the calculation, the 7-bit ideal value of the gain settings for the IREFP/IREFN in I-VGA and Q-VGA (i.e., $\sin\theta$ for I-VGA and $\cos\theta$ for Q-VGA) were used. Therefore, the 7-bit amplitude quantization error is included in Fig. 7. The calculated maximum amplitude error with and without the proposed technique from Fig. 7 (a) were 0.38 and 0.51 dB, respectively. The maximum phase errors calculated with and without the proposed technique from Fig. 7 (b) were 1.55° and 2.99°, respectively. The proposed technique achieved a 0.13 dB and 1.44° improvement in the amplitude and phase error of VGPS, respectively.

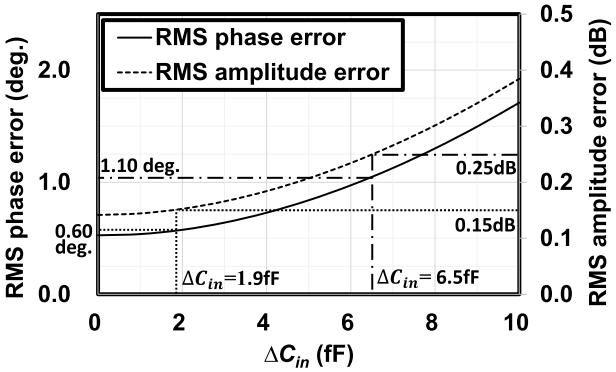


Fig. 8 Calculation results of the RMS amplitude and phase errors of VGPS using ΔC_{in}.

Table 1 Parameters of the VGA and VGPS.

Parameter	Value
Q1–Q4	0.12 μm / 4 μm
Q5–Q8	0.12 μm / 12 μm
I_{total}	2 mA
L	512 pH
C_{var}	27–34 fF (anode length: 1 μm, anode width: 15 μm)

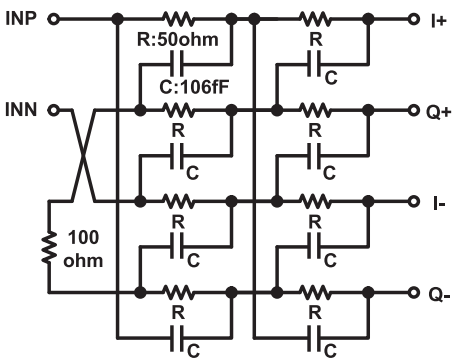


Fig. 9 Circuit configuration of the I/Q generator

The RMS phase shift error φ_{rms} and RMS amplitude error A_{rms} of an m-bit phase shifter owing to I/Q phase imbalance are calculated as follows:

$$\begin{aligned}
\varphi_{rms} &= \sqrt{\frac{\sum_{i=1}^{2^m} \varphi_{err,i}^2}{2^m}} \\
A_{rms} &= \sqrt{\frac{\sum_{i=1}^{2^m} A_{err,i}^2}{2^m}}
\end{aligned} \tag{13}$$

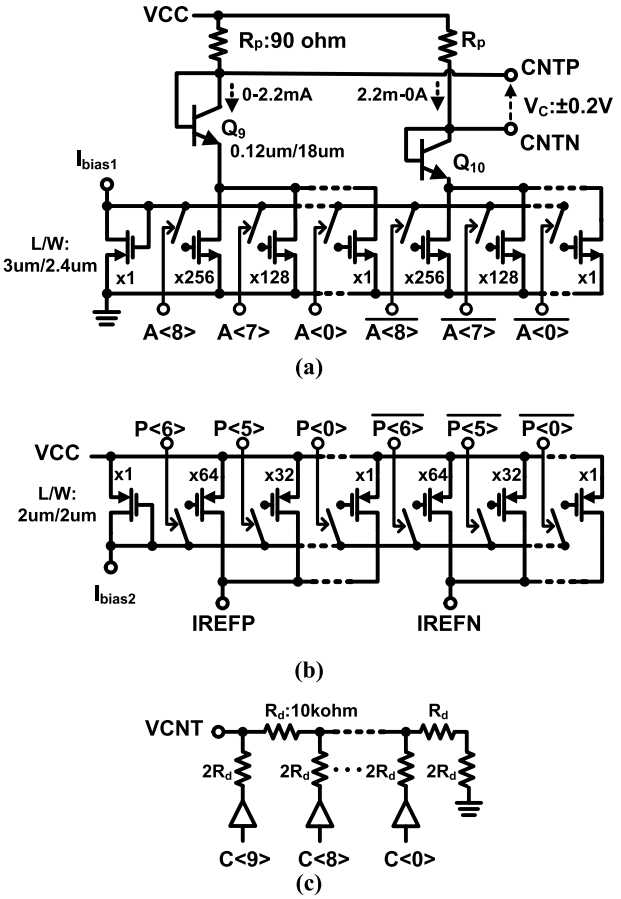


Fig. 10 Circuit configuration of the DACs: (a) 9-bit DAC for amplitude control, (b) 7-bit DAC for phase control, and (c) 10-bit DAC for phase compensation

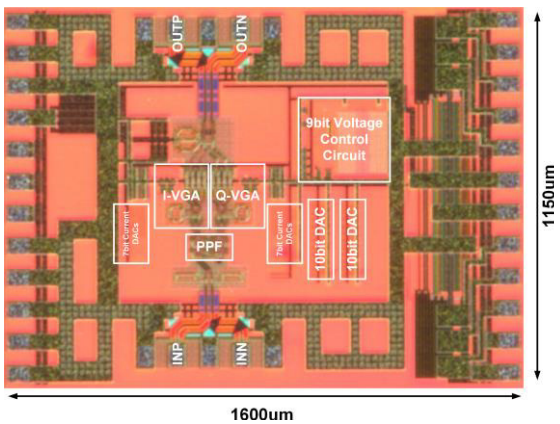


Fig. 11 Photograph of the manufactured IC (size 1600 μm × 1150 μm).

The RMS amplitude and phase errors of the VGPS due to the variation in ΔC_{in} can be calculated using Eqs. (10), (12), and (13). The calculation results of the RMS amplitude and phase errors of VGPS by ΔC_{in} are shown in Fig. 8. ΔC_{in} was 6.5 fF as calculated in Fig. 5 without the proposed technique, and the calculated RMS amplitude and phase error were 0.25 dB and 1.10°, respectively. In contrast, ΔC_{in} was

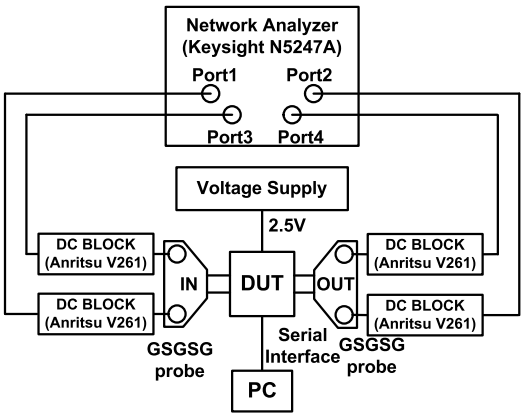


Fig. 12 Measurement system.

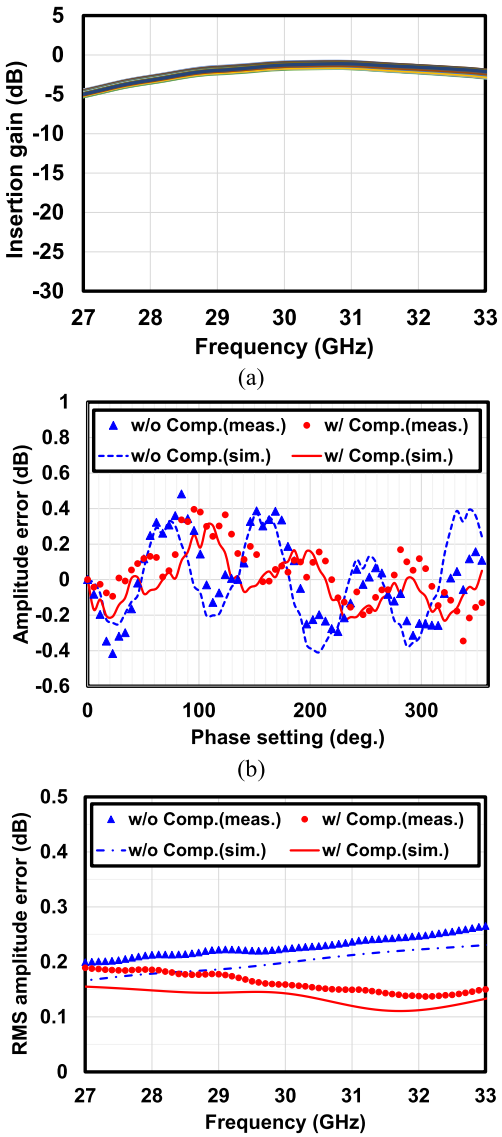


Fig. 13 Measured gain performance of the VGPS when the phase shift was controlled within 360° with 5.625° steps and the maximum gain state: (a) insertion gain, (b) amplitude error comparison with simulation at 30 GHz, (c) RMS amplitude error

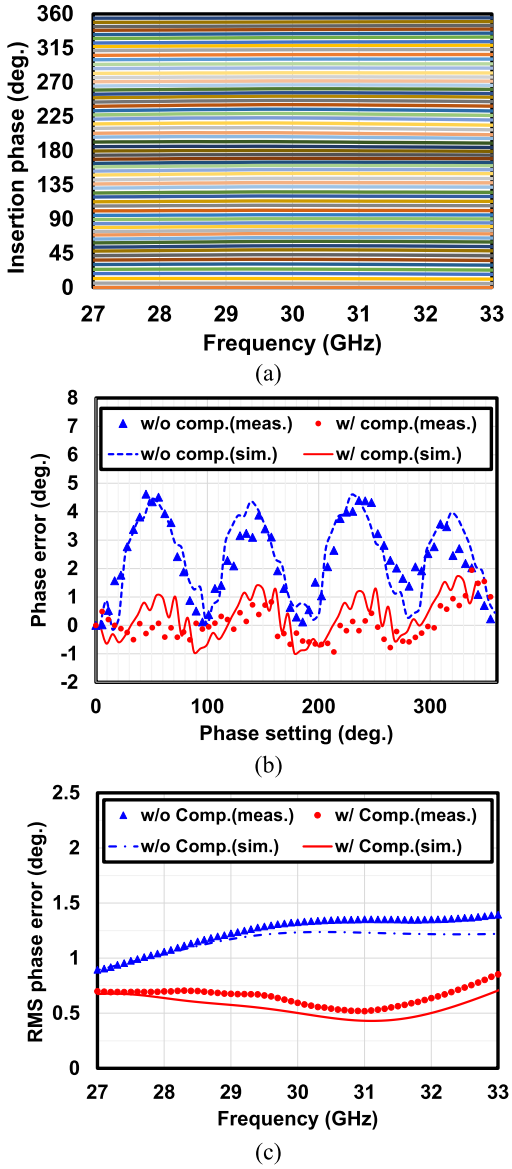


Fig. 14 Measured phase performance of the VGPS when the phase shift was controlled within 360° with 5.625° steps and the maximum amplitude state: (a) insertion phase, (b) phase error comparison with simulation at 30 GHz, (c) RMS phase error.

1.9 fF with the proposed technique, and the calculated RMS amplitude and phase error were 0.15 dB and 0.60°, respectively. The proposed technique achieved a 0.10 dB and 0.50° improvement in the RMS amplitude and phase errors, respectively. The reason why the RMS phase error and amplitude error are not zero at $\Delta C_{in} = 0$ fF is due to the 7-bit amplitude quantization error of I/Q VGAs.

From the upper discussion, the proposed technique can reduce the variation in the insertion phase of the IQ-VGAs by controlling the varactor voltage in the input terminal of the IQ-VGAs linearly with respect to the IQ-VGAs amplitude control value. This is because the input capacitance variation of IQ-VGA can be maintained constant in any phase state. As a result, the proposed technique can achieve

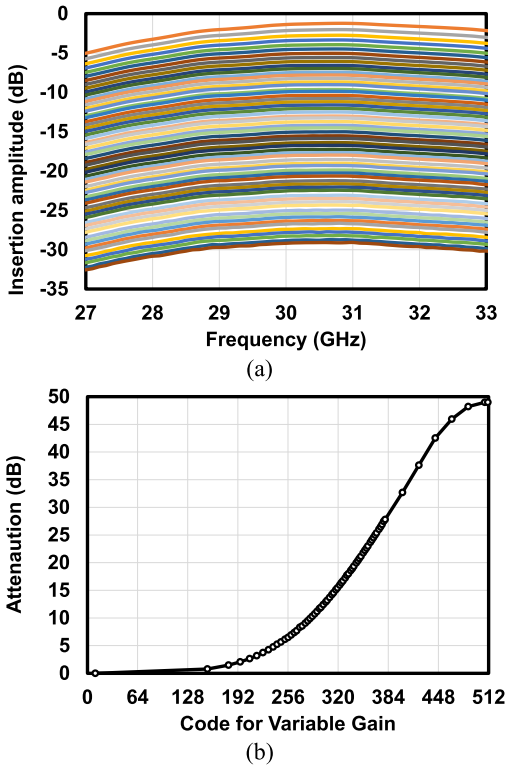


Fig. 15 Measured variable gain performance. (a) Insertion amplitude (b) Attenuation characteristics at 30 GHz.

low phase and amplitude errors for the VGPS.

3. Implementation

The proposed VGPS shown in Fig. 1 is implemented. Table 1 shows the device parameter of the VGA shown in Fig. 2 and the VGPS. Figure 9 shows the circuit configuration of the I/Q generator. The I/Q generator is a two-stage RC polyphase filter. The resistor R is 50 Ω and the capacitance C is 106 fF, which is determined for the single-pole angular frequency of 30 GHz. Figure 10 shows the configuration of the DACs. Figure 10 (a) shows the circuit configuration of the 9-bit DAC for amplitude control. The DAC consists of binary weighted NMOS current mirrors, NPN transistors Q_9 and Q_{10}, and resistors R_p. V_c, which is the difference between *CNT_P* and *CNT_N*, is approximately ±0.2 V. The number of bits of the amplitude control DAC is set to 9 ($> 0.4V/\Delta V_c$:1.5mV = 266) from Eq. (3) so that 0.5dB steps amplitude resolution can be obtained within the variable range V_c. The minimum device L/W of NMOS corresponds to 3 μm/2.4 μm. Figure 10 (b) shows the circuit configuration of the 7-bit DACs for phase control. The DACs are composed of binary weighted PMOS current mirrors. The minimum device L/W of PMOS corresponds to 2 μm/2 μm. This DAC determines the VGA amplitude ($I_p - I_n$) resolution and RMS phase and amplitude error of VGPS due to quantization error. To achieve both 0.37° RMS phase error and 0.03° RMS amplitude error due to the quantization error in the 6-bit VGPS, the number of bits of this

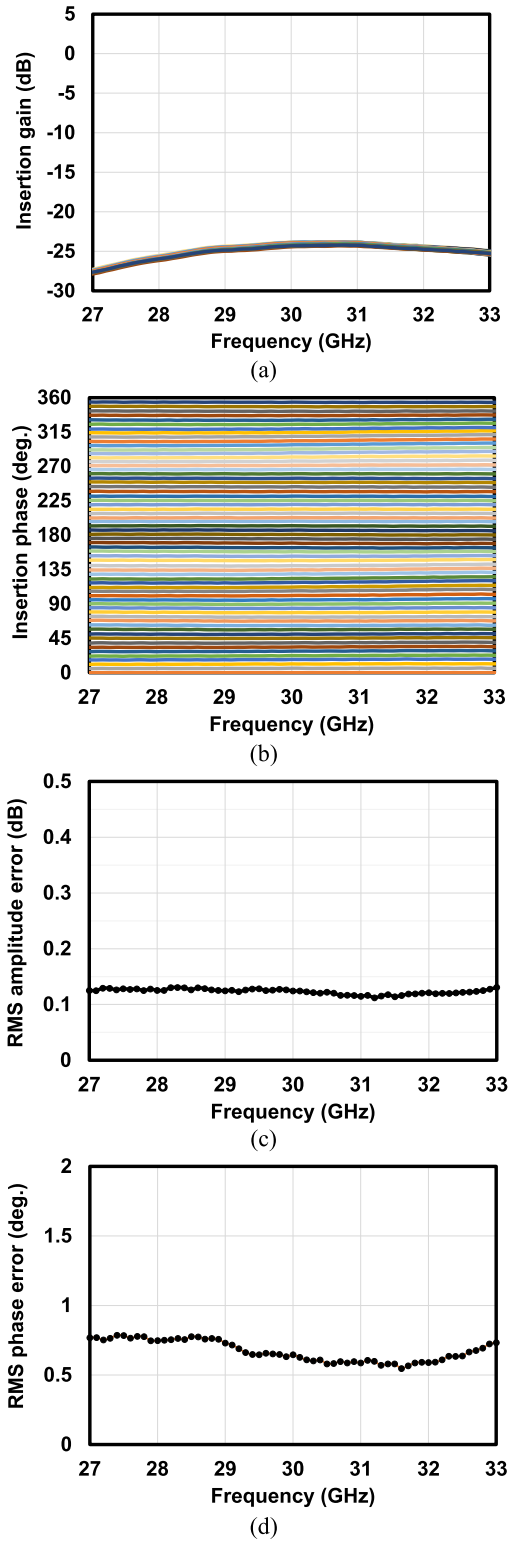


Fig. 16 Measured gain and phase performance of the VGPS when the phase shift is controlled within 360° with 5.625°-steps and a 23 dB attenuation state. (a) insertion gain, (b) RMS amplitude error, (c) insertion phase, (d) RMS phase error.

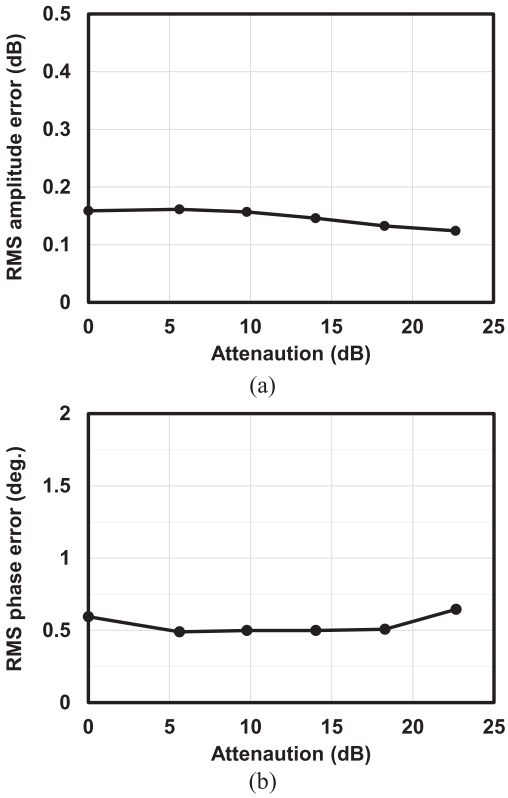


Fig. 17 Phase shift performance with respect to the attenuation. (a) RMS amplitude error (b) RMS phase error.

DAC should be at least 6 bits. 1-bit for polarity reversal is added and the total DAC bit is set to 7. Figure 10 (c) shows the circuit configuration of the 10-bit DACs for phase compensation. A phase compensation DAC requires a resolution similar to that of a phase control DAC in order to avoid the influence of quantization errors set by capacitances. In the varactor shown in Sect. 2.2, 27–34.5 fF corresponds to a control voltage range of 0–0.5V. Therefore, the required voltage resolution is 3.9 mV (= $0.5\text{V}/2^{7bit}$). Since it is a power supply voltage (2.5V) division type DAC, the resolution is set to 10 ($> 2.5V/3.9mV = 640$). The DACs are composed of R-2R ladder resistors for rail-to-rail outputs. R is 10 kΩ for this design.

4. Measurement Result

Figure 11 shows a die photograph of the VGPS fabricated using the 130 nm SiGe BiCMOS process. The chip area was 1150 μm × 1600 μm. The active area was 0.31 mm^2. Figure 12 shows the measurement system. A probe station with GSGSG probes and a four-port network analyzer (Keysight N5247A) were used to characterize the performance of the chip. A PC provided the input code for the DAC via the serial interface in the chip. In the measurements, the ideal value of the gain settings for the DACs input code-VGA and Q-VGA (i.e., $\sin\theta$ for I-VGA and $\cos\theta$ for Q-VGA) were used for the 7-bit DACs for phase control. In addition, the varactor voltage was controlled linearly with respect to

Table 2 Comparison of vector-sum phase shifters of this and other studies

	Process	Frequency (GHz)	Configuration	Gain ctrl		Phase ctrl				Gain (dB)	Power consumption (mW)	Chip area (mm2)
				Range (dB)	Resolution (dB)	Resolution (dB)	RMS phase error (deg.)	RMS gain error (dB)	Gain variation (dB)			
This work	130nm SiGeBiCMOS	28-32	VGPS	23	0.5	6bit	0.75	0.19	0.8	-3.2	27.5	0.31
[14]	65nm CMOS	26-30	VGPS	16	0.5	6bit	1.5	0.25	-	14.8*	44*	0.09**
[15]	65nm CMOS	21-30	VGA&PS	24	0.75	0.8 degrees	0.88	0.16	0.5	12.2	12	0.34
[16]	130nm SiGeBiCMOS	26-28	PS	-	-	8bit/5bit	0.2/4	0.2	-	-0.5	23	0.45
[17]	90nm SiGeBiCMOS	20.5-26.5	PS	-	-	6bit	2	-	1.5	-1	10	0.12
[18]	180nm CMOS	18.1-19.9	PS	-	-	4bit	2.5	0.7	4.52	-2.75	10	0.67
[20]	65nm CMOS	32-40	PS	-	-	7bit	1.6	0.38	1.2	-17.5	0	0.14
[21]	130nm SiGeBiCMOS	26.5-29.5	PS	-	-	4bit	3.5/4.2	0.7/1.0	-	-4.4/2.3	27.5/42.5	0.71/1.15
[22]	65nm CMOS	19-23	PS	-	-	6bit	2.3	0.38	1.73	-14	0	0.64
[23]	65nm CMOS	52-64	VGPS	14.8	-	6bit	3.3	0.5	-	-5.8	18	0.40
[28]	65nm CMOS	30-32.5	VGPS	17.3	-	5bit	2.6	0.4	-	-2.8	18	0.21
[29]	65nm CMOS	20.8-25	VGPS	17.8	0.57	7bit	1.17	0.13	-	-3.5	6.6	0.13
[30]	65nm CMOS	79	VGPS	21.6	3	5bit	6.7	1.89	-	-11.4	24.7	0.14
[34]	250nm SiGeBiCMOS	8-12	PS with on/off chip calibration	-	-	7bit	2	1.6	-	-8.6	110	2.60
[35]	65nm CMOS	14.5-15	PS with on/off chip calibration	-	-	6bit	1.4	0.7	2.2	-9.7	67.1	0.72**
[36]	28nm CMOS	22-44	PS with on chip calibration	-	-	7bit	0.92	0.36	2.73	-3.1	35	0.74

*including additional amplifiers, ** estimation from chip photographs

the difference $I_p - I_n$, which was the same as that in Fig. 5. The current from a 2.5 V voltage supply was 11.0 mA. The power consumption was 27.5 mW.

The measured gain and phase performance of the VGPS when the phase shift was controlled within 360° with 5.625° steps and the maximum gain state (A<8:0>= 0) are shown in Figs. 13 and 14. Figures 13 (a) and 14 (a) show the insertion gain and phase, respectively. The measured average gain at 30 GHz was −1.3 dB. Figures 13 (b) and 14 (b) show a comparison between the simulated and measured results of the amplitude and phase error at 30 GHz. From Fig. 13 (b), the measured maximum amplitude error with and without the proposed technique were 0.40 and 0.48 dB, respectively. The simulated maximum amplitude error with and without the proposed technique were 0.31 and 0.40 dB, respectively. From Fig. 14 (b), the measured maximum phase errors with and without the proposed technique were 1.95° and 4.62°, respectively. The simulated maximum phase errors with and without the proposed technique were 1.73° and 4.57°, respectively. Figures 13 (b) and 14 (b) show that the simulated and measured amplitude and phase errors were almost consistent with each other. In addition, these results were in almost good agreement with the calculated maximum amplitude and phase error (0.38 dB/1.55° with the proposed technique and 0.51 dB/2.99° without the proposed technique) given in Sect. 2. Figures 13 (c) and 14 (c) show the RMS amplitude and phase error with and without the proposed technique. The proposed technique achieved measured RMS amplitude and phase errors of 0.16 dB and 0.59° at 30 GHz. In contrast, these errors were 0.22 dB and 1.32° without the proposed technique. The proposed technique achieved 0.06 dB and 0.73° improvement in the RMS amplitude and phase error, respectively. These results were in good consistent with the calculated results (0.15 dB and 0.60° with the proposed technique, and 0.25 dB and 1.10° without the proposed technique) given in Sect. 2. The measured maximum RMS amplitude and phase errors at 28–32 GHz were 0.19 dB and 0.71°, respectively, with the proposed technique.

The measured variable gain performance is shown in Fig. 15. Figure 15 (a) shows the insertion amplitude. Figure 15 (b) shows the attenuation characteristics at 30 GHz with respect to the variable gain code A<8:0> (Fig. 10 (a)). The gain control range was greater than 40 dB. The gain resolution was less than 0.5 dB when the attenuation amount was less than 27 dB. The measured gain and phase performance of the VGPS with phase compensation when the phase shift was controlled within 360° with 5.625° steps and 23 dB attenuation state (A<8:0>= 365) are shown in Fig. 16. Figure 16 (a) and 16 (b) show the insertion gain

and phase, respectively. The measured gain at 30 GHz was −24.3 dB. Figure 16 (c) and 16 (d) show the RMS amplitude and phase error, respectively. The measured RMS amplitude and phase errors at 30 GHz were 0.12 dB and 0.65°, respectively. The phase-shift performance with respect to the attenuation at 30GHz is shown in Fig. 17. Figure 17 (a) and 17 (b) show that the measured RMS amplitude and phase errors achieved less than 0.16 dB and 0.65° in more than 23 dB gain control range. The VGPS achieved measured RMS amplitude and phase errors of less than 0.19 dB and 0.75°, respectively, in a gain control range of 23 dB with a frequency range of 28 to 32 GHz. Table 2 shows a performance comparison of the VSPSs of this and other studies. This study achieved the lowest RMS phase error in the VGPS. A small chip size and low power consumption were also demonstrated relative to the other VSPS with calibration techniques.

5. Conclusion

This study demonstrated a phase compensation technique using varactors for a VGPS based on a common emitter-based VGA. The phase control performance degenerates because the input capacitance of I/Q VGAs varies with the collector current. The proposed phase-compensation technique reduces the variation in the insertion phase of I/Q VGAs by adjusting the voltage of the varactor and maintaining the input capacitance constant in any amplitude state. Consequently, the proposed VGPS can provide low phase and amplitude errors under phase control. The Ka-band VGPS with the proposed phase compensation technique, which was fabricated in a 130-nm SiGe BiCMOS process, demonstrated 0.06 dB and 0.73° improvement of the RMS amplitude and phase error compared with the case without the compensation technique. The VGPS achieved measured RMS amplitude and phase errors of less than 0.19 dB and 0.75°, respectively, in a gain control range of 23 dB with a frequency range of 28 to 32 GHz.

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