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PAPER

# Radiation-Hardened Flip-Flops in a 65 nm Bulk Process for Terrestrial Applications Coping With Radiation Hardness and Performance Overheads

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**SUMMARY**
Integrated circuits used in automotive or aerospace applications must have high soft error tolerance. Redundant Flip Flops (FFs) are effective to improve the soft error tolerance. However, these countermeasures have large performance overheads and can be excessive for terrestrial applications. This paper proposes two types of radiation-hardened FFs named Primary Latch Transmission gate FF (PLTGFF) and Feed-Back Gate Tri-state Inverter FF (FBTIFF) for terrestrial use. By increasing the critical charge ($Q_{\mathrm{crit}}$) at weak nodes, soft error tolerance of them were improved with low performance overheads. PLTGFF has the 5% area, 4% delay, and 10% power overheads, while FBTIFF has the 42% area, 10% delay, and 22% power overheads. They were fabricated in a 65 nm bulk process. By $\alpha$-particle and spallation neutron irradiation tests, the soft error rates are reduced by 25% for PLTGFF and 50% for FBTIFF compared to a standard FF. In the terrestrial environment, the proposed FFs have better trade-offs between reliability and performance than those of multiplexed FFs such as the dual-interlocked storage cell (DICE) with larger overheads than the proposed FFs.

***key words:*** *Soft error, Single Event Upset (SEU), critical charge, $\alpha$-particle, spallation neutron, Flip-Flop, terrestrial environment*

## 1. Introduction

Soft errors are one of the temporal failures that upset stored values in storage elements such as flip-flops (FFs) or SRAMs caused by a radiation strike. In the terrestrial environment, $\alpha$-particles and neutrons cause an upset of storage elements [1]. When a radiation particle hits on a chip, its ionizing effect generates electron-hole pairs in p-well and n-well. Generated electrons in the p-well are collected into the drain regions of NMOS transistors by funneling, drift, and diffusion [2]. The drain voltage is flipped by collected electrons. As the CMOS technology is down scaling, the amount of charge required to upset stored values in storage elements is gradually reduced due to the low supply voltage and small capacitance of transistors. So soft errors become more serious with technology down scaling [3]–[6]. In the terrestrial environment, high reliability is required for supercomputers, medical instruments, automotive driving technologies, and so on. Therefore, countermeasures against soft errors are necessary [7] [8]. To improve the soft error tolerance of FFs, several redundant circuits such as Triple Modular Redundancy FF (TMRFF) [9], Built-In Soft Error Resilience FF (BISERFF) [10], Bistable Cross-coupled Dual Modular Redundancy FF (BCDMRFF) [11] and the Dual Interlocked Storage Cell FF (DICEFF) [12] [13] have been proposed. However, the number of transistors of these FFs is significantly larger than that of a standard FF (STDFF), and the performance overheads are large. Those redundant FFs may not be optimal for some applications. For example, due to higher radiation flux in outer space than in the terrestrial environment, storage-cell multiplication is an effective countermeasure in outer space. In the terrestrial environment, however, the possibility of soft errors is much lower than space. Thus multiplication is sometimes an excessive countermeasure. Therefore, it is necessary to take a countermeasure to bring a trade-off between soft error tolerance and circuit performance. In recent years, device-level and circuit-level soft error countermeasures have been considered as non-multiplexing countermeasures [14]–[17]. However, these countermeasures cannot be applied to conventional bulk process technologies, and it is necessary to develop countermeasures without multiplexing.

In this paper, we proposed two types of radiation-hardened FFs with low performance overheads by increasing the critical charge ($Q_{\mathrm{crit}}$) [18]. We compared the soft error tolerance and the circuit performance of the proposed FFs with STDFF and DICEFF. Area, delay and power of these proposed FFs were larger than those of STDFF. However, these overheads were much smaller than DICEFF. Although the proposed FFs are weaker to soft errors than multiplexed FFs, they still have higher soft error tolerance than the STDFF to $\alpha$-particles and neutrons. These results revealed that the proposed FFs have better trade-offs between reliability and performance compared to STDFF and the redundant FFs for the terrestrial environment.

This paper is organized as follows. Section 2 describes soft error mechanism in a bulk process. Section 3 describes soft error suppression mechanisms and circuit performance of the proposed FFs. Section 4 describes the soft error tolerance of the proposed FFs evaluated by device simulations. Section 5 evaluates the soft error tolerance of the proposed FFs by $\alpha$-particle and neutron irradiation tests. Section 6 concludes this paper.

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## 2. Principle of Soft Error in a Bulk Process

In the terrestrial environment, soft errors are caused by $\alpha$ particles emitted from package material and neutron generated in the atmosphere by cosmic ray. When an $\alpha$ particle penetrate into a silicon device, electron-hole pairs are generated by its ionizing effect along the particle track as show in Fig. 1. In contrast, neutrons do not directly produce electron-holes pair. However, when a neutron collides with a Si atom in the substrate and cause a nuclear reaction, charged secondary particles are generated. Then the secondary particles generate electron-hole pairs. The generated minority carriers, electrons in the p-well, are collected in the drain region of the NMOS transistor by funneling, drifting, and diffusion. The drain output can be flipped by collected electrons transiently. Its radiation effect is termed as a single event effect (SEE). When radiation hits an inverter that constitutes a storage element such as a latch, charges are collected in the diffusion region and a single event transient (SET) pulse is generated at the output of the inverter (node B) as shown in Fig. 2. If a SET pulse is injected to the next gate and the output value (node A) is flipped before the output value of the inverter (node B) returns to the correct value, the stored value of the storage element is flipped. This inversion of the stored value of a storage element is called a soft error. The soft error rate of silicon devices increases with process scaling because process scaling reduces the gate capacitance of the transistor, making the output more easily to flip.

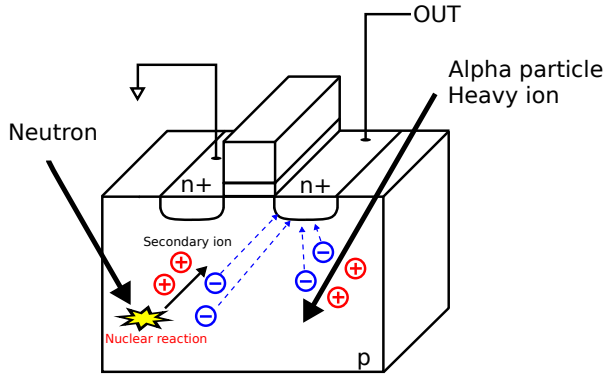
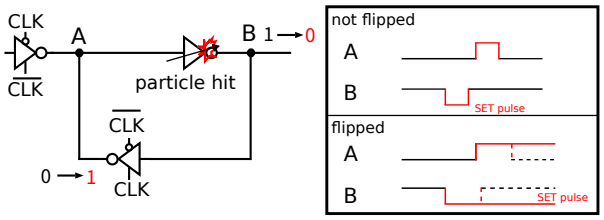



Fig. 1: Single event effect on a silicon devices.




(a)Schematic (b)Waveforms

Fig. 2: Soft error mechanism in a latch.

## 3. Proposed Radiation Hardened FFs Design

### 3.1 Conventional FF

Fig. 3 shows STDFF without any radiation hardness. We focus on critical charge ($Q_{\mathrm{crit}}$) calculated by circuit simulations. $Q_{\mathrm{crit}}$ represents the minimum amount of charge at which the stored value of a latch is flipped. Fig. 4 shows the schematic to obtain $Q_{\mathrm{crit}}$ of the NMOS and PMOS transistors. By connecting the current sources as shown in the Fig. 4, charge collection into the diffusion region can be simulated as shown in Fig. 5. Soft errors occur due to electrons in NMOS and holes in PMOS [19]. Table 1 shows the relationship between the circuit nodes and the states of DATA / Q and CLK. Fig. 6 shows the locations of soft errors in STDFF for each condition.

The current source used for the simulation is the single exponential model in Eq. (1) [20]. $T$ in Eq. (1) refers to the time constant determined by a process node. $T$ is set to 20 ps, corresponding to a 65 nm process [21].

$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right) \tag{1}$$

Table 2 shows $Q_{\mathrm{crit}}$ of NMOS and PMOS transistors of the evaluated FFs. $Q_{\mathrm{crit}}$ of PMOS transistors is larger than NMOS transistors at each node. Soft errors are more likely to occur on NMOS transistors than on PMOS transistors because the mobility of electrons is larger than that of holes [21]. In [22], it has been reported that increased $Q_{\mathrm{crit}}$ improved soft-error tolerance in a 130 nm bulk process. Therefore, we considered countermeasures to increase the $Q_{\mathrm{crit}}$ on NMOS transistors. In STDFF, the node ① and ③ are weaker to soft errors than the other nodes because the output current of the clocked inverter is low. The proposed FFs increase $Q_{\mathrm{crit}}$ at the vulnerable nodes to improve soft-error tolerance.

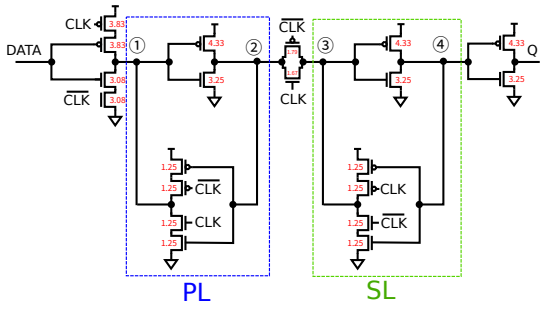
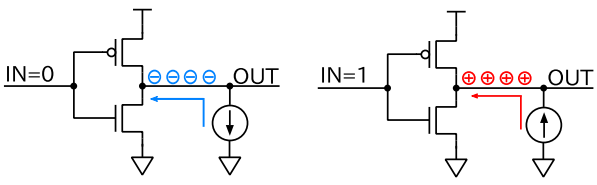
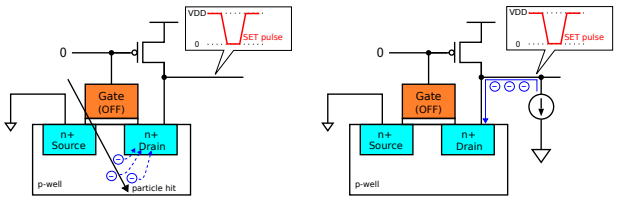



Fig. 3: Standard FF (STDFF)



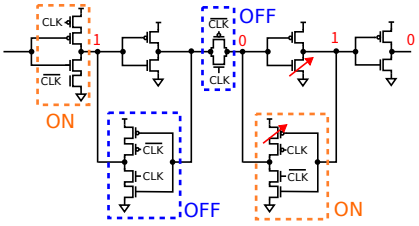

(a) NMOS (b) PMOS

Fig. 4: Schematic to obtain $Q_{\mathrm{crit}}$ of each transistors.

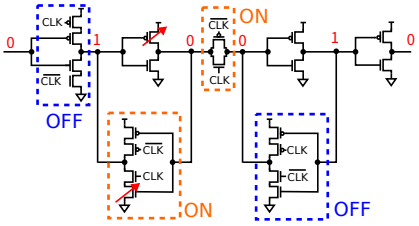



(a) Radiation hits (b) Circuit simulation

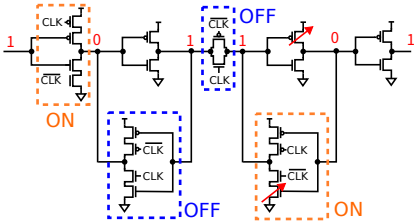
Fig. 5: Charge collection is emulated by a current source in circuit simulation.



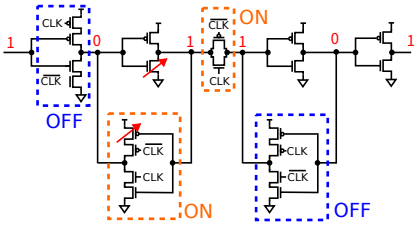

(a) (DATA / Q, CLK) = (0, 0)




(b) (DATA / Q, CLK) = (0, 1)




(c) (DATA / Q, CLK) = (1, 0)




(d) (DATA / Q, CLK) = (1, 1)

Fig. 6: Locations to cause soft errors in STDFF for each condition

### 3.2 PLTGFF

Fig. 7 shows one of the proposed FFs named Primary Latch

Table 1: Relationship between the measurement nodes and the input values.

(a)NMOS transistor

| (DATA / Q, CLK) | STDFF | PLTGFF | FBTIFF |
|---|---|---|---|
| (0, 1) | 1 | 1, 2 | 1 |
| (1, 1) | 2 | 1’ | 2 |
| (0, 0) | 4 | 3 | 3 |
| (1, 0) | 3 | 4 | 4 |

(b)PMOS transistor

| (DATA / Q, CLK) | STDFF | PLTGFF | FBTIFF |
|---|---|---|---|
| (0, 1) | 2 | 1’ | 2 |
| (1, 1) | 1 | 1,2 | 1 |
| (0, 0) | 3 | 4 | 4 |
| (1, 0) | 4 | 3 | 3 |

Table 2: $Q_{\mathrm{crit}}$ of all internal nodes in the standard and proposed FFs.

(a) NMOS transistor

| FF | $Q_{\mathrm{crit}}$ [fC] | | | | |
|---|---|---|---|---|---|
| | 1 | 1’ | 2 | 3 | 4 |
| STDFF | 3.7 | - | 11 | 3.0 | 11 |
| PLTGFF | 5.7(+2.0) | 8.9 | 14(+3.0) | 4.6(+1.6) | 8.7(−2.3) |
| FBTIFF | 8.9(+5.2) | - | 9.4(−1.8) | 20(+17) | 17(+6.0) |

(b) PMOS transistor

| FF | $Q_{\mathrm{crit}}$ [fC] | | | | |
|---|---|---|---|---|---|
| | 1 | 1’ | 2 | 3 | 4 |
| STDFF | 4.5 | - | 13 | 3.9 | 12 |
| PLTGFF | 5.8(+1.3) | 11 | 16(+3.0) | 4.5(+0.6) | 11(−1.0) |
| FBTIFF | 5.8(+1.3) | - | 11(+0) | 7.4(+3.5) | 7.6(−4.4) |

Transmission gate FF (PLTGFF). In PLTGFF, the circuit topology is revised to increase $Q_{\mathrm{crit}}$. The number of the passing logic gates from node ② to Q is reduced to two and then the increment of CLK-Q delay is suppressed. The connection of the last gate inverter is moved from node ④ to node ③, so the parasitic capacitance and $Q_{\mathrm{crit}}$ at node ③ is increased. In PL, the clocked inverter is replaced with the transmission gate and the inverter in red is added. These changes result in exactly the same circuit operation as STDFF without increasing the number of transistors and suppress circuit performance overheads. The gate width of the PMOS transistors in blue is doubled, which increases the number of holes that capture the electrons collected in the diffusion region [22].

### 3.3 FBTIFF

Fig. 8 shows the other proposed FF named Feed-Back Tristate Inverter FF (FBTIFF). FBTIFF is also implemented to increase $Q_{\mathrm{crit}}$ as in PLTGFF. The CLK-Q delay of FBTIFF is suppressed by revising the circuit topology as the similar manner as PLTGFF. The SET pulse generated at node ③ can be suppressed by adding the PMOS pass transistor (P1) [23]. However, it significantly increases static power because of the drain node of the normally-on PMOS pass-transistor.

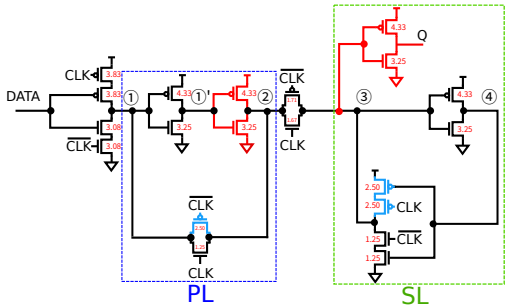



Fig. 7: Primary Latch Transmission Gate FF (PLTGFF)

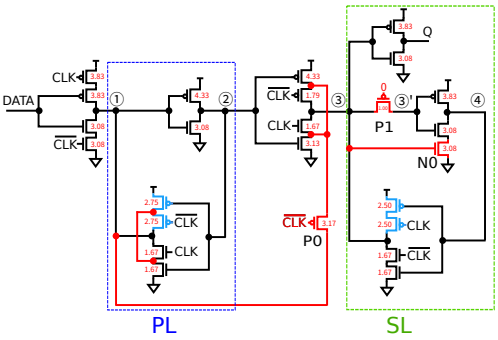
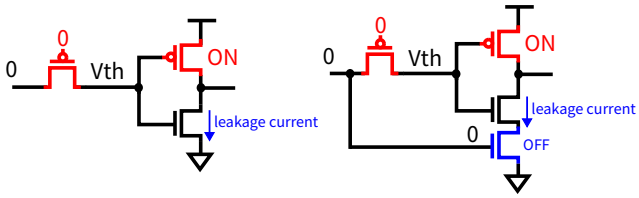



Fig. 8: Feed-Back Tri-state Inverter FF (FBTIFF)




(a)without N0 (b)with N0

Fig. 9: The suppression mechanism of static power in FBTIFF.

Fig. 9 shows the suppression mechanism of static power. In the PMOS pass transistor, when the drain voltage is 0, a voltage drop of Vth occurs, and then the source voltage becomes Vth as shown in Fig. 9 (a). Hence, when node ③ is 0, leakage current flows in the next-stage NMOS, and then the static power increases. Therefore, the cascaded NMOS transistor (N0) is added to the SL inverter as shown in Fig. 9 (b). When node ③ goes to 0, N0 turns off, so the leakage current does not flow and the static power is reduced. Table 3 shows static power with or without N0. These results show that static power can be reduced by more than 99% due to the cascaded NMOS transistor. Both of the clocked inverters in PL and placed between PL and SL are split into the inverter and the transmission gate. The clock signal input transistors, which are connected in series in the initial structure, are connected in parallel in revised structure by the additional wiring. The parallel connection lowers the overall resistance of these logic gates. Therefore, the amount of current flowing to the output increases and $Q_{\mathrm{crit}}$ also increases [22]. The pass transistor (P0) is added

Table 3: Difference in static power with or without N0 (Normalized to STDFF).

| FF | Static power |
|---|---|
| STDFF | 1.00 |
| FBTIFF | 1.55 |
| FBTIFF (without N0) | 212 |

between node ① and the tri-state inverter between PL and SL. Connecting the tri-state inverter to node ① increases the amount of current flowing into node ①. As a result, $Q_{\mathrm{crit}}$ at node ① also increases. If an error occurs in the tri-state inverter connecting PL and SL, a SET pulse is injected to node ① through the additional wiring, and the stored value of PL is flipped. By adding P0, the SET pulses generated by the tri-state inverter between SL and PL can be suppressed as in the case with P1. The input of P0 is set to $\overline{\mathrm{CLK}}$ so as to disconnect node ① with the intermediate nodes of the tristate inverter connecting PL and SL when CLK = 0. Therefore, when the state of DATA changes, node ① can be easily flipped by an input tri-state inverter, thus reducing the increase in D-Q delay. Node ① is fully pull-downed by the clocked inverter in PL even though P0 was added. Therefore, the leak current is negligible in the inverter. The gate width of the PMOS transistors are also doubled as PLTGFF. These revisions increase the amount of current flowing into node ① and $Q_{\mathrm{crit}}$.

As shown in Table 2 (a), $Q_{\mathrm{crit}}$ of NMOS transistors increases at most nodes in PLTGFF. However, $Q_{\mathrm{crit}}$ at node ④ decreases because the gate capacitance of the last-stage inverter is removed. In FBTIFF, $Q_{\mathrm{crit}}$ at node ④ increases despite of removing the last-gate inverter. If radiation strikes the inverter of the latch, a SET pulse is generated at node ④. In this case, the state of the input of the inverter (STDFF : node ③, FBTIFF : node ③') must be inverted before the SET pulse of node ④ returns to its correct value so as to completely flip the stored value in the latch. Therefore, the shorter the delay time from node ④ to the input of the inverter, the more likely a stored value of latch will be flipped. The delay time from node ④ to the input of the inverter is longer for FBTIFF than for STDFF due to the additional P1. Therefore, $Q_{\mathrm{crit}}$ also increases because the width of the SET pulse required to flip the stored value increases. However, $Q_{\mathrm{crit}}$ at node ② decreases by the increased drive strength of the clocked inverter. Adding wire to the clocked inverter reduces the overall resistance of the gate. Thereby, the delay time from node ② to node ① is reduced. Therefore, the width of the SET pulse required to flip the stored value can be reduced, and $Q_{\mathrm{crit}}$ at node ② decreases. At PMOS transistors, $Q_{\mathrm{crit}}$ at each node increase while decreasing at node ④ in FBTIFF. Since the NMOS transistor (N0) is stacked, the amount of current flowing to node ④ and $Q_{\mathrm{crit}}$ becomes small. However, because of the much increase in $Q_{\mathrm{crit}}$ of the NMOS transistors, the soft-error tolerance at node ④ is expected to be improved.

Table 4: Simulation results of area, D-Q delay, CLK-Q delay, setup time, hold time and power of the conventional and proposed FFs at $V_{DD}$ = 1.2 V. (Normalized to STDFF). The number of transistors does not include clock buffers.

| FF | # of Tr. | Area | D-Q delay | CLK-Q delay | Setup time | Hold time | Power |
|---|---|---|---|---|---|---|---|
| STDFF | 20 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| PLTGFF (proposed) | 20 | 1.05 | 1.04 | 0.94 | 3.18 | 0.94 | 1.10 |
| FBTIFF (proposed) | 25 | 1.42 | 1.10 | 0.98 | 3.80 | 0.96 | 1.22 |
| DICEFF | 42 | 2.95 | 2.28 | 1.92 | 8.69 | 0.67 | 2.86 |

Table 5: Cross Section of the node ① and ③.

| | Cross Section [$cm^2$/ion] | |
|---|---|---|
| | node ① | node ③ |
| STDFF | $1.90 \times 10^{-9}$ | $2.02 \times 10^{-9}$ |
| PLTGFF (proposed) | $1.75 \times 10^{-9}$ | $1.20 \times 10^{-9}$ |
| FBTIFF (proposed) | $0.976 \times 10^{-9}$ | 0 |

### 3.4 Circuit performance

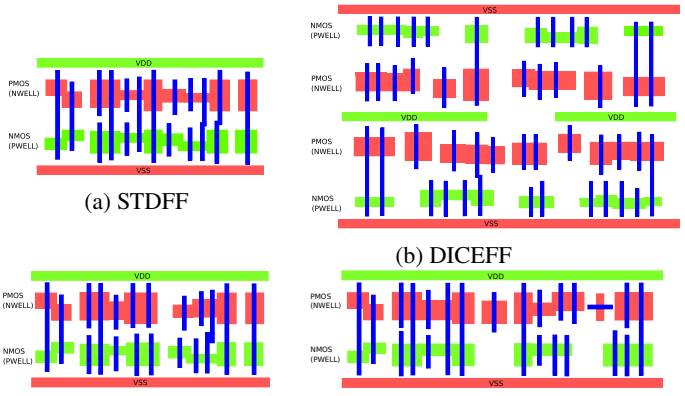
Fig. 10 shows the simplified layout patterns of the fabricated FFs in a 65 nm bulk process with 9 wire pitches. In all layouts, well taps are placed under the VDD and VSS straps. We calculated area, delay time and power consumption of those FFs using circuit simulations at the standard voltage ($V_{dd}$) of 1.2 V. These performance of STDFF, proposed FFs, and DICEFF are shown in Table 4. Power is evaluated with the activation rate of 10% and is averaged between D = 0 and 1. The CLK frequency is 1 GHz. It is calculated as the product of the standard voltage, 1.2 V, and the average value of the current estimated by circuit-level simulations. These values are normalized to STDFF. PLTGFF has the area, D-Q delay, and power overheads by 5%, 4%, and 10% respectively. FBTIFF has the area, D-Q delay, and power overheads by 42%, 10%, and 22% respectively. According to Table 4, the setup times of the proposed FFs are longer than STDFF. Fig. 11 shows the signal path from node ① to the pass transistor between PL and SL. The number of logic gates from node ① to the pass transistor is one for STDFF and two for the proposed circuits. Therefore, the delay time is longer and the setup time of the proposed circuits increased. On the other hand, CLK-Q delay of the proposed FFs is shorter than STDFF because of the circuit topology optimizations discussed in Section 3.2. Therefore, the proposed FFs are able to suppress D-Q delay. The area of FBTIFF increases by 42% compared to STDFF due to the additional PMOS pass transistors. The proposed FFs have a smaller number of transistors than conventional radiation hardened FFs such as DICEFF and much lower performance overheads.

## 4. Soft Error Tolerance Evaluated by Device Simulation

In this section, soft error rates at vulnerable nodes were estimated by TCAD simulations. 3D TCAD simulations were carried out using Synopsys Sentaurus to evaluate the radiation hardness of the proposed FFs.

### 4.1 Simulation Setup

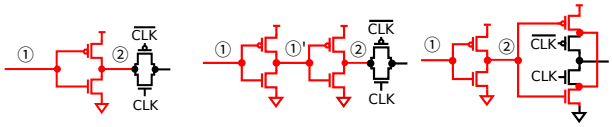
In the simulation results of $Q_{crit}$, the variation of error rates




(a) STDFF (b) DICEFF

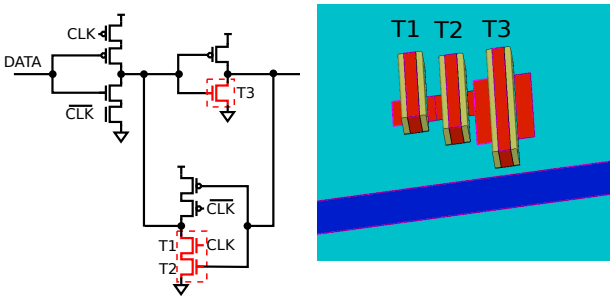
(c) PLTGFF (d) FBTIFF

Fig. 10: Simplified layout patterns of STDFF, DICEFF and the proposed FFs. They are designed in 9 wire pitches. DICEFF is designed in the double height.




(a) STDFF (b) PLTGFF (c) FBTIFF

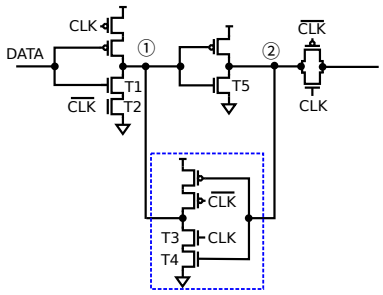
Fig. 11: The signal path from node ① to the pass transistor that connects PL and SL.



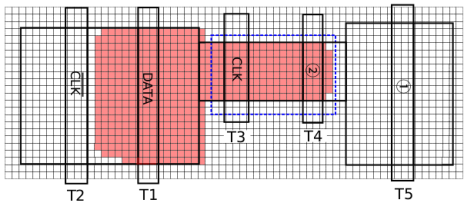

(a) Schematic (b) 3D device

Fig. 12: Schematic and 3D device structure on TCAD.

due to the increase in diffusion area was not taken into account. Therefore, to investigate the impact of diffusion area on soft errors, a 3D structure was constructed using a 65 nm bulk process for TCAD simulations. NMOS transistors in PL and SL are modeled in the device level, while the other transistors are modeled in the circuit level to reduce simulation time. The 3D device structures are shown in Fig. 12. We constructed 3D transistor models to fit static characteristics of SPICE simulation models distributed from a fabri-

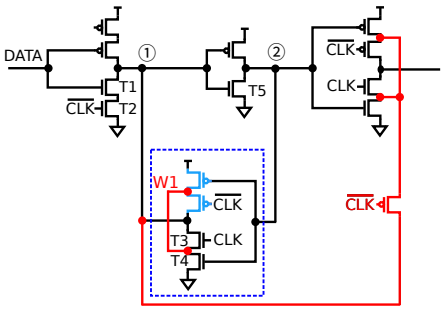



(a) Schematic

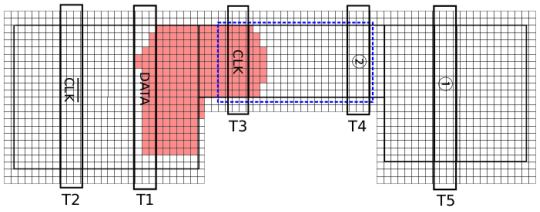



(b) Sensitive area

Fig. 13: Shape of sensitive area in PL of STDFF by heavy ions with LET of 1.4 MeV·cm$^2$/mg.




(a) Schematic




(b) Sensitive area

Fig. 14: Shape of sensitive area in PL of FBTIFF by heavy ions with LET of 1.4 MeV·cm$^2$/mg.

cation company. Current and capacitance characteristics on TCAD simulations decreased relative errors between TCAD and SPICE simulations to less than 10.4% in the region of $|V_{gs}| > 0.6$ V.

In this paper, we estimate soft error tolerance by the cross section (CS). The CS is defined as a sensitive area for soft errors. A smaller CS indicates greater resistance to soft errors [24]. In order to evaluate the CS, the 3D model transistors are split into a 20 nm square grid, and heavy ions are irradiated at the center of every grid. A Heavy ion with linear transfer (LET) of 1.4 MeV·cm$^2$/mg, which is the maximum LET of alpha particles from packages or bonding wires [25], strikes the 3D model transistors.

### 4.2 Simulation results

Table 5 shows CS values at the node ① and ③, which are vulnerable to soft errors in STDFF. The proposed FFs, especially FBTIFF, can reduce the CS of vulnerable nodes. In PL, CS is reduced by increasing $Q_{\mathrm{crit}}$ and the additional wire. Figs. 13 and 14 show the CSs in the PL of STDFF and FBTIFF. In FBTIFF, the clocked inverter in PL is split into the inverter and transmission gate to increase $Q_{\mathrm{crit}}$. Electrons generated by a particle strike combine with holes in the PMOS transistor through the additional wire (W1). Therefore, soft errors are less likely to occur in the diffusion between T3 and T4. CS is also reduced between T1 and T2 although STDFF and FBTIFF have the same structure of T1 and T2. This is because of the difference of $Q_{\mathrm{crit}}$ at node ① and the decrease in charge collection due to the distance between the drain region and the irradiation location. The diffusion region between T1 and T2 is defined as node X. As shown in Fig. 15, when a radiation particle strikes between T1 and T2, charges are generated and collected at node X and node ①. When the amount of charges collected in each diffusion area exceeds a certain amount, both of T1 and T2 are turned on and an error occurs. The farther the collision location of radiation becomes, the less charge is collected on node ① and less likely to flip the stored value. Fig. 16 shows the current and voltage waveforms at node ① when heavy ions are irradiated at the midpoint between T1 and T2. As can be seen from Fig. 16 (a), there is no significant difference in the amount of current at node ①. Therefore, the amount of charge collected at node ① is same for the both FFs. However, because of the increased $Q_{\mathrm{crit}}$ at node ①, the voltage does not drop to the threshold value and the stored value is not flipped in FBTIFF as shown in Fig. 16 (b).

CS at the node ③ is 0 cm$^2$/ion in FBTIFF by the PMOS pass transistor (P1). Fig. 17 shows simulation results of voltage waveforms by a heavy-ion strike. The SET pulse is suppressed by 56% after passing through P1.

## 5. Experimental Results

### 5.1 Setup of irradiation tests

The test chips were fabricated in a 65 nm bulk process. All FFs are implemented as shift registers. FFs are initialized

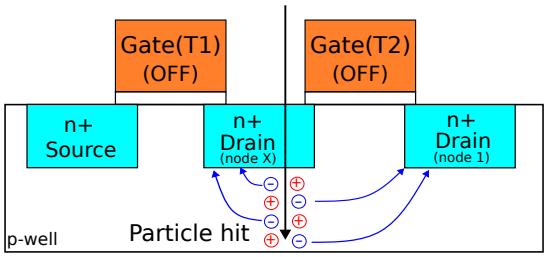
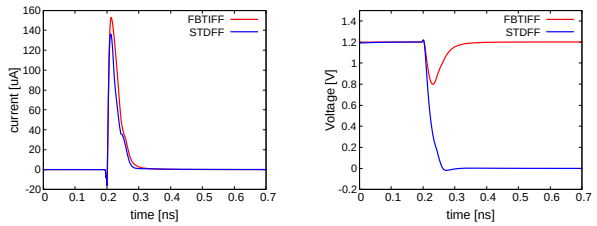



Fig. 15: Charge collection in case of radiation strike between T1 and T2.




(a) Current (b) Voltage

Fig. 16: The current and voltage waveforms at node ① when heavy ions ( LET = 1.4 MeV·cm$^2$/mg ) are irradiated at the midpoint between T1 and T2.

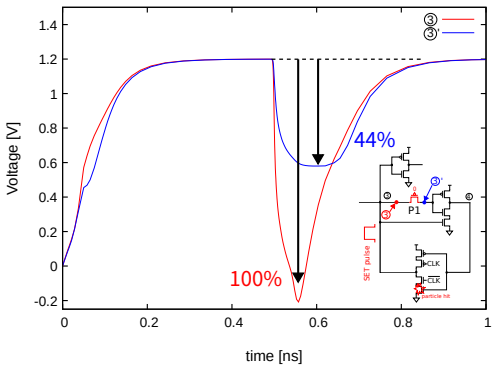



Fig. 17: TCAD simulation results. node ③ and ③' are influenced by a particle hits. P1 reduces the SET pulse by 56%.

with the same value, so DATA and Q have the same value. We evaluated soft-error tolerance by $\alpha$-particle and neutron irradiation tests. The irradiation tests were conducted as follows.

1. Initialize serially-connected FFs by all 0 or 1.
2. Stabilize CLK to 0 or 1.
3. Expose $\alpha$-particles or neutrons to FFs.
4. Read out stored data of FFs.
5. Count the number of upsets.
6. Repeat 1 - 5 for four (Q, CLK) conditions.

Soft-error rates (SERs) are calculated using Eq. (2).

$$\text{SER}\ \ [\text{FIT/Mbit}] = \frac{N_{\text{error}} \times 10^9 \times 1024^2}{N_{\text{FF}} \times F_{\text{acc}} \times t} \qquad (2)$$

$F_{\text{acc}}$ : Acceleration factor

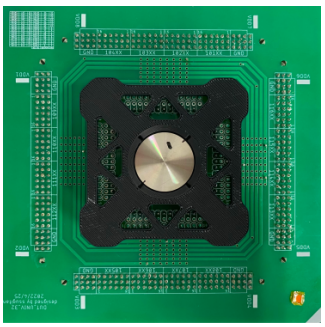


Fig. 18: $\alpha$-irradiation tests. An $\alpha$ source was placed on the test chip.

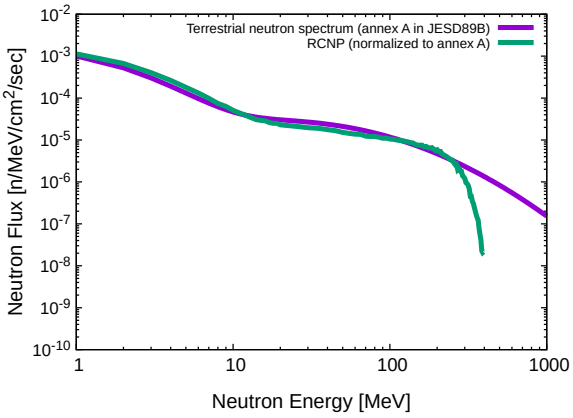



Fig. 19: Terrestrial neutron spectrum and that from spallation neutron source at RCNP.

$t$ : Measurement time [hours]
$N_{\text{error}}$ : Number of errors
$N_{\text{FF}}$ : Number of FFs

$\alpha$-particle irradiation tests were carried out using a 3 MBq $^{241}$Am source, whose size is 9.5 × 9.5 mm. As shown in Fig. 18, the $\alpha$-particle source is placed on the test chip. We exposed $\alpha$-particles to FFs for 30 seconds. The attenuation rate of $\alpha$-rays depends on the distance between $\alpha$ source and test chip. The distance between the $\alpha$ source and the chip is 0.9 mm. $F_{\text{acc}}$ of $\alpha$-particle is calculated as Eq. (3). The alpha dose emitted from the package is assumed to be 0.001 count/cm$^2$/hour for Ultra Low Alpha grade [26].

$$F_{\text{acc}} = \frac{1.5 \times 10^6\ \text{count/sec} \times 3600 \times 1/0.95^2\ \text{cm}^{-2}}{0.001\ \text{count/cm}^2\text{/hour}} \times 0.9$$
$$= 5.4 \times 10^{12} \qquad (3)$$

Neutron irradiation tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [27]. Fig. 19 shows the normalized neutron beam spectrum with the terrestrial neutron spectrum defined in JESD 89B (12.96 n/cm$^2$·h) [28]. The average $F_{\text{acc}}$ is $1.0 \times 10^8$. We exposed neutrons to FFs for 1800 seconds. In order to increase the number of errors in the limited measurement time, 32 test chips were measured simultaneously as shown in Fig. 20.

Fig. 20: Simultaneous measurement of 32 test chips at the neutron irradiation test. 16 chips are mounted on the DUT board, and two DUT boards were simultaneously irradiated.

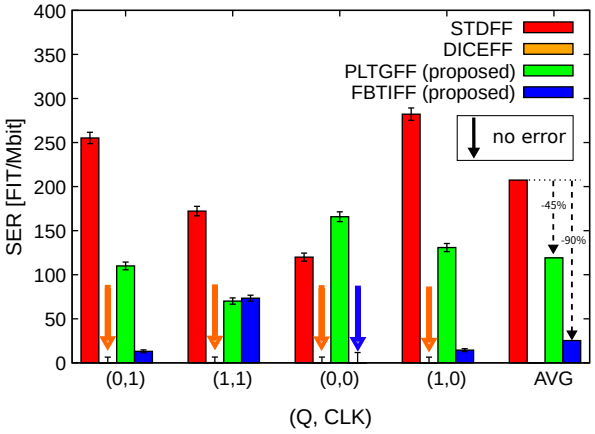



Fig. 21: $\alpha$-SER under four (Q, CLK) states and average $\alpha$-SER. Error bars are within 95% confidence. These results assume the use of the super ultra low alpha (SULA) package (0.001 cph/cm$^2$). Note that DICEFF has no error at all conditions.

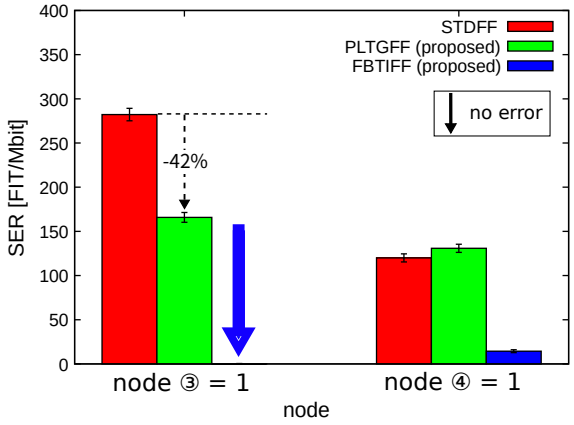



Fig. 22: $\alpha$-SER results considering the difference in (Q, CLK) between STDFF and the proposed circuits. To facilitate comparison of the results of the STDFF and the proposed circuit, it shows the error rate for each node when the value of each node is 1.

### 5.2 $\alpha$-particle irradiation

Fig. 21 shows $\alpha$-SER of the proposed FFs with error bars of 95% confidence at $V_{dd}$ = 1.2 V. The $\alpha$-SER of DICEFF is almost zero. The proposed FFs have improved soft-error tolerance compared to STDFF. However, PLTGFF has lower soft error tolerance than STDFF when (Q, CLK)=(0, 0). As shown in Figs. 3, 7 and 8, the position of the inverter connecting to the output Q is different between the STDFF and the proposed FFs. Therefore, the relationship between the measurement node and (Q, CLK) is different between STDFF and the proposed FFs. Fig. 22 shows the $\alpha$-SER considering the difference of (Q, CLK) between STDFF and the proposed circuits. To facilitate comparison of the results of the STDFF and the proposed circuits, Fig. 22 shows the SER when the value of each node is 1. According to the result, the $\alpha$-SER of PLTGFF is 42% smaller than STDFF when node ③ = 1. The $\alpha$-SER of FBTIFF is 0 when node ③ = 1. Therefore, the proposed FFs have improved soft-error tolerance at the vulnerable nodes (node ① and ③) compared to STDFF because of increased $Q_{crit}$. The overall SERs are 45% lower for PLTGFF and 90% lower for FBTIFF than STDFF.

### 5.3 Neutron irradiation

Fig. 23 shows neutron-SER (n-SER) of the proposed FFs with error bars of 95% confidence at $V_{dd}$ = 1.2 V. The n-SER of DICEFF is almost zero, indicating that it is sufficiently resistant to terrestrial neutrons. Compared to STDFF, the soft-error tolerance of FBTIFF is improved at (Q, CLK) = (0, 0), (0, 1), and (1, 0) while FBTIFF was weak at (Q, CLK) = (1, 1) due to insufficient $Q_{crit}$. The soft-error tolerance of PLTGFF is improved at (Q, CLK) = (0, 1) and (1, 0). However, PLTGFF is weak at (Q, CLK) = (0, 0) and (1, 1). From Table 1, when (Q, CLK) = (1, 1), a soft error occurs in the NMOS drain region at node ② in STDFF and at node ①' in PLTGFF. From Table 2 (a), $Q_{crit}$ of PLTGFF is less than that of STDFF in (Q, CLK) = (1, 1). When CLK = 0, the relationship between the measurement node and (Q, CLK) is different between STDFF and the proposed FFs as described in Section 5.2. Fig. 24 shows the n-SER results considering the difference in (Q, CLK) between STDFF and the proposed circuits. According to the result, the n-SER are 42% lower for PLTGFF and 84% lower for FBTIFF than STDFF when node ③ = 1. The overall SERs are 18% lower for PLTGFF and 35% lower for FBTIFF than STDFF.

### 5.4 Discussions

Fig. 25 shows the sum of $\alpha$- and n-SERs of STDFF, DICEFF, and the proposed FFs. Each SER is the average of all four (Q, CLK) conditions. For all FFs, n-SER is larger than $\alpha$-SER. Thus, the error rate due to neutrons is higher than due to $\alpha$ particles in the terrestrial environment. In [29], it was reported that $\alpha$ particles have a higher rate of change in SER

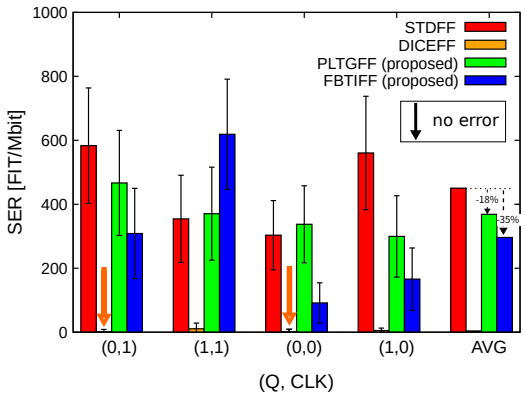



Fig. 23: n-SER under four (Q, CLK) states and average. Error bars are within 95% confidence.

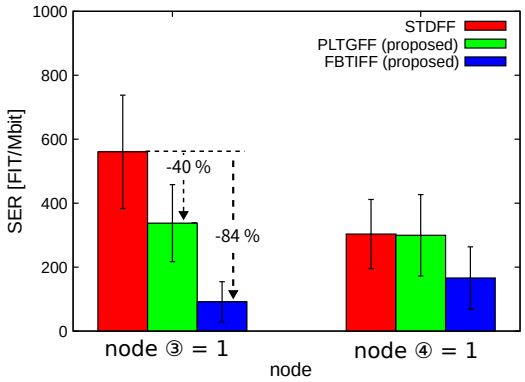



Fig. 24: n-SER results considering the difference in (Q, CLK) between STDFF and the proposed circuits. To facilitate comparison of the results of the STDFF and the proposed circuit, it shows the error rate for each node when the value of each node is 1.

with respect to $Q_{\mathrm{crit}}$ than neutrons due to the difference of the LET of the particles. Therefore, the tolerance to $\alpha$ particle irradiation of the proposed FFs is better than that to neutron irradiation. Both $\alpha$- and n-SERs of DICEFF are almost zero, ensuring sufficient soft-error tolerance. The proposed FFs are not as soft-error tolerant as DICEFF. However, the SERs in the terrestrial environment are reduced by 25% for PLTGFF and 50% for FBTIFF compared to STDFF.

Fig. 26 shows the 2-dimensional charts of plotting performance overheads and soft-error tolerance of those FFs. The value of SER is the sum of $\alpha$- and n-SER. The SER and performances are normalized to the STDFF value. The numerical values in the graph indicate the distance from the origin. The smaller they are, the better the trade-off between performances and reliability becomes. The figure shows that DICEFF has the highest soft-error tolerance with relatively large performance overhead. In the terrestrial environment, the proposed FFs have better trade-offs between reliability and performance compared to DICEFF and STDFF. In particular, PLTGFF is better in terms of area, and FBTIFF is better in terms of delay in the terrestrial environment.

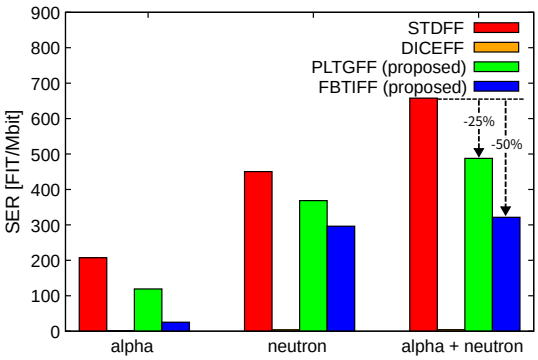
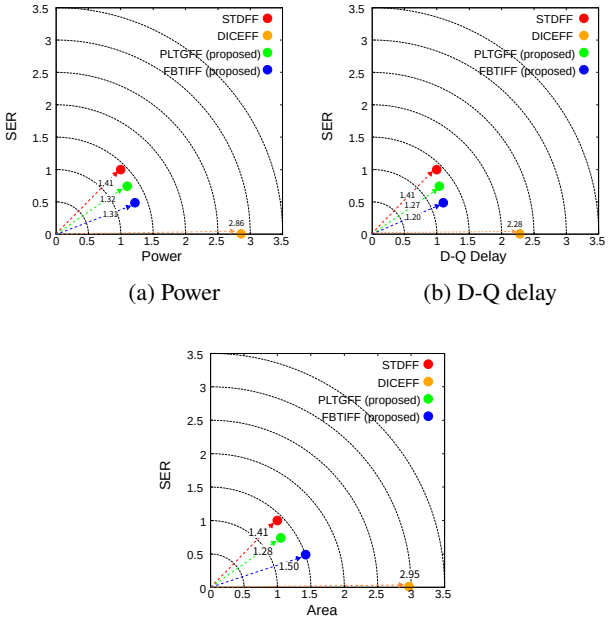



Fig. 25: Sum of $\alpha$- and n- SER. Each SER is the average of all four (Q, CLK) conditions.




(a) Power (b) D-Q delay

(c) Area

Fig. 26: 2 dimensional charts of soft error tolerance and each performance (Area, D-Q delay, Power). SER is the sum of $\alpha$-SER and n-SER. SER and each performance are normalized by the STDFF value.

These circuit structures could be applied to other soft-error countermeasure methods. For example, a countermeasure was proposed to improve soft error tolerance by modifying the latch structure in the multiplexing circuit [30]. TMRFF triples the STDFF. By using the proposed circuit instead of STDFF, further improvement of soft-error tolerance in outer space is expected. Furthermore, in the FDSOI process, the carrier collection efficiency is less than the bulk process [31]. Thus the proposed countermeasures are especially effective to the FDSOI process. Adapting the proposed

circuit to these countermeasures is expected to improve soft-error tolerance further not only in the terrestrial environment but also in outer space.

## 6. Conclusion

Redundant flip flops are strong against soft errors with large performance overheads. We proposed radiation-hardened FFs for terrestrial applications balancing performance overheads and radiation hardness. $Q_{\mathrm{crit}}$ at the vulnerable nodes are increased by changing circuit topologies with additional transistors and wires. These proposed FFs have fewer transistors and have lower performance overhead than conventional multiplexed circuits. The proposed FFs can suppress the D-Q delay increase less than 10%. The performance overheads of the proposed FFs are smaller than DICEFF. We fabricated the proposed FFs in a 65 nm bulk process. By $\alpha$ and neutron irradiation tests, PLTGFF and FBTIFF reduce soft error rates by 25% and 50%, respectively. Although the proposed FFs are weaker for soft errors than DICEFF, they have better trade-offs between reliability and performance than DICEFF and STDFF.

## Acknowledgement

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## Appendix: Netlists

The netlists of the three circuits used for circuit simulation are shown below. UW is the value of the normalized gate width.

STDFF

```
.SUBCKT STDFF CP D Q VDD VSS
MM22 net21 net49 VSS VSS nch l=60n UW=1.50
MM20 net49 CP VSS VSS nch l=60n UW=1.62
MM19 net018 net21 net28 VSS nch l=60n UW=1.66
MM28 Q net33 VSS VSS nch l=60n UW=3.25
MM14 net33 net28 VSS VSS nch l=60n UW=3.25
MM27 net43 net33 VSS VSS nch l=60n UW=1.25
MM24 net28 net49 net43 VSS nch l=60n UW=1.25
MM9 net45 net018 VSS VSS nch l=60n UW=1.25
MM6 net013 net21 net45 VSS nch l=60n UW=1.25
MM4 net018 net013 VSS VSS nch l=60n UW=3.25
MM3 net47 net49 VSS VSS nch l=60n UW=3.08
MM0 net013 D net47 VSS nch l=60n UW=3.08
MM23 net21 net49 VDD VDD pch l=60n UW=2.16
MM21 net49 CP VDD VDD pch l=60n UW=2.16
MM18 net018 net49 net28 VDD pch l=60n UW=1.79
MM29 Q net33 VDD VDD pch l=60n UW=4.33
MM15 net33 net28 VDD VDD pch l=60n UW=4.33
MM26 net28 net21 net44 VDD pch l=60n UW=1.25
MM25 net44 net33 VDD VDD pch l=60n UW=1.25
MM8 net013 net49 net46 VDD pch l=60n UW=1.25
MM7 net46 net018 VDD VDD pch l=60n UW=1.25
MM5 net018 net013 VDD VDD pch l=60n UW=4.33
MM2 net013 D net48 VDD pch l=60n UW=3.83
MM1 net48 net21 VDD VDD pch l=60n UW=3.83
.ENDS
```

PLTGFF

```
.SUBCKT PLTGFF CP D Q VDD VSS
MM22 net21 net49 VSS VSS nch l=60n UW=1.50
MM20 net49 CP VSS VSS nch l=60n UW=1.62
MM19 net026 net21 net28 VSS nch l=60n UW=1.66
MM28 Q net28 VSS VSS nch l=60n UW=3.25
MM14 net33 net28 VSS VSS nch l=60n UW=3.25
MM27 net43 net33 VSS VSS nch l=60n UW=1.25
MM24 net28 net49 net43 VSS nch l=60n UW=1.25
MM32 net026 net25 VSS VSS nch l=60n UW=3.25
MM31 net16 net21 net026 VSS nch l=60n UW=1.25
MM4 net25 net16 VSS VSS nch l=60n UW=3.25
MM3 net47 net49 VSS VSS nch l=60n UW=3.08
MM0 net16 D net47 VSS nch l=60n UW=3.08
MM23 net21 net49 VDD VDD pch l=60n UW=2.16
MM21 net49 CP VDD VDD pch l=60n UW=2.16
MM18 net026 net49 net28 VDD pch l=60n UW=1.70
MM29 Q net28 VDD VDD pch l=60n UW=4.33
MM15 net33 net28 VDD VDD pch l=60n UW=4.33
MM26 net28 net21 net44 VDD pch l=60n UW=2.50
MM25 net44 net33 VDD VDD pch l=60n UW=2.50
MM30 net16 net49 net026 VDD pch l=60n UW=2.50
MM33 net026 net25 VDD VDD pch l=60n UW=4.33
MM5 net25 net16 VDD VDD pch l=60n UW=4.33
MM2 net16 D net48 VDD pch l=60n UW=3.83
MM1 net48 net21 VDD VDD pch l=60n UW=3.83
.ENDS
```

FBTIFF

```
.SUBCKT FBTIFF CLK D Q VDD VSS node1
node1n
MM43 node4 net52 net046 VSS nch l=60n UW=3.08
MM9 net046 node3 VSS VSS nch l=60n UW=3.08
MM7 net042 node4 VSS VSS nch l=60n UW=1.66
MM65 net048 node1n VSS VSS nch l=60n UW=1.66
MM0 node1 D net125 VSS nch l=60n UW=3.08
MM3 net125 cn VSS VSS nch l=60n UW=3.08
MM4 node1n node1 VSS VSS nch l=60n UW=3.08
MM32 node2 node1n VSS VSS nch l=60n UW=3.12
MM24 node3 cn net042 VSS nch l=60n UW=1.66
MM66 node1 cp net048 VSS nch l=60n UW=1.66
MM28 Q node3 VSS VSS nch l=60n UW=3.08
MM19 node2 cp node3 VSS nch l=60n UW=1.66
```

```
MM20 cn CLK VSS VSS nch l=60n UW=1.62
MM22 cp cn VSS VSS nch l=60n UW=1.50
MM40 node3 VSS net52 VDD pch l=60n UW=1.00
MM8 node4 net52 VDD VDD pch l=60n UW=3.83
MM6 net127 node4 VDD VDD pch l=60n UW=2.50
MM1 net124 cp VDD VDD pch l=60n UW=3.83
MM2 node1 D net124 VDD pch l=60n UW=3.83
MM5 node1n node1 VDD VDD pch l=60n UW=4.33
MM33 node2 node1n VDD VDD pch l=60n UW=4.33
MM46 node1 cn node2 VDD pch l=60n UW=3.16
MM72 net048 node1n VDD VDD pch l=60n UW=2.75
MM26 node3 cp net127 VDD pch l=60n UW=2.50
MM29 Q node3 VDD VDD pch l=60n UW=3.83
MM18 node2 cn node3 VDD pch l=60n UW=1.79
MM21 cn CLK VDD VDD pch l=60n UW=2.16
MM23 cp cn VDD VDD pch l=60n UW=2.16
MM71 node1 cn net048 VDD pch l=60n UW=2.75
.ENDS
```

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