IEICE TRANSACTIONS

on Electronics

DOI:10.1587/transele.2024ECS6003

Publicized:2024/07/17

This advance publication article will be replaced by the finalized version after proofreading.

A PUBLICATION OF THE ELECTRONICS SOCIETY

The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3chome, Minato-ku, TOKYO, 105-0011 JAPAN

BRIEF PAPER

Ga-Sn-O thin film, mist-CVD method, and analog memristor: promising proposals for neuromorphic systems

Ryo ITO†, Sumio SUGISAKI†, Toshiyuki KAWAHARAMURA,†† Tokiyoshi MATSUDA†††,†, *Nonmember*, Hidenori KAWANISHI†,††††, *Member*, *and* Mutsumi KIMURA†,††††, *Senior member*

SUMMARY Promising proposals of a material, deposition process, and storage device have been demonstrated for neuromorphic systems. The material is Ga-Sn-O (GTO), amorphous metal-oxide semiconductor, and does not contain rare metals such as In. The deposition process is a mist chemical-vapor-deposition (CVD) method, atmospheric pressure process. Therefore, the material and fabrication costs can be simultaneously saved, and three-dimensional stacked structures will be possible. The storage device is an analog memristor, a kind of memristors, but has continuous conductance, and analog computing will be possible owing to continuous weights of synapse elements in neural networks. These structures and computing are the same as those in living brains. We have succeeded in attaining an analog memristive characteristic by optimizing the Ga:Sn composition rate, namely, completing an analog memristor. The analog memristor of the GTO thin film by the mist CVD method can be expected to be a key component for neuromorphic systems.

key words: *Ga-Sn-O (GTO), thin film, mist-CVD, analog memristor, neuromorphic system*

1. Introduction

Artificial intelligences are indispensable concepts in present and future societies [1,2], whose hardware is being investigated to be realized in two approaches: Neumann-type computers [3,4] and neuromorphic systems [5-8]. Neumann-type computers are wholly based on digital technologies, whose fundamental function can be typified only to execute numerical computation exactly and speedily. The main materials are silicon, deposition processes are vacuum processes, storage devices are binary memories, etc., which are optimized to achieve the abovementioned function [9-11]. On the other hand, neuromorphic systems are anticipated to be accomplished with analog technologies partially at least, whose desired functions are broadly cognitive behaviors. Currently, the conventional technologies for the Neumann-type computers are also used as those for the neuromorphic systems [12,13]. However, since the cognitive behaviors are excellently exercised in living brains, it is reasonable that the materials, deposition processes, storage devices, etc., should enable the similar organizations of living brains [14].

In this research, promising proposals of a material, deposition process, and storage device have been demonstrated for neuromorphic systems. The material is Ga-Sn-O (GTO) [15,16], which is an amorphous metal-oxide semiconductor (AOS) [17] and does not contain rare metals such as In, and therefore the material cost can be saved. The deposition process is a mist chemical-vapor-deposition (CVD) method, which is an atmospheric pressure process, and therefore the fabrication cost can be also saved at the same time [18,19]. Moreover, it is fine-channel type, which can improve the thickness uniformity and film quality. As a result, by employing the combination of the GTO and mist CVD technologies, three-dimensional stacked structures will be possible [20,21], which are the same as those in living brains. The storage device is an analog memristor, which is a kind of memristors [22-25] that are often made of GTO [26,27] and other AOS [28-31], but has continuous conductance according to preceding history of voltage application [32-34]. By employing the analog memristor, analog computing will be possible because the electric conductance can be corresponded to continuous weights of synapse elements in neural networks, which is also the same as that in living brains. Here, the material of the GTO is formed by the deposition process of the mist-CVD method to complete the storage device of the analog memristor. These technologies are simultaneously combined for the first time. In the following paragraphs, first, the device structure and deposition process will be explained, next, the structural analysis is shown, afterwards, analog memristive characteristics will be confirmed, and finally, the working mechanism is discussed.

2. Device Structure and Deposition Process

The device structure and deposition process are shown in Fig. 1. As shown in Fig. 1(a), first, a quartz substrate is used, and a Ti thin film is deposited using a vacuum evaporation method as a bottom electrode. As shown in Fig. 1(b), next, a GTO thin film is deposited using the mist-CVD method as a conductance change layer. Ga acetylacetonate (Ga(acac)) and Sn acetylacetonate (Sn(acac)) are dissolved in HCl of

† The authors are with Ryukoku University, Otsu, 520-2194 Japan.
†† The author is with Kochi University of Technology, Kami, 782-8502, Japan.
††† The author is with Kindai University, Higashiosaka, 577-8502 Japan.
†††† The authors are with Nara Institute of Science and Technology (NAIST), Ikoma, 630-0192 Japan.

Copyright © 20XX The Institute of Electronics, Information and Communication Engineers

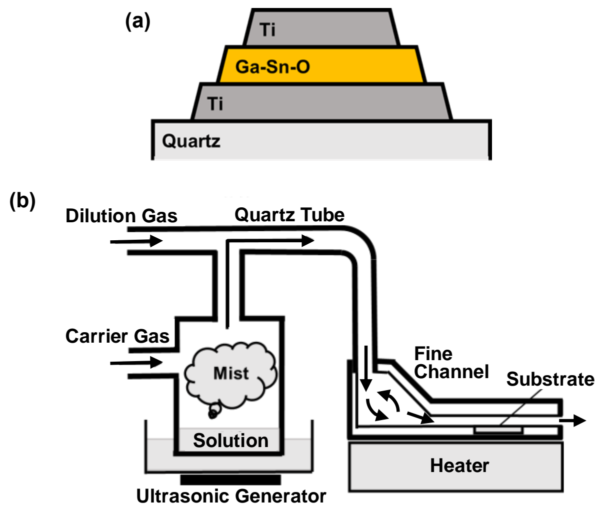

Fig. 1 Device structure and deposition process.

(a) Device structure. The device structure is very simple, namely, the GTO thin film is sandwiched between the top and bottom electrodes. (b) Deposition method. Since the flowing speed in the fine channel is sufficiently speedy, a reaction-limiting condition is obtained, which can improve the thickness uniformity and film quality.

20 % of 3 g and H_2O of 40 mL, and the volumes of the Ga(acac) and Sn(acac) are adjusted to the total mol concentration of 0.03 mol/L. The composition ratio of the atoms are varied to Ga:Sn = 1:1 ~ 1:5 in the solution. A mist of the solution is generated by ultrasonic generators, carried by a carrier gas of air of the flow rate of 2 L/min, diluted by a dilution gas of air of the flow rate of 1 L/min, and injected through a quartz tube into a fine channel. Since the flowing speed in the fine channel is sufficiently speedy, not a supply-limiting condition but a reaction-limiting condition is obtained, which can enhance the process stability and improve the thickness uniformity and film quality. The fine channel is heated to the temperature of 400 °C by a heater, and the GTO thin film is deposited during the deposition time of 20 min. Incidentally, the temperature is carefully optimized to this one. Below 400 °C, the GTO thin film is hardly deposited because the decomposition of the Ga(acac) and Sn(acac) does not seem to occur sufficiently, whereas above that, the Ti thin film as the bottom electrode is damaged, and the GTO thin film is hardly deposited on the substrate again because the decomposition of the Ga(acac) and Sn(acac) seems to occur before they reach the substrate. Finally, a Ti thin film is again deposited using a vacuum evaporation method as a top electrode. The device structure is very simple, namely, the GTO thin film is sandwiched between the top and bottom electrodes.

3. Structural Analysis

The structural analysis is shown in Fig. 2. The thickness distributions are shown in Fig. 2(a). It is found that the thickness distributions are relatively flat and uniform. The dependences of the film thickness and root-mean-square of

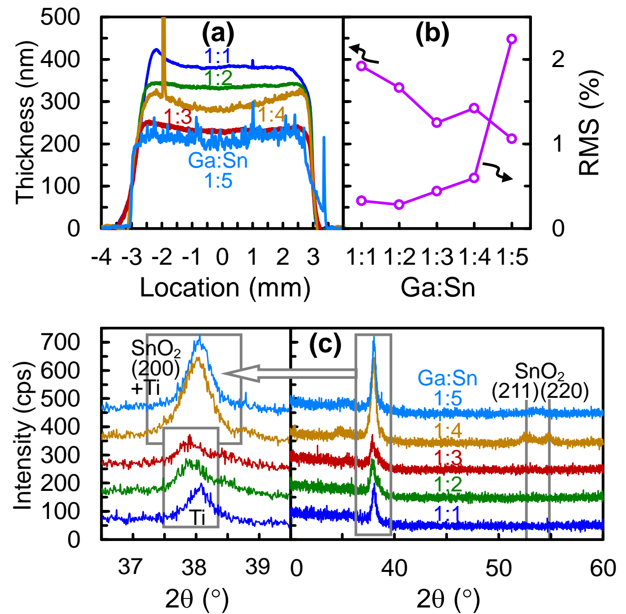

Fig. 2 Structural analysis.

(a) Thickness distributions. The thickness distributions are relatively flat and uniform. (b) Dependences of the film thickness and RMS on the Ga:Sn. The film thickness decreases as Ga:Sn increases, and the film roughness increases as Ga:Sn increases and becomes quite rough when Ga:Sn = 1:5. (c) XRD patterns. The crystal peaks of SnO_2 appear when Ga:Sn = 1:4 and 1:5. It can be suggested that the film roughness increases because the GTO film changes from an amorphous to polycrystalline phase.

the film roughness (RMS) on the Ga:Sn are shown in Fig. 2(b). It is found that the film thickness decreases as Ga:Sn increases. Moreover, it is also found that the film roughness increases as Ga:Sn increases, and it becomes quite rough when Ga:Sn = 1:5. The XRD patterns are shown in Fig. 2(c). It is found that the crystal peaks of SnO_2 (211) and (200) appear when Ga:Sn = 1:4 and 1:5, and the crystal peak of SnO_2 (200) significantly increases at that Ga:Sn, although this peak overlaps on the peak of Ti. As a result, it can be suggested that the film roughness becomes rough because the GTO thin film changes from an amorphous phase to a polycrystalline phase.

4. Electrical Characteristics

The electrical characteristics are shown in Fig. 3. The dependences on Ga:Sn are shown in Fig. 3(a). Here, an applied voltage to the top electrode (V) is scanned to 0 V ~ +5 V ~ 0 V ~ -5 V ~ 0 V, and the flowing current (I) is measured. Three samples are measured for each Ga:Sn. The maximum positive voltage is defined as a set voltage (Vset), because a set transition from the low conductance state (LCS) to the high conductance state (HCS) is guessed to occur, whereas the maximum negative voltage is defined as a reset voltage (Vreset), because a reset transition reversely is guessed to occur. It is found that hysteresis curves are observed when Ga:Sn = 1:1 and 1:2, and it becomes greatest when Ga:Sn = 1:3 and fades when Ga:Sn = 1:4 and 1:5. The

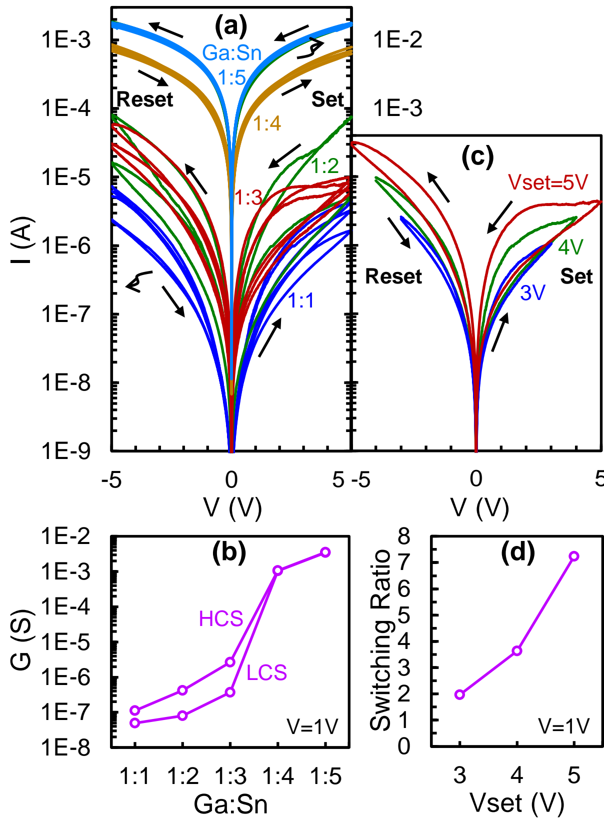

Fig. 3 Electrical characteristics.

(a) Dependences on Ga:Sn. Hysteresis curves are observed when Ga:Sn = 1:1 and 1:2, and it becomes greatest when Ga:Sn = 1:3 and fades when Ga:Sn = 1:4 and 1:5. (b) Electric conductance. The electric conductance increases as Ga:Sn increases and becomes quite high when Ga:Sn = 1:4 and 1:5. It can be suggested that the hysteresis curve fades and the electric conductance becomes high because the GTO film changes from an amorphous to polycrystalline phase. (c) Analog memristive characteristics. The hysteresis width increases as Vset increases. (d) Switching ratio. The switching ratio increases as the Vset increases. It can be concluded that an analog memristor has been completed.

electric conductance is shown in Fig. 3(b). Here, the electric conductance is measured for the LCS and HCS at V = +1 V. It is found that the electric conductance increases as Ga:Sn increases, and it becomes quite high when Ga:Sn = 1:4 and 1:5. Along with the result of the structural analysis, as a result, it can be suggested that the hysteresis curve fades and the electric conductance becomes high because the GTO film changes from an amorphous phase to a polycrystalline phase.

The analog memristive characteristics are shown in Fig. 3(c). Here, Ga:Sn = 1:3, and Vset is regulated to 3 V ~ 5 V. It is found that the hysteresis width increases as Vset increases. The switching ratio is shown in Fig. 3(d). Here, the switching ratios are calculated from the conductance ratios between the LCS and HCS at V = +1 V. It is found that the switching ratio increases as the Vset increases. It can be concluded that we have succeeded that an analog memristive characteristic has been attained by optimizing the Ga:Sn composition rate, namely, an analog memristor has been completed.

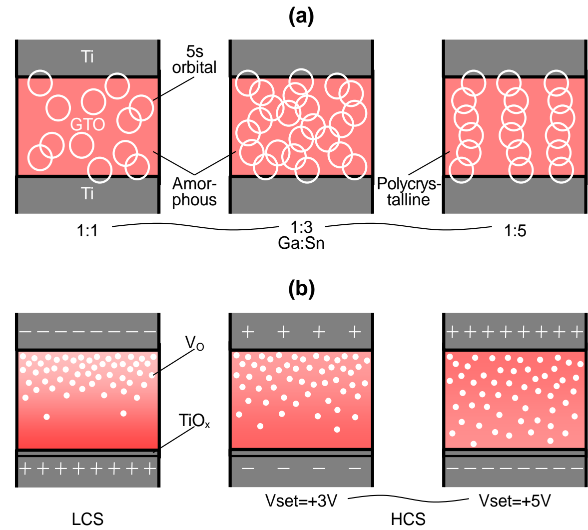

Fig. 4 Working mechanism..

(a) Dependences on Ga:Sn. When Ga:Sn = 1:3, although the GTO is in the amorphous phase, Sn is enough to form the percolation paths and increase the electric conductance. When Ga:Sn = 1:5, since the GTO is in the polycrystalline phase, the grain boundaries may form firm paths with V_O, fade the hysteresis curves, and heighten the electric conductance. (b) Analog memristive characteristic. Since pure Ti remains on the interface of the top electrode and reacts with oxygen, the V_O is many near the top electrode in the GTO thin film. In the LCS, the low conductance is because the V_O is sparce near the bottom electrode that is not conductive. In the HCS, the high conductance is because the V_O drifts toward the bottom electrode, and VO is dense also there that is conductive.

5. Working mechanism

The working mechanism is shown in Fig. 4. The dependence on Ga:Sn is shown in Fig. 4(a). Here, 5s orbitals of Sn are indicated by white circles. It is known that the outermost-shell s orbitals form the conductive paths in AOS, which are 5s orbitals of Sn in GTO. When Ga:Sn = 1:1, Sn is not enough in amount for 5s orbitals to form the percolation paths. When Ga:Sn = 1:3, although the GTO thin film is in the amorphous phase, Sn is enough to form the percolation paths, and the electric conductance increases. When Ga:Sn = 1:5, since the GTO thin film is in the polycrystalline phase, the grain boundaries may form well-ordered and firm paths. If it is assumed that the oxygen vacancies (V_O) are collected and fixed at the grain boundaries, the hysteresis curves fades, and the electric conductance becomes quite high.

The analog memristive characteristic is shown in Fig. 4(b). Here, V_O is indicated by white dots. It is assumed that TiO_x exists on the interface of the bottom electrode, because the interface is exposed to normal air and high temperature air at the beginning of the mist-CVD method. Since the TiO_x does not react with oxygen further, oxygen is enough near the bottom electrode in the GTO thin film, and the V_O is few. On the other hand, pure Ti remains on the interface of the top electrode, because the interface is exposed to nothing. Since the Ti reacts with oxygen, oxygen is not enough near the top electrode in the GTO thin film, and the V_O is many.

In the LCS, the reason for the low conductance is because the V_O is sparce near the bottom electrode that is not conductive. On the other hand, in the HCS, the reason for the high conductance is because the V_O drifts toward the bottom electrode by the electric field, and V_O is dense also near the bottom electrode that is conductive. Since the density of the V_O depends on the Vset, the electric conductance increases as the Vset increases, namely, analog memristive characteristic has been attained.

6. Conclusion

Promising proposals of a material, deposition process, and storage device have been demonstrated for neuromorphic systems. The material is GTO, which is an AOS and does not contain rare metals such as In. The deposition process is a mist-CVD method, which is an atmospheric pressure process. Therefore, the material and fabrication costs can be saved at the same time, and three-dimensional stacked structures will be possible. The storage device is an analog memristor, which is a kind of memristors but has continuous conductance, and analog computing will be possible owing to continuous weights of synapse elements in neural networks. These structures and computing are the same as those in living brains. These technologies were simultaneously combined for the first time. Here, we have succeeded that an analog memristive characteristic has been attained by optimizing the Ga:Sn composition rate, namely, an analog memristor has been completed. The analog memristor consisting of the GTO thin film deposited by the mist CVD method can be expected to be a key component for neuromorphic systems. Although the detailed way to implement the analog memristors into neuromorphic systems were not described in this paper, all conventional memristors can be replaced with the analog memristors in this paper.

Acknowledgments

This work is supported in part by JSPS KAKENHI (A) 22H00515, (C) 19K11876, JST SICORP Taiwan, ALCA-Next, High-Tech Research Center in Ryukoku University, Laboratory for Materials and Structures in Tokyo Institute of Technology, and Research Institute of Electrical Communication in Tohoku University. We also would like to thank Dr. Ryohei Takahashi of Ryukoku University for useful discussion on the related experiments.

References

[1] J. McCarthy, M. L. Minsky, N. Rochester, and C. E. Shannon, A Proposal for the Dartmouth Summer Research Project on Artificial Intelligence, Dartmouth Conference, (1956).
[2] S. Russell and P. Norvig, Artificial Intelligence: A Modern Approach, Global Edition. Pearson Education (2016).
[3] M. D. Godfrey and D. F. Hendry, IEEE Annals of the History of Computing 15, 11 (1993).
[4] J. von Neumann, IEEE Annals of the History of Computing, 15, 27 (1993).
[5] C. Mead, Proc. IEEE, 78, 1629 (1990).
[6] http://www.ibm.com/smarterplanet/jp/ja/brainpower/.
[7] J. Hsu, IEEE Spectrum, 51, 17 (2014).
[8] M. Suri, Advances in Neuromorphic Hardware exploiting Emerging Nanoscale Devices. Springer (2017).
[9] J. D. Plummer, M. Deal, and P. B. Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, Prentice Hall (2000).
[10] H. Geng, Semiconductor Manufacturing Handbook, 2nd Ed. McGraw Hill (2017).
[11] B. Keeth, R. J. Baker, B. Johnson, and F. Lin, DRAM Circuit Design: Fundamental and High-Speed Topics. Wiley-IEEE Press (2007).
[12] https://research.ibm.com/blog/northpole-ibm-ai-chip
[13] https://www.intel.com/content/www/us/en/research/neuromorphic-computing-loihi-2-technology-brief.html
[14] E. Kandel, J. Schwartz, T. Jessell, S. Siegelbaum, and A.J. Hudspeth, Principles of Neural Science, 5th Ed., McGraw-Hill Professional (2012).
[15] T. Matsuda, K. Umeda, Y. Kato, D. Nishimoto, M. Furuta, and M. Kimura, Scientific Reports 7, 44326 (2017).
[16] T. Matsuda, M. Uenuma, and M. Kimura, Jpn. J. Appl. Phys. 56, 070309 (2017).
[17] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature 432, 488 (2004).
[18] J.-G. Lu, T. Kawaharamura, H. Nishinaka, Y. Kamada, T. Oshima, and S. Fujita, J. Crystal Growth 299, 1 (2007).
[19] G. T. Dang, T. Kawaharamura, M. Furuta, and M. W. Allen, IEEE Electron Device Lett. 36, 463 (2015).
[20] K. Nomura, T. Aoki, K. Nakamura, T. Kamiya, T. Nakanishi, T. Hasegawa, M. Kimura, T. Kawase, M. Hirano, and H. Hosono, Appl. Phys. Lett. 96, 263509 (2010).
[21] E. Iwagi, T. Tsuno, T. Imai, Y. Nakashima, and M. Kimura, IEEE J. Electron Devices Society 10, 784 (2022).
[22] L. Chua, IEEE Trans. Circuit Theory 18, 507 (1971).
[23] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, Nature 453, 80 (2008).
[24] J. J. Yang, D. B. Strukov, and D. R. Stewart, Nat. Nanotechnol. 8, 13 (2013).
[25] D. Kim, J. Kung, S. Chai, S. Yalamanchili, and S. Mukhopadhyay, ACM SIGARCH Computer Architecture News 44, 380 (2016).
[26] S. Sugisaki, T. Matsuda, M. Uenuma, T. Nabatame, Y. Nakashima, T. Imai, Y. Magari, D. Koretomo, M. Furuta, and M. Kimura, Scientific Reports 9, 2757 (2019).
[27] Y. Takishita, M. Kobayashi, K. Hattori, T. Matsuda, S. Sugisaki, Y. Nakashima, and M. Kimura, AIP Advances 10, 035112 (2020).
[28] B. Lu, Y. Lu, H. Zhu, J. Zhang, S. Yue, S. Li, F. Zhuge, Z. Ye, and J. Lu, Mater. Lett. 249, 169 (2019).
[29] S.-Y. Min and W.-J. Cho, Nanomaterials 11, 1081 (2021).
[30] M. E. Pereira, J. Deuermeier, P. Freitas, P. Barquinha, W. Zhang, R. Martins, E. Fortunato, and A. Kiazadeh, APL Mater. 10, 011113 (2022).
[31] R. A. Martins, E. Carlos, J. Deuermeier, M. E. Pereira, R. Martins, E. Fortunato, and A. Kiazadeh, J. Mater. Chem. C 10, 1991 (2022).
[32] M. Kimura, R. Sumida, A. Kurasaki, T. Imai, Y. Takishita, and Y. Nakashima, Scientific Reports 11, 580 (2021).
[33] D. Makioka, S. Shiomi, and M. Kimura, IEEE J. Electron Devices Soc. 11, 174 (2023).
[34] T. Katagiri, T. Matsuda, H. Kawanishi, and M. Kimura, Jpn. J. Appl. Phys. 62, 058002 (2023).