IEICE TRANS. ELECTRON., VOL.E100–C, NO.2 FEBRUARY 2017

INVITED PAPER *Special Section on Fabrication Technologies Supporting the Photonic/Nanostructure Devices*

Dry Etching Technologies of Optical Device and III-V Compound Semiconductors

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SUMMARY Dry etching is one of the elemental technologies for the fabrication of optical devices. In order to obtain the desired shape using the dry etching process, it is necessary to understand the reactivity of the materials being used to plasma. In particular, III-V compound semiconductors have a multi-layered structure comprising a plurality of elements and thus it is important to first have a full understanding of the basic trends of plasma dry etching, the plasma type and the characteristics of etching plasma sources. In this paper, III-V compound semiconductor etching for use in light sources such as LDs and LEDs, will be described. Glass, LN and LT used in the formation of waveguides and MLA will be introduced as well. And finally, the future prospects of dry etching will be described briefly.

key words: *optical device, III-V compound semiconductor, dry etching, LD, LED, glass*

1. Introduction

The history of III-V compound semiconductor development goes as far back as that of optical devices. It was found that III-V compound semiconductors are capable of achieving characteristics far superior to silicon semiconductors through a combination of various selective elements. Its applications include photo-detectors, high-frequency transistors, and Solid State Lighting (SSL) such as light emitting diodes (LED) and laser diodes (LD). In addition, it has recently been observed to be useful in the field of power devices too.

Looking back on when the mass production of III-V compound semiconductors was introduced, the increasing demand for mobile phone technologies had ushered in the era of GaAs. Soon after, with the spread of LEDs for general lighting and liquid crystal display (LCD) backlights, GaN was introduced. In time, the mass production of power devices is also expected.

Figure 1 and Fig. 2 illustrate the dry etching processes of III-V compound semiconductors and optical devices.

LD: Bilayer mesa etching
Vertical cavity surface emitting laser (VCSEL):
Non-selective etching of multi layer substrate
LED: Mesa and isolated etching of GaN,
Patterned sapphire substrate (PSS)
Optical fiber, Photo-detector, etc.:
Formed waveguide, micro lens array (MLA)

Manuscript received June 7, 2016.
Manuscript revised September 15, 2016.
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DOI: 10.1587/transele.E100.C.150

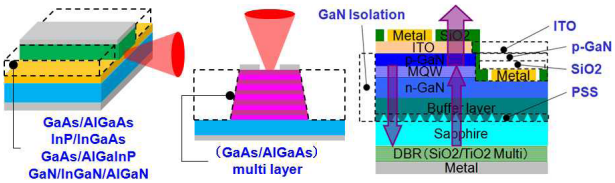


Fig. 1 Schematic of device structure and etching part of (a) LD, (b) LED

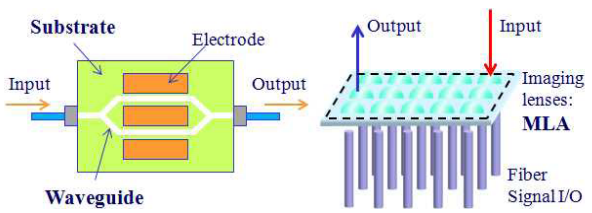


Fig. 2 Formation point of (a) waveguide, (b) MLA

This paper will discuss the latest trends, and the prospects of plasma dry etching technology for optical devices focusing mainly on III-V compound semiconductors.

2. Plasma Dry Etching

Table 1 shows the characteristics of a plasma dry etching reaction.

Chemical etching is a result of reactions with radicals and it is isotropic. Similar to wet etching, the etching rate (E/R) and the selectivity are high while the etching damage (e.g., ion damage, charge up damage) is low. Figure 3 shows the vapor pressure curve of reaction products. For example, in the case of Al, it is observed that $AlCl_3$ volatilizes at 40 degrees Celsius or higher.

On the other hand, physical etching is a method whereby a material is exposed to ion bombardment, which leads to anisotropic etching. The etching rate and the selectivity are low while the etching damage is high. However, as shown in Fig. 4, upon ion bombardment, sputtered particles will have a distribution of emission angles. As a result, it is not recommended for vertical processing through sidewall redeposition.

By using a mix of both chemical etching and physical etching to stimulate chemical reactions through ion bombardment, it is possible to control the shape of the etching.

Table 1 Characteristic of plasma dry etching reaction

	Chemical etching	Physical etching	Chemical physical etching
	radical	+ ion	+ ion
	Isotropic etching	Sputter etching Anisotropic etching	Reactive ion etching Anisotropic etching
E/R	High	Low	Mid
Selectivity	High	Low	Mid
Damage	Low	High	Mid

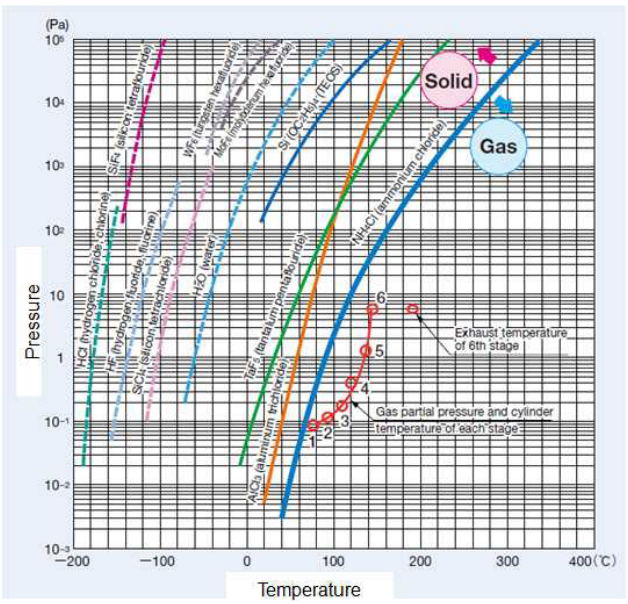
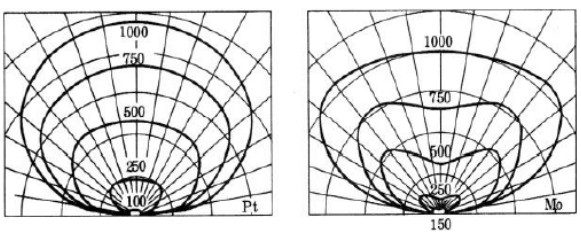


Fig. 3 Vapor pressure curve of reaction products



(a) (b)

Fig. 4 Emission angle distribution of sputtered particles, (a) Pt, (b) Mo

Subsequently, in Table 2, the volatilization temperature of the reaction products of a representative constituent element used in a compound semiconductor are recorded. It was observed that most of the materials volatilized by reacting with Cl. However, Indium (In) requires a high relativity reaction temperature of approximately 200 degrees Celsius. On the down side, it is highly likely that the surface materials As, P, and N are damaged by the compositional changes. This is due to As, P and N being much more volatile than other elements. As such, this possibility needs to be taken into consideration.

Table 2 Reaction product volatilization temperature of the III-V group element under atmospheric pressure

(a)

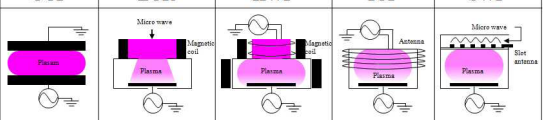
Al	bp/℃	Ga	bp/℃	In	bp/℃
AlF_3	1276	GaF_3	950	InF_3	>1200
$AlCl_3$	180	$GaCl_3$	201	InCl	608
$AlBr_3$	255	$GaBr_3$	279	InBr	656
AlI_3	382	GaI_3	340	InI_3	—
$(CH_3)_3Al$	127	$(CH_3)_3Ga$	56	$(CH_3)_3In$	136

(b)

As	bp/℃	P	bp/℃	N	bp/℃
AsF_3	57	PF_3	-102	NF_3	-129
$AsCl_3$	130	PCl_3	76	NCl_3	71
$AsBr_3$	221	PBr_3	173	NBr_3	—
AsI_3	424	PI_3	227	NI_3	—

*bp : boiling point

Table 3 Characteristics of various plasma sources

Plasma	CCP	ECR	HWP	ICP	SWP
					
Pressure (Pa)	5(10)-100	0.05-0.5(10)	0.05-1(10)	0.1-10	1-100
Frequency (MHz)	13.56-60	915, 2450	5-30	1-50	915, 2450
Electron temperature (eV)	1-5	2-5(10)	5-10	4-5(10)	1-3
Plasma Density (cm^{-3})	~10E+10	10E+11-12	10E+11-13	10E+11-12	10E+10-12

The following explains etching plasma sources. With reference to Table 3, several plasma sources have been proposed. These include: Capacitive Coupled Plasma (CCP), Electron Cyclotron Resonance Plasma (ECR), Helicon Wave Plasma (HWP), Inductively Coupled Plasma (ICP), and Surface Wave Plasma (SWP).

If the sustaining discharge pressure spreads over a wide surface area, the area for processing becomes relatively large. Higher pressure means higher concentration of plasma but this will lead to a shortened mean free path and thus a decrease in the rate of ion injection. The opposite is true for lower pressure. In addition, at lower pressure, it is possible to control the plasma density by adjusting the voltage fed into the plasma source. As the electron temperature is proportionate to the temperature of the wafer, the lower the temperature of the wafer, the easier it is to control the etching process. In addition, since the plasma density is dependent on the plasma source, pressure and frequency, a wider processing area can be achieved through selection of appropriate materials. In addition, RF of stage bias performs ion drawing-in and ion energy control. In basic CCP, the plasma density and ion energy will simultaneously change by controlling the RF power on the stage bias. For this reason, it leads to ion damage. In other structures, the plasma

density and ion energy can be controlled individually and thus it is easy to control damage.

CCP and ICP have simple structures and yet allow for large processing areas. As a result, they are the more commonly used sources recently. ICP is the most widely used source especially in the etching process of optical devices. In order to optimize each process, the inductively super magnetron (ISM) and the Neutral Loop Discharge (NLD) are used as the plasma source system. The NLD plasma source and the ISM plasma source have a general characteristic of specific magnets attached to ICP structure.

3. Etching of III-V Compound Semiconductors

The ISM plasma source is used to etch III-V compound semiconductors as depicted in the schematic in Fig. 5. By aligning magnets around the STAR electrode, even at low pressure and low RF power, it is possible to steadily generate plasma and to cover a wider area of discharge pressure and RF power. This plasma source has an extensive track record of low damage processing.

First, as shown in Fig. 6, in the processing of LD, $SiCl_4$ is commonly used as it forms a byproduct layer ($SiCl_x$) which gives protection to the wall being etched. As a result of this etching characteristic, uniformity in the vertical direction can be achieved. Figure 7 and Fig. 8 show the dependency of the conditions in the processing of an LD using AlGaInP. When the wafer temperature is not high enough for volatilization to occur, the chemical etching characteristic is weak, and the surface will end up rough and tapered. However, by increasing the wafer temperature, uniformity in the vertical direction can be improved, thus avoiding a rough finish on the surface. In addition, the chemical etching characteristic is strong when the amount of Cl-based gas is high compared to alternative gases and Ar reduces the dilution rate. As a result, the footing is large. It is necessary to optimize the wafer temperature and gas ratio in order to determine the rectangularity.

The processing of optical waveguide uses the same process gases as the laser processing. However, when the butt-joint re-growth processing method [1] is introduced after the etching process, Si-based material may barely remain on the surface. In that case, it is possible to select gases such as CH_4 and HI, with exception of $SiCl_4$, to reproduce the effect of sidewall protection. Figure 9 shows an example of the processing in the case of HI as the main gas. When the processing is performed on a mixture of mask pattern sizes, it may lead to a micro-loading effect as shown by "RIE Lag" in the schematic diagram [2]. This effect becomes significant with a strong chemical etching element. However, it is impossible to completely cancel the micro-loading effect even this element is suppressed.

Figure 10 illustrates an example of VCSEL processing. Observe the formation of tapered shapes and smooth surfaces here. There are two methods. One is the method of

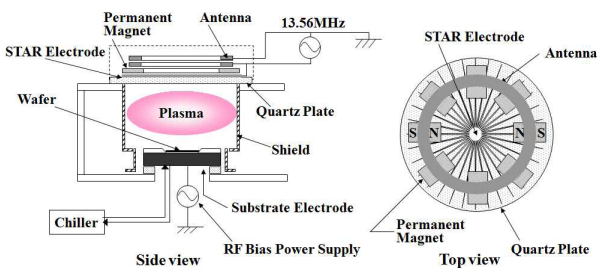


Fig. 5 ISM system schematic

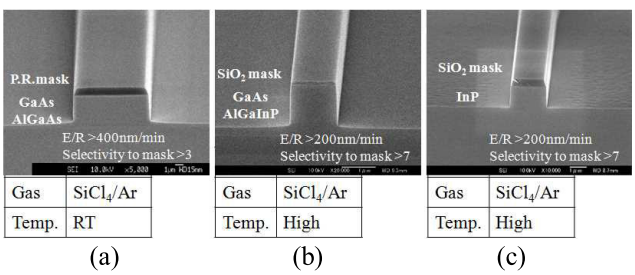


Fig. 6 Etched profile of LD using (a) AlGaAs, (b) AlGaInP, (c) InP

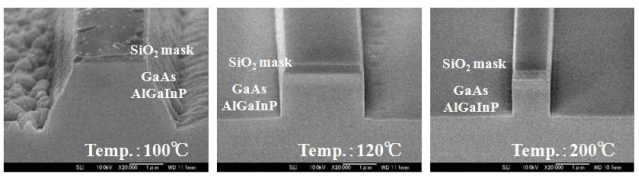


Fig. 7 Temperature dependence of the AlGaInP etching

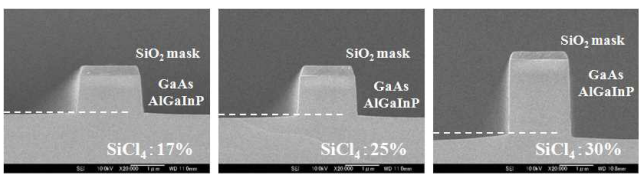


Fig. 8 Gas flow rate ratio dependence of the AlGaInP etching

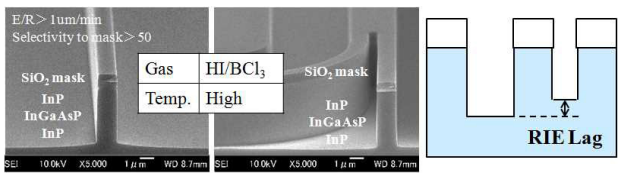


Fig. 9 Etched profile of optical waveguide

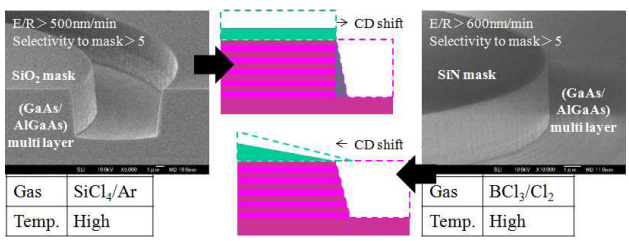


Fig. 10 Etched profile of VCSEL

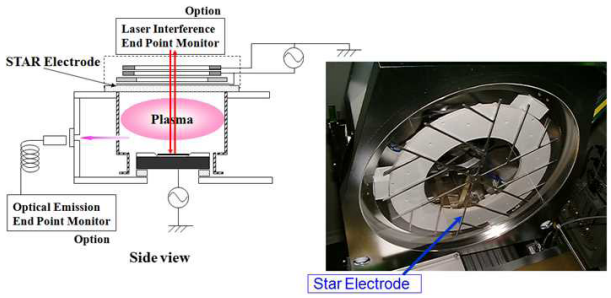


Fig. 11 (a) Setting diagrammatical view of EPM, and (b) image of STAR electrode

obtaining a uniform tapered shape, while gradual suppression of the side etching of each layer, is performed with a sidewall protecting effect. In this way, Critical Dimensional (CD) will be wider. It means etched shape will turn out to be bigger than mask itself. The other is the method of obtaining a tapered shape with a physical etching element while controlling the suppression of the chemical etching element and the differences in etching rate. As a result, etched shape will turn out to be smaller than mask itself. That means CD will be narrower.

On a further note, the depth of the etching can be monitored using an interferometer, which thus makes it possible to control the depth of etching. However, during the process of etching, reaction products will hinder the measurement of the interferometer. The process will also become more stable by keeping the light intensity of the interferometer constant. And in order to achieve constant light intensity, STAR electrode is used as depicted in Fig. 11. For etching of non-volatile metals, ICP plasma is not generated when a conductive film is deposited on the insulator just below the ICP antenna or above the wafer. Thus the STAR electrode was originally developed for the purpose of preventing ICP plasma from not being generated.

Also, in the case of etching an In-based material, which has a relatively high volatilization temperature and fluctuations in the etching rate as shown in Fig. 12, by maintaining the shield temperature at 200 degrees Celsius, the stability of the etching rate can be improved. This is due to the effect of the temperature fluctuations within the chamber.

The following introduces the LED processing. GaN is a material that is difficult to wet etch, making dry etching indispensable. In a typical LED structure with a p-n junction, although p-type layer mesa processing is considered to expose the n-type layer, in some circumstances there is a need for surface control such as Rough-to-Rough, Rough-to-Smooth, and Smooth-to-Rough (Fig. 13) to extract more light. These surface controls can be achieved by adjusting the etching gas ratio. On the other hand, isolation processing of GaN devices uses deep dry etching of approximately 10 um vertically or reverse taper shapes using high wafer temperatures.

In recent LED technology, PSS (Patterned Sapphire Substrate) processing has become another indispensable

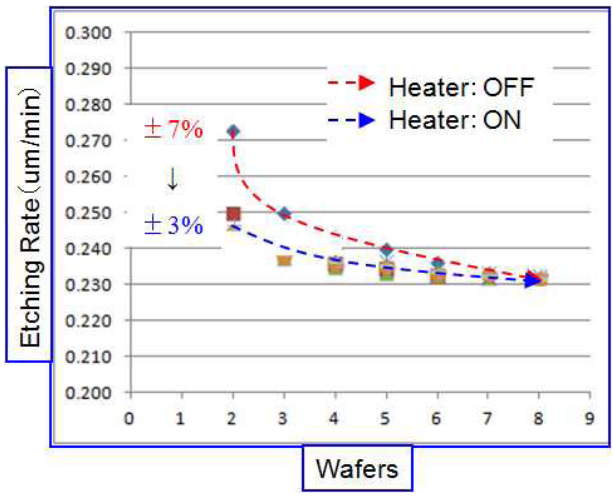


Fig. 12 Repeatability of the etching rate of InP

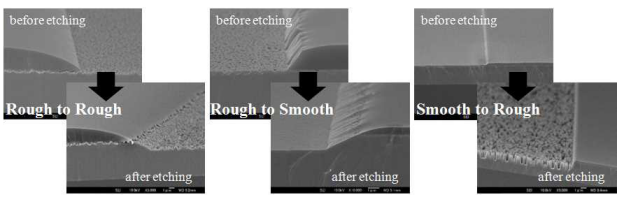


Fig. 13 Etched surface of GaN

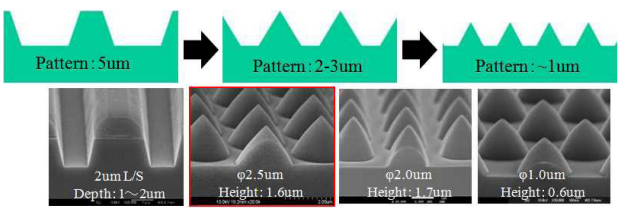


Fig. 14 Etched profiles during PSS processing

processing method. But this processing is not for compound semiconductors. PSS is the processing of the sapphire substrate before GaN epitaxial growth. Initially, the main purpose was to reduce threading dislocation of the epitaxial film [3]. The shape and dimensions of PSS have to be optimized in order to improve LEE (Light Extraction Efficiency) [4]. As shown in Fig. 14, the processed shape and the processed dimensions of PSS has been optimized through maintaining the consistency with the epitaxial technology. As the miniaturization of the dry etching technology had been advanced, optimization of PSS shape can be further improved. Photonic Crystal (PhC) is said to be the most suitable processing structure for LEE. PSS structure utilizes the theory of light scattering in order to achieve total reflection. On the other hand, PhC structure has a photonic band gap for light. For this reason a PhC structure can control the total transmission and total reflection of light emission [5]. However, in the case of using PhC, the pattern size will be on the sub-micron order. In the application of photo-aligner, it is difficult to create PhC patterns

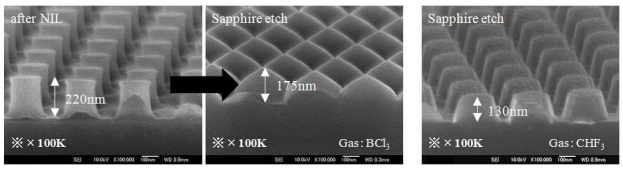


Fig. 15 PhC etching by single layer of nano-imprint resist

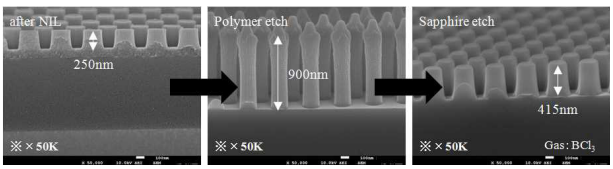


Fig. 16 PhC etching by bilayers of nano-imprint resist

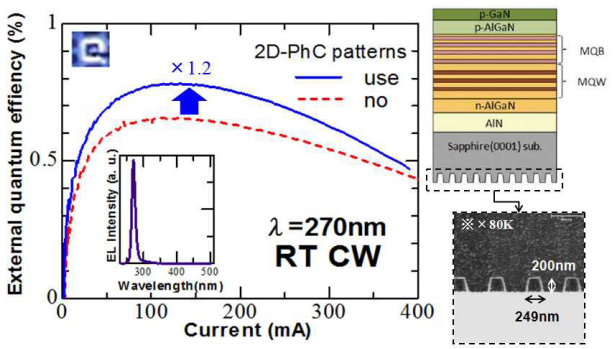


Fig. 17 EQE improvement of DUV-LED by using PhC

using lithography. Also, this method will be expensive as it requires the usage of electron beam lithography. As a result, nano-imprint lithography is a more popular method instead [6], [7]. Nano-imprint resist is weak against plasma as it needs to maintain liquidity and releasability. Hence, high aspect processing of sapphire, which is one of the most difficult materials to etch, is unlikely to be achieved (Fig. 15). It was through collaboration with other players that a high aspect PhC process, which uses bilayer resist method, was developed. Moreover, this process will be further evaluated for its application to LEDs (Fig. 16) [8]. Research of Deep UV-LED (DUV-LED) is being conducted in RIKEN. Figure 17 shows that improvement in the EQE (External Quantum Efficiency) has been achieved [9]. In the future, improvement in the LEE of DUV-LED has been the most important issue, and it is highly likely that forming the technology for PhC will be more crucial than that for blue LEDs.

4. Etching of Glass, LN, LT

As illustrated in Fig. 18, NLD plasma source is used to etch materials such as glass, LN ($LiNbO_3$) and LT ($LiTaO_3$). This plasma source consists of top, middle and bottom coils that are vertically mounted to produce zero magnetic field where plasma is generated. Within this enclosed field, regardless of low pressure or high plasma density, low electron temperature plasma can be generated. In addition, the size of the plasma, which determines the area for etching, can be controlled through the nature of the zero magnetic fields. This relationship is depicted in Fig. 19 [10].

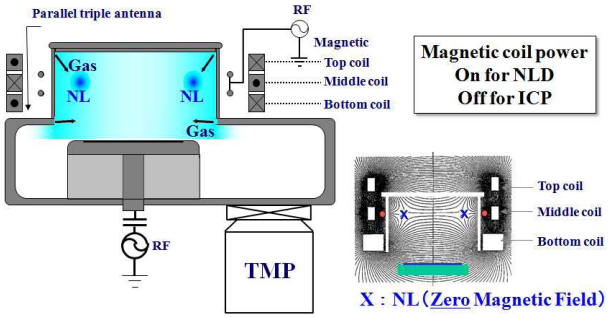


Fig. 18 NLD system schematic

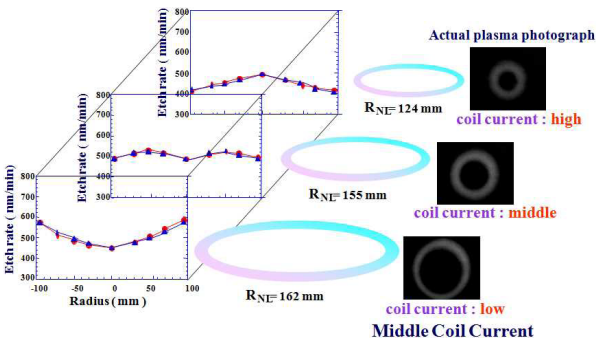


Fig. 19 The effect of plasma diameter on etch rate distribution

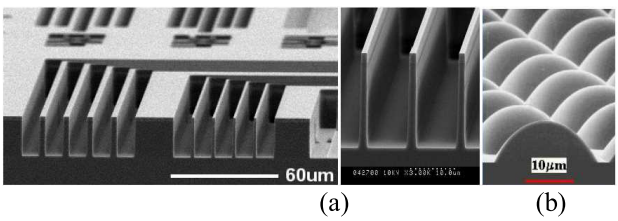


Fig. 20 Etched profiles of (a) optical waveguides using SiO_2, (b) quartz MLA

Figure 20 shows an example of optical waveguide processing and MLA processing of quartz. Optical waveguide processing is a deep etching processing of more than 20 um. It uses a metal mask rather than a resist mask as there is a lack of selectivity. On the other hand, MLA processing uses resist mask formed by a reflow process, and can be transferred and formed through optimal selectivity.

Figure 21 shows an example of optical waveguide processing of LN and LT. It is necessary to pay attention to the pyroelectricity of LN and LT substrates in this processing method. Upon applying high RF power, charge-up of the wafer, chucking errors and wafer cracking are likely to occur and thus the wafer is vacuum-sucked onto the stage as a result. Also, the rapid increase in wafer temperature and the distribution of the wafer temperature generate substrate warpage which leads to chucking errors and wafer cracking.

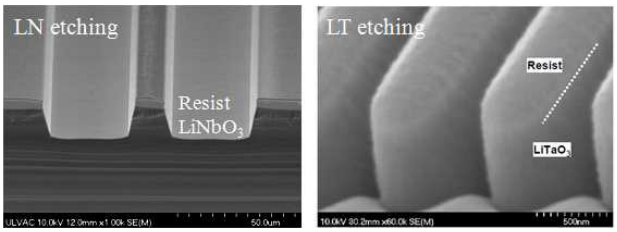


Fig. 21 Etched profiles of optical waveguides using (a) LN, (b) LT

Therefore, specific know-how will be necessary in order to handle this kind of wafer.

5. Conclusions

So far, the LED market is the largest among optical device technologies. With the rapid spread of LED lighting around the world, it is crucial to further lower their cost and to improve mass production. On the other hand, dry etching technology still has room for improvement to achieve high value-added applications in the category of Display, Automotive and DUV-LED. Moreover, it intends to contribute to the construction of a DUV-LED market by improving the properties of DUV-LEDs with PhC.

In the upcoming era of IoT (Internet of Things), handling of large amounts of information will become increasingly significant which leads to the need for more communication devices such as high-frequency transistors. It is expected that high-paced research and development of the technologies for combining different substrates to improve the characteristics of the semiconductors will be crucial as the devices that use the PhC structure will be indispensable in the world of IoT. In addition, with laser lighting and laser displays entering the spotlight, it is necessary to further develop packaging and componential technology for optical devices, especially III-V compound semiconductors.

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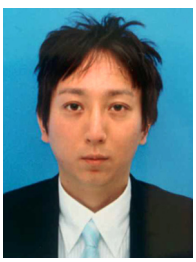

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