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Sub-fF-Capacitance Photonic-Crystal Photodetector Towards fJ/bit On-Chip Receiver

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SUMMARY An ultra-compact InGaAs photodetector (PD) is demonstrated based on a photonic crystal (PhC) waveguide to meet the demand for a photoreceiver for future dense photonic integration. Although the PhC-PD has a length of only 1.7 μm and a capacitance of less than 1 fF, a high responsivity of 1 A/W was observed both theoretically and experimentally. This low capacitance PD allows us to expect a resistor-loaded receiver to be realized that requires no electrical amplifiers. We fabricated a resistor-loaded PhC-PD for light-to-voltage conversion, and demonstrated a kV/W efficiency with a GHz bandwidth without using amplifiers. This will lead to a photoreceiver with an ultralow energy consumption of less than 1 fJ/bit, which is a step along the road to achieving a dense photonic network and processor on a chip.

key words: *photonic crystal waveguide, photodetector, buried heterostructure, optical interconnection*

1. Introduction

A highly integrated chip-scale photonic interconnection and/or a photonic-network-on-chip architecture are demanded for future microprocessors [1]–[3]. As the communication distance decreases and the integration density increases, the size and energy consumption of opto-electronic devices will become a significant issue, and so nanophotonic technologies should be implemented in the system. A photoreceiver will be a critical device because of its large energy consumption. This mainly originates from the need to use a trans-impedance amplifier (TIA) and some voltage amplifiers for a conventional receiver circuit, which incurs an energy cost of hundred fJ/bit and requires an area of more than 10^4 μm^2 [4]–[6]. Therefore, this will constitute a significant bottleneck when implemented for dense on-chip communication [7]. One solution is to realize ultrasmall-capacitance photodetectors (PDs) and thus allow connection to a high impedance receiver circuit while maintaining a large resistance-capacitance (RC) bandwidth. This would lead to a reduction in electrical amplification or even its elimination (known as a receiver-less PD [5], [7], [8]), which promises an ultralow-energy on-chip photoreceiver.

Photonic crystals (PhCs) are promising for creating an ultrasmall PD because of their strong light confinement. We have been studying such a PhC-PD with a compact InGaAs absorber embedded in an InP-based PhC waveguide, which we fabricated using a buried-heterostructure (BH) formation technique [9]–[11]. This compact BH with a PhC waveguide can confine both photons and carriers in an ultrasmall space to achieve both high optical responsivity and ultrasmall device capacitance thus making it desirable in terms of meeting the demand for an amplifier-less photoreceiver.

In this paper, we describe an InGaAs-embedded PhC-PD where the absorber length was reduced to only 1.7 μm and the device capacitance was less than 1 fF. The size is still sufficient to obtain a high responsivity of 1 A/W and a clear eye opening for a 40-Gbit/s signal. Furthermore, we fabricated a PhC-PD integrated with a several-kΩ load resistor to demonstrate on-chip light-to-voltage conversion. We employed an electro-optic (EO) probe to measure the voltage generation in the PhC-PDs, which revealed a conversion efficiency of as high as 4 kV/W. The expected bandwidth after removing the parasitic wiring elements exceeds 10 GHz [10]. This suggests that the optical energy required for generating a CMOS voltage level is less than 1 fJ/bit, which can be obtained without electrical amplification and therefore dominates the total energy consumption. These results reveal a successful way of realizing an ultrasmall/ultralow-energy photoreceiver that can be densely integrated on a chip.

2. Requirement for Resistor-Loaded Photoreceiver

To discuss the required capacitance of a PD used for configuring a resistor-loaded photoreceiver, we considered the simple PD-resistor circuit shown in Fig. 1 (a). This consists of PD capacitance C_j, PD series resistance R_s, load resistance R_{load}, and front-end capacitance (including parasitic capacitances) C_p. The output voltage V_{out} for the photocurrent I_{pd} is given by

$$V_{out} = \frac{R_{load} I_{PD}}{1 - R_{load} R_s C_j C_p \omega^2 + j\omega \left[R_{load} \left(C_j + C_p \right) + R_s C_j \right]} \quad (1)$$

For a low frequency response, $V_{out} = R_{load} I_{PD}$, which leads to a transimpedance gain of $V_{out}/I_{PD} = R_{load}$. The light-to-voltage conversion efficiency would be $\eta_{LV} = V_{out}/P_{opt} = \eta_{pd} R_{load}$ [V/W], where η_{pd} [A/W] is optical responsivity. On

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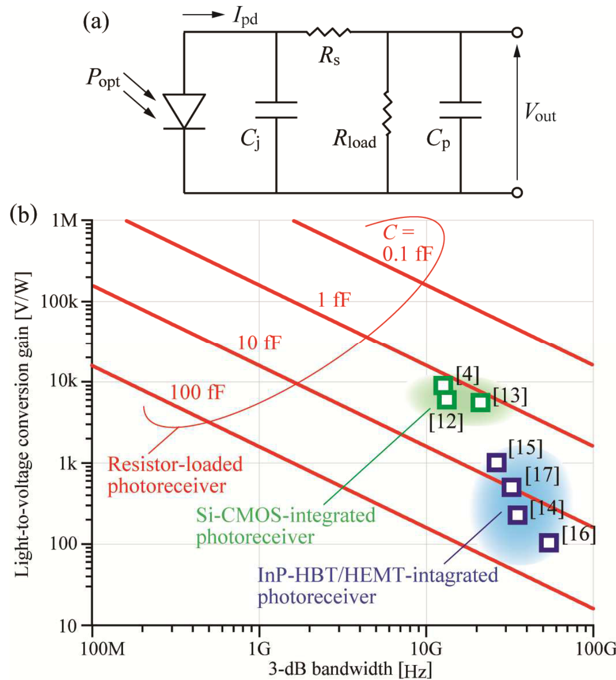

Fig. 1 Theoretical required capacitance for a resistor-loaded PD. (a) Equivalent circuit of the resistor-loaded PD. (b) Calculated light-to-voltage conversion efficiency and 3-dB bandwidth (red lines). The total capacitance is changed as a parameter. The reported values for the Si-CMOS integrated photoreceivers (green plots) and the InP-HBT/HEMT-integrated photoreceivers (blue plots) are also plotted.

the other hand, the RC bandwidth f_{RC} can be obtained by setting the magnitude of the denominator of Eq. (1) at $\sqrt{2}$. Roughly speaking, the second term of the denominator is negligible below the 3-dB bandwidth, and R_s is assumed to be much lower thanR_{load}. As a result, f_{RC} is given by

$$f_{RC} \approx \frac{1}{2\pi R_{load}\left(C_j + C_p\right)} \tag{2}$$

Figure 1 (b) shows the calculated light-to-voltage conversion efficiency and the corresponding 3-dB bandwidth. Bandwidth limit due to the carrier transit time is not included in this calculation. The total capacitance $C = C_j + C_p$ is changed as a parameter, which clearly determines the efficiency-bandwidth product (EBP) as given by $\eta_{LV} f_{RC} = \eta_{pd}(2\pi C)^{-1}$. We assume an optical responsivity $\eta_{pd} = 1$ A/W, which is actually obtained in the experiment. Figure 1 (b) also includes plots for reported Ge-based photoreceivers integrated with a Si-CMOS TIA/Limiting amplifier (LA) circuit [4], [12], [13] and InGaAs-based photoreceivers integrated with an InP-based heterojunction bipolar transistor (HBT)/high electron mobility transistor (HEMT) circuit [14]–[17]. These receivers support a high conversion efficiency and large bandwidth thanks to the integrated amplifiers. However, it should be noted that such amplifiers also consume a huge amount of electric power (several mW) [5], [6], and this dominates the overall power consumption. To exceed these conventional receivers with resistor-loaded receiver in terms of EBP, C should be lower than 1 fF. Recent Ge-waveguide PDs have exhibited a capacitance of 4–5 fF [18], [19], which does not meet this requirement.

A low-capacitance resistor-loaded receiver also has the advantage on the signal-to-noise ratio because of its high resistance and consequent low thermal noise even at a GHz range. For the amplifier-integrated receiver, the amplifier noise generally limits the lowest optical power required for the error-free operation. For the resistor-loaded receiver, on the other hand, the required voltage at the front end basically determines the optical power. At this situation, the noise level is enough low for the error-free operation [10].

To these purposes, we need to focus on reducing the PD capacitance to achieve a resistor-loaded receiver that offers sufficiently high performance without the need for any signal amplifiers.

3. Ultra-Small Capacitance Photonic-Crystal PD

3.1 Device Structure and Capacitance

We have employed the combination of a PhC waveguide and cavity and an ultrasmall BH to demonstrate optical nanodevices such as nanolasers and all-optical memories [9], [11], which exhibited a record low power consumption. This structure can be employed for PDs by embedding a compact InGaAs absorber, thereby reducing the device capacitance by miniaturization. Figure 2 (a) shows a schematic of our PhC-PD. The device consists of an InP PhC waveguide, a BH for embedding the InGaAs, and a lateral p-i-n junction [20]. The inset shows the fundamental waveguide mode profile, which was simulated with the finite-element method (FEM). The lattice constant a and the air-hole diameter $2r$ were 420 and 200 nm, respectively ($2r/a = 0.476$). The InP slab and the InGaAs absorber were 250 and 150 nm thick, respectively, and the InGaAs was 350 nm wide. The waveguide width was set at 0.95 W_0, where W_0 is the basic line defect width defined as the removal of one row of air holes (W1 waveguide). The optical confinement factor (Γ) in the embedded InGaAs absorber is given by

$$\int_{absorber} \varepsilon |E|^2 d\mathbf{r} \Big/ \int_{All} \varepsilon |E|^2 d\mathbf{r} \tag{3}$$

The propagation mode is concentrated in the waveguide core region at $a/\lambda = 0.28$, thus resulting in a Γ of as high as 0.5. The group index n_g at this wavelength is 5. The PhC waveguide also has a large n_g (slow light), which can lead to absorption enhancement. However, the slow-light waveguide needs an optimized coupler to prevent any significant optical reflection, and this is a topic for future study. As shown in this paper, the normal n_g value (= 5) still has good capability for achieving an ultrashort PD.

The small dimensions of the absorber and the p-i-n junction mean that the device capacitance should be reduced to the fF level, as shown in Fig. 2 (b). The parallel-plate capacitance (= $\varepsilon_0 \varepsilon_{InGaAs} L_{abs} T_j / d_j$) is less than 0.2 fF for an absorber length $L_{abs} < 3\,\mu$m. However, for an ultrasmall

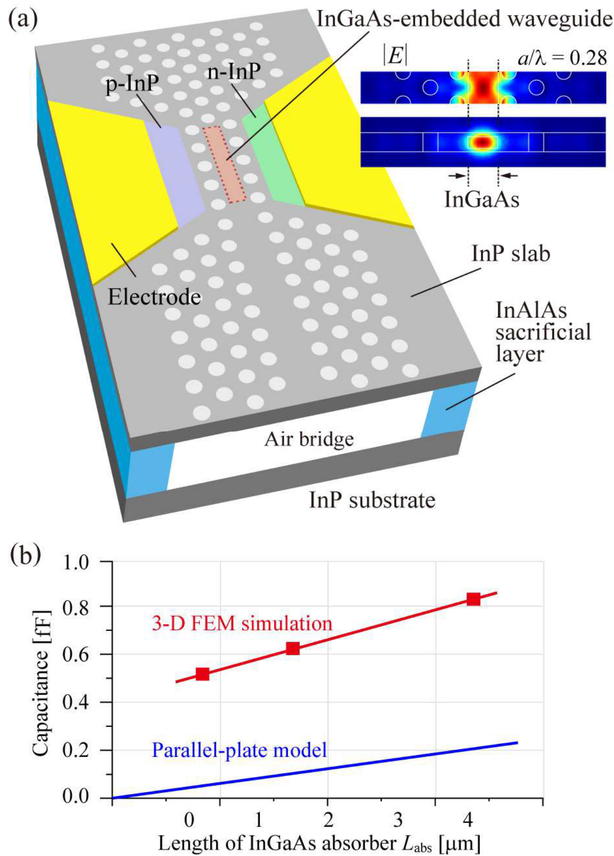

Fig. 2 PhC-PD structure and capacitance. (a) Schematic of PhC-PD. The inset is the calculated mode profile of the fundamental mode. (b) Calculated capacitance of PhC-PD. The blue curve is calculated from the parallel-plate model. The red plots are the results simulated by FEM with a 3-D model.

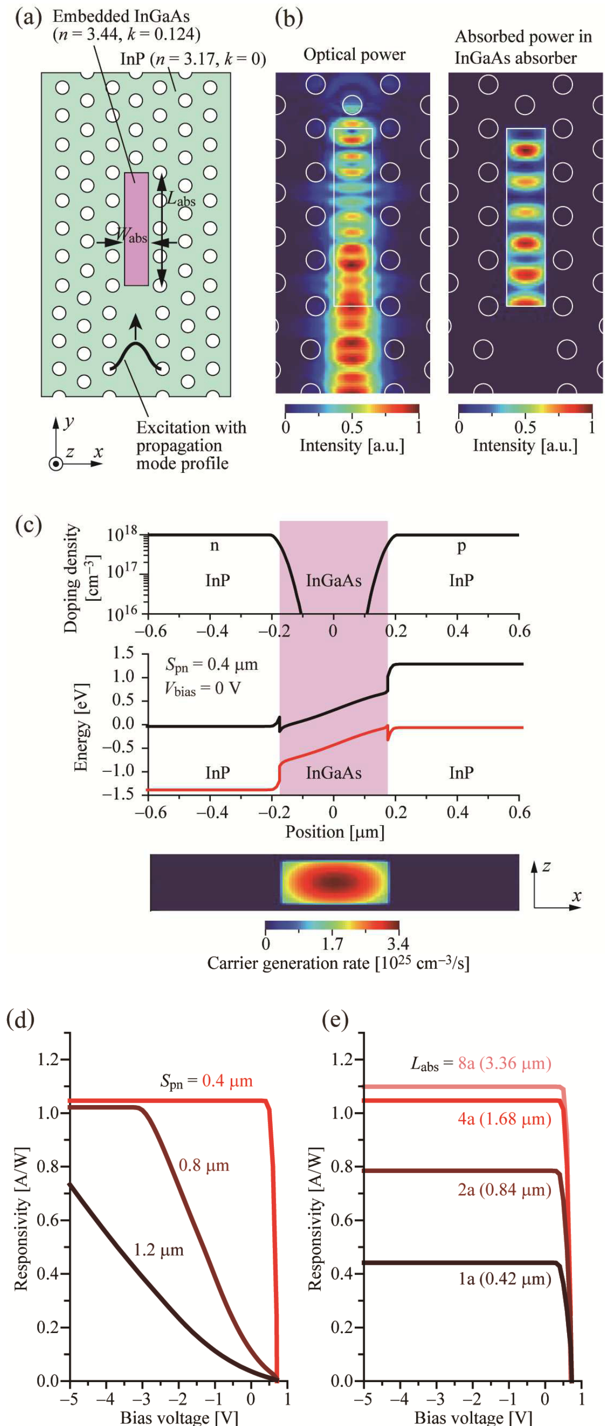

Fig. 3 Calculated responsivity of PhC-PD. (a) Calculation model for $L_{abs} = 4a$ (1.68 μm) and W_{abs} = 350 nm. (b) Propagated light power profile (left) and absorbed power profile (right). (c) Doping profile (top), energy band diagram (middle), and carrier generation rate profile for incident optical power of 1 μW. (d) Calculated responsivity for different p/n separations S_{pn}. $L_{abs} = 4a$ is fixed. (e) Calculated responsivity for different L_{abs}. S_{pn} = 0.4 μm is fixed.

junction, the fringing field contribution of the junction also becomes significant, and hence it is important to include the fringe capacitance [21]. This contribution was simulated by the FEM with a full 3-D model excluding the large electrical pads, and the total capacitance exceeded that of the parallel plate model. The total capacitance of our PhC-PD is still < 1 fF, which is smaller than our target given the goal of realizing a resistor-loaded receiver, as discussed in the Sect. 2.

3.2 Responsivity Calculation

We simulated the optical responsivity for this PhC-PD using the commercial software (Lumerical [22]). A 3-D finite-difference time domain (FDTD) solver was used to simulate the light propagation and absorption, while an FEM-based carrier transport solver was used to calculate the responsivity. Figure 3 (a) shows the simulation model, consisting of an InP PhC and an embedded InGaAs absorber. An absorber length L_{abs} of 4a, and an absorption coefficient of 10^4 cm^{-1} (imaginary part of index $k = 0.124$) were assumed. Other parameters are the same as in Fig. 2 (a). Because of the index difference between the InP PhC waveguide and the InGaAs-embedded waveguide, their widths were adjusted so that their guiding bands matched. To this end, the widths of the InP and InGaAs-embedded regions were changed to 1.1 W_0 and 0.95 W_0, respectively. Excited light with the shape of the fundamental mode was introduced at the in-

put waveguide to be forwarded to the absorber. Figure 3 (b) shows the power profiles of the propagated and absorbed light. We confirmed that most of the light was absorbed after a single roundtrip in the absorber, resulting in an absorption efficiency of 85%.

Figure 3 (c) shows the cross-sectional doping profile and the corresponding energy band diagram that we used for the carrier transport simulation. The doping levels for both the p and n layers were 10^{18} cm^{-3} and the separation between them was S_{pn} = 0.4 μm. The light absorption profile in Fig. 3 (b) gives the carrier generation rate when the incident light power was set at 1 μW in this calculation. To avoid a long calculation time, a 2-D carrier transport simulation was carried out, for which the optical absorption profile was averaged in the y direction and thus the carrier generation rate profile on the x-z axis was obtained as shown in Fig. 3 (c). Figure 3 (d) shows the calculated responsivity for the bias voltage when S_{pn} was changed. When S_{pn} = 0.4 μm, which matches the absorber width, a flat responsivity of 1.02 A/W was calculated for the entire reverse voltage range. Increases in S_{pn} make the static electric field weaker, resulting in carrier accumulation and poor carrier extraction compared with carrier recombination (a lifetime of 10 ns in this calculation). This suggested that the PhC-PD would maintain a high responsivity thanks to the narrow optical confinement and subsequent local absorption. On the other hand, Fig. 3 (d) shows the responsivities for different absorber lengths L_{abs} where S_{pn} = 0.4 μm is fixed. A responsivity of >1 A/W is expected for $L_{abs} \geq 4a$ (1.68 μm). A decrease in L_{abs} degrades the absorption efficiency, but still maintains >0.5 A/W for $L_{abs} \leq 2a$ (0.84 μm). As well as the capacitance simulation, these results clearly promise the highly-efficient ultrasmall PD towards configuring an amplifier-less receiver.

4. Fabrication and Measurement of PhC PD

4.1 Device Preparation

For device fabrication, we employed the same process for combining a PhC waveguide and an ultrasmall BH as used that used for PhC nanolasers and all-optical memories [9], [11]. An ultra-small InGaAs absorber layer, which was lattice matched to InP, was embedded in a line-defect PhC waveguide using butt-joint techniques. Figure 4 (a) shows a SEM image of the PhC PD, revealing a flat surface resulting from the successful butt-joint regrowth. PhC air holes were formed by electron-beam lithography and Cl_2-based dry etching. A lateral p-i-n junction was formed by employing Zn diffusion and Si ion implantation for the p- and n-type doping, respectively. After metallization, a sacrificial layer was etched to form an air-bridge structure. As mentioned later, InGaAs or InAlAs was employed for the sacrificial layer, and the latter can work to reduce the dark current in operation.

We measured the device characteristics by employing a wavelength-tunable laser light, as shown in Fig. 4 (a). The

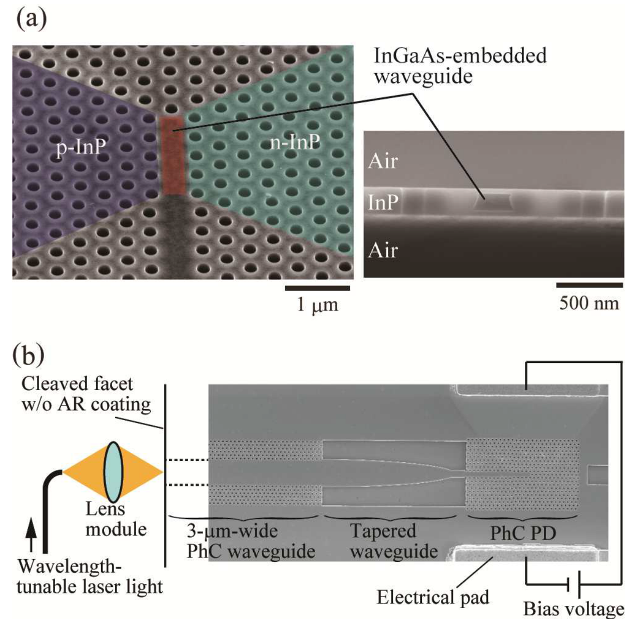

Fig. 4 Fabricated sample and measurement setup. (a) SEM images of top and cross-section. (b) Measurement setup and input waveguides for injecting light into the PD.

light was injected into the InP PhC waveguide from the fiber via a lens module, a 3-μm-wide PhC waveguide, and a tapered waveguide. In the measurement, a fiber polarization controller was used to tune the input light to TE polarization. The total coupling loss from the fiber to the input PhC waveguide was 11 dB, which was used to estimate the on-chip power.

4.2 Static Responses

The photocurrent (I) was measured for a different bias voltage (V) and CW optical power. For the first trial device fabrication, an InGaAs sacrificial layer was employed. As shown in Fig. 5 (a), the dark currents were approximately 3 and 40 nA when the reverse bias voltages were set at −2 and −4 V, respectively. This originated from the leakage current that passed through the InGaAs sacrificial layer and the surface of the InP buffer layer, despite the formation of an air-bridge structure. To solve this, the sacrificial layer was changed to InAlAs, which has a large bandgap energy, and an Fe-doped InP buffer layer was employed to form the semi-insulating surface. As a result, the dark current in the same voltage range fell to less than 100 pA, as shown in Fig. 5 (b).

Figure 5 (c) shows photocurrent as a function of optical input power at a bias voltage of −2 V for a device with an InAlAs sacrificial layer. We successfully estimated a large optical responsivity of 0.98 A/W even for L_{abs} = 1.7 μm. Specifically, our BH formation does not increase the non-radiative carrier recombination loss thanks to the successful butt-joint epitaxial growth. In fact, a carrier lifetime of 7 ns has been confirmed for our BH structure [11], and this would

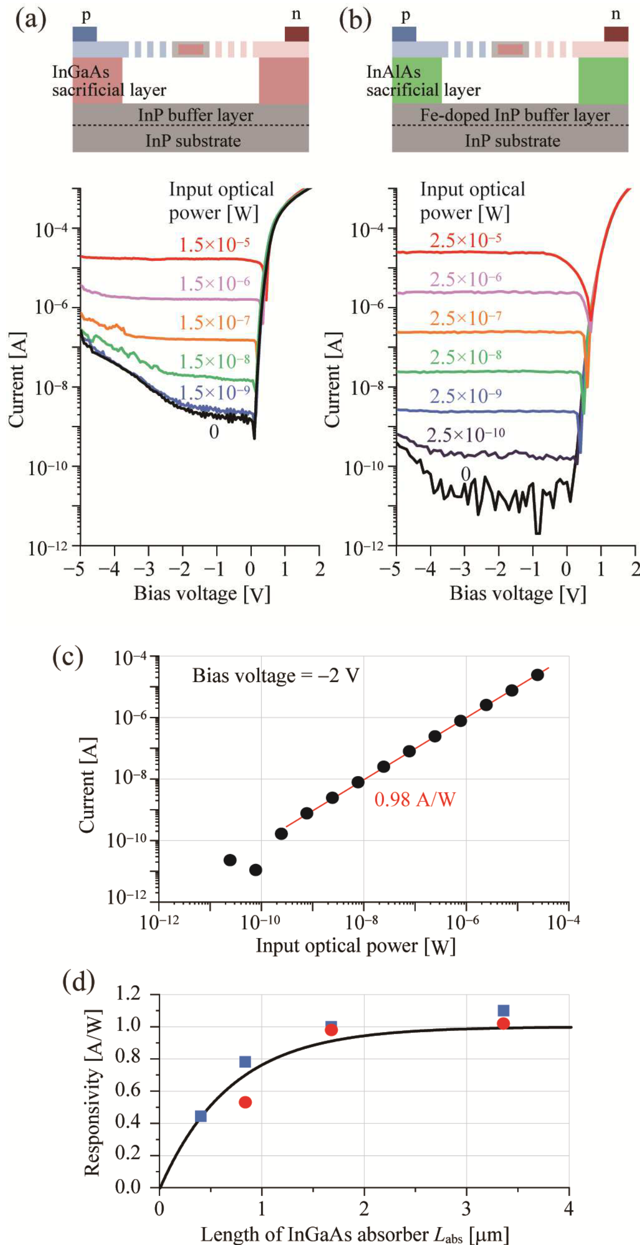

Fig. 5 Static responses for CW light input. (a) DC photocurrent versus bias voltage characteristics for PD with InGaAs sacrificial layer. (b) PD with InAlAs sacrificial layer. The absorber length is $L_{\mathrm{abs}} = 1.7\,\mu$m for both (a) and (b). The light wavelength is 1536.7 nm. (c) Photocurrent versus optical power characteristics for PD with InAlAs sacrificial layer. Inset shows the photocurrent spectrum for the optical power of 10 μW. (d) DC responsivity versus L_{abs} characteristics. Experimental results (red circles), simulated results of Fig. 3 (e) (blue squares), and theoretical curve of Eq. (3) (black curve) are shown.

be long enough to prevent carrier loss during a fast carrier extraction. The inset of Fig. 5 (c) shows the photocurrent spectrum, which shows that the high and flat responsivity of more than 50 nm (1490–1540 nm) was observed.

The photocurrent was reduced when the absorber length became short, as summarized in Fig. 5 (d). The theoretical responsivity η_{PD} for a single roundtrip of light in the

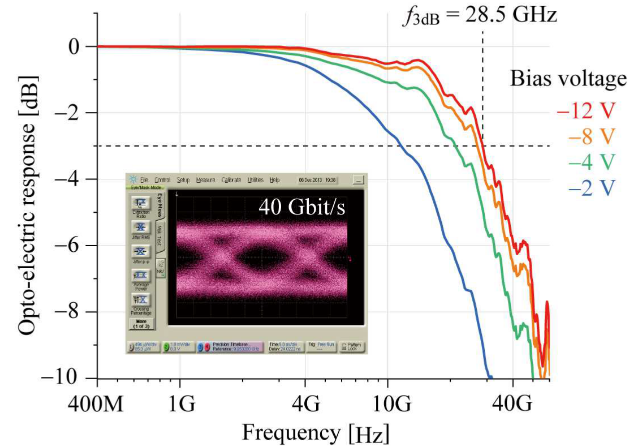

Fig. 6 Small signal responses for different reverse-bias voltages. Inset shows the eye diagram for 40 Gbit/s NRZ optical signals. The input wavelength was 1536.7 nm and the optical peak power was 100 μW.

absorber is given by

$$\eta_{\mathrm{PD}} = \eta_{\mathrm{eff}} \cdot \frac{e}{h\nu} \cdot \left\{1 - \exp\left(-2\frac{n_{\mathrm{g}}}{n}\alpha_{\mathrm{abs}}\Gamma L_{\mathrm{abs}}\right)\right\} \qquad (4)$$

where e is the electron charge, h is the Planck constant, ν is the frequency of light, n is the material index, n_{g} is the group index, α_{abs} is the absorption constant of InGaAs, Γ is the optical confinement factor, and L_{abs} is the absorber length. η_{eff} is a loss factor that includes the losses for both light and the photo-generated carrier. Figure 5 (d) includes the theoretical curves given by Eq. (4), in which we adopted the simulated values of $\Gamma = 0.5$ and $n_{\mathrm{g}} = 5$, and assumed parameters of $\alpha_{\mathrm{abs}} = 10^4\,\mathrm{cm}^{-1}$, $n = 3.4$, and $\eta_{\mathrm{eff}} = 0.8$. The theoretical curve is a good fit with the experimental plots and the simulation results estimated from Fig. 3 (e). We confirmed that the shortest length with which to maintain a high responsivity close to 1 A/W was $L_{\mathrm{abs}} = 1.7\,\mu$m.

4.3 Dynamic Responses

We investigated the dynamic performance of our PD by injecting an intensity-modulated optical signal under a reverse bias through a bias tee thereby extracting an RF signal. Figure 6 shows the operation dynamics of our PD, into which we injected an intensity-modulated optical signal with a peak power of 100 μW. At the low frequency region (<1 GHz), the bias voltage as low as −2 V works for the high responsivity, which suggests that the carrier drift is sufficiently faster than the carrier recombination. The maximum 3-dB bandwidth was 28.5 GHz when the bias voltage was −12 V, which reveals the capability for a bit rate of around 50 Gbit/s for a non-return-to-zero (NRZ) signal. Actually, the clear eye opening was observed for 40-Gbit/s NRZ signals generated with a $2^{31} - 1$ pseudo-random bit sequence, as shown in the inset of Fig. 6. The high bias voltage (−12 V) required for the high frequency region is probably caused from the wider depletion region than we expected. The wide depletion region degrades the internal

electric field, and therefore the bias voltage should be increased to maintain the fast carrier extraction. This bias voltage will be reduced by optimizing the separation between p and n region, as suggested in the simulation of Fig. 3 (d).

5. Resistor-Loaded PhC PD

5.1 Device Preparation and Electro-Optic Probing Setup

The ultrasmall capacitance of our PD enables us to connect it with a high load resistance without the need for amplifiers to convert photocurrent to voltage while maintaining a large RC bandwidth. However, there has been no report evaluating the on-chip light-to-voltage conversion dynamics of resistor-loaded nano-PDs. The experimental difficulty is that a conventional measurement using an oscilloscope/network analyzer with an additional electrical pad would hinder correct device evaluation, because in most cases their impedances are lower than the device load of 50 Ω. This makes it difficult to measure the voltage across the load. (Note that direct connection with a high-impedance CMOS gate would be available for a photoreceiver in an on-chip-communication application.) In our measurement, we employed an electro-optic (EO) probing technique [23]. When we prepared the sample for EO probing, our PhC-PD was connected to a load resistor R_{load} with a gold strip line with a length L_{strip}, as shown in Fig. 7 (a).

The experimental setup for EO probing is shown in Fig. 7 (b). Sinusoidal modulated light (50 MHz) was injected into the PhC-PD. Photocurrent flows into the load resistor, and generates a modulated electric field (proportional to the voltage) between the strip lines. An EO probe consisting of an optical fiber with an EO crystal (ZnTe) was brought towards the strip line. CW light ($\lambda = 1.55\ \mu$m) was separately injected into the EO probe and sensed the modulated electric field via the EO crystal. By combining a polarization beam splitter and a balanced photoreceiver, the polarization change of the CW light was detected as an EO probing voltage. Before the device measurement, the EO probing voltage for AC voltage applied to the strip line was acquired to obtain the correspondence between the two voltages. To this end, a sinusoidal voltage signal from a function generator was directly applied to the reference strip line and the EO-probing voltage was detected at the mid-point between the strip lines. As shown in Fig. 7 (c), we observed a clear proportional relationship with the minimum observable voltage across the strip line of 40 mV. Thereafter, we replaced the reference with a PhC-PD sample to evaluate the photo-generated voltage.

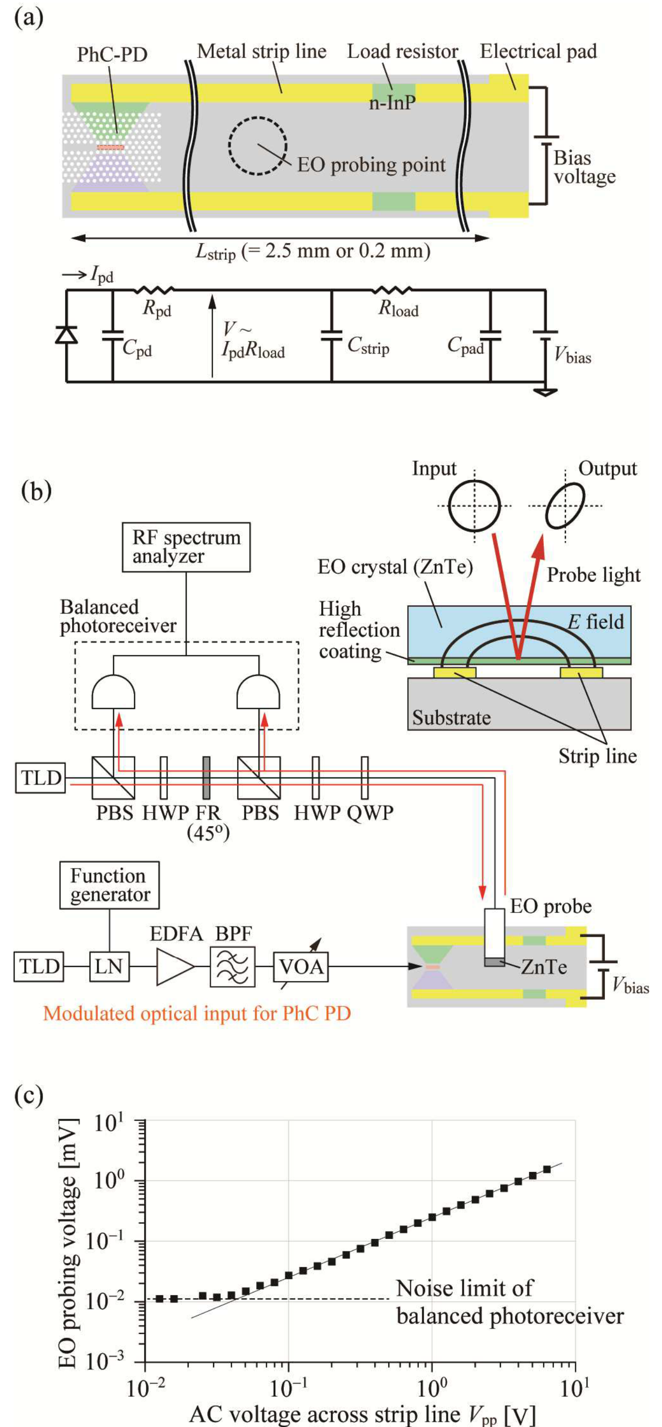

Fig. 7 Resistor-loaded PhC-PD and EO probing measurement setup. (a) Schematic of sample (top) and corresponding equivalent circuit (bottom). (b) Experimental setup for EO probing measurement. (TLD: Tunable laser diode, LN: Lithium-niobate modulator, EDFA: Erbium-doped fiber amplifier, BPF: Band-pass filter, VOA: Variable optical attenuator, PBS: Polarization beam splitter, HWP: Half-wave plate, QWP: Quarter-wave plate, FR: Faraday rotator) (c) EO probing voltage for AC voltage applied to the reference strip line.

5.2 Demonstration of Light-to-Voltage Conversion

Figure 8 (a) shows the light-to-voltage conversion efficiency η_{LV} for PDs with different R_{load} values. The generated AC voltage V_{pp} clearly increased as R_{load} became larger. A maximum $\eta_{\mathrm{LV}} = 3.95$ kV/W was achieved for $R_{\mathrm{load}} = 8.8$ kΩ.

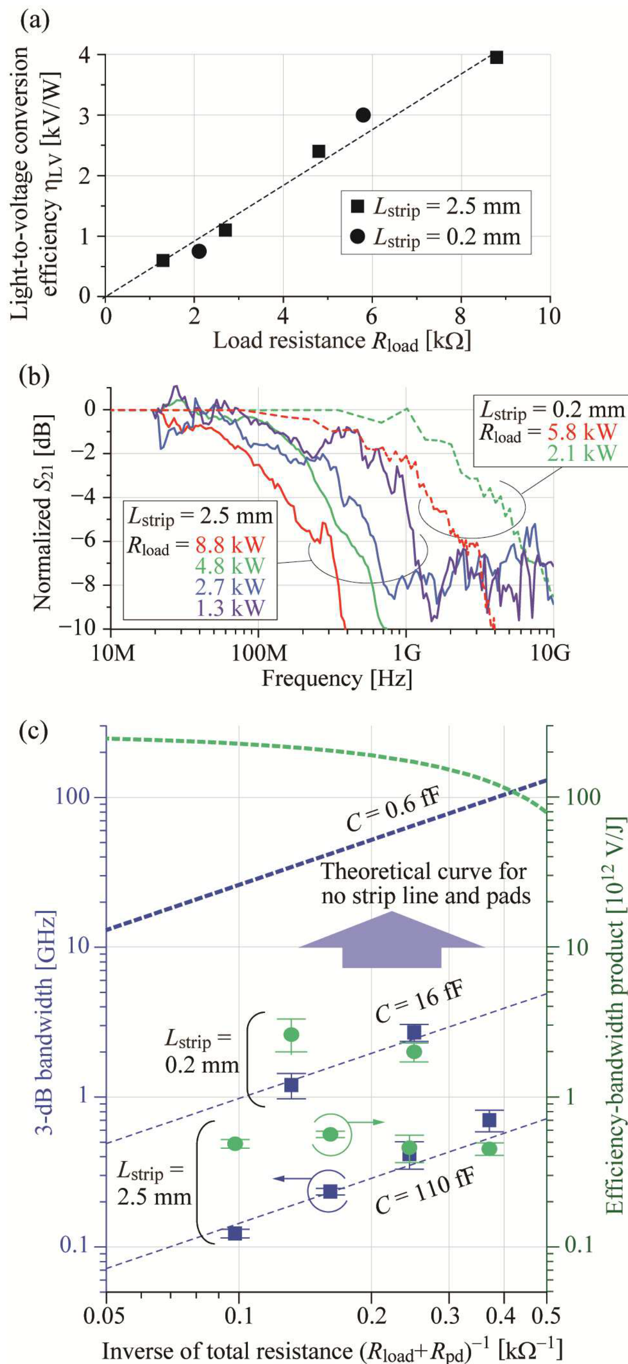

Fig. 8 Measurement results for voltage generation in resistor-loaded PhC-PD. (a) Light-to-voltage conversion efficiency for different load resistances R_{load}. Square and circle plots show results for L_{strip} values of 2.5 and 0.2 mm, respectively. (b) Small-signal responses for different load resistances R_{load} and strip line lengths L_{strip}. (c) 3-dB bandwidth (square plots for left axis) and efficiency-bandwidth product (circle plots for right axis). The plots show the experimental results, and the dashed curves show the calculated results considering both the PD junction capacitance and the parasitic capacitances. The bold dashed curves are calculated under the assumption of no parasitic capacitances.

These results show that an optical power of 50 μW can generate the V_{pp} of 200 mV that is required for a CMOS inverter [5]. On the other hand, the operation bandwidth is limited by RC, although a gold strip line and a pad with a much larger capacitance than the PhC-PD were included in our sample because they were necessary for EO probing. Figure 8 (a) shows the frequency responses for different R_{load} values, in which samples with different L_{strip} values of 2.5 and 0.2 mm were evaluated. The smaller R_{load} and L_{strip}, which resulted in a shorter RC time, appear to increase the bandwidth. The RC-limited bandwidth for L_{strip} = 2.5 mm was estimated from f_{RC} = 120–750 MHz for R_{load} values of 1.3–8.8 kΩ, while that for L_{strip} = 0.2 mm increased to f_{RC} = 1.2–2.7 GHz. Figure 8 (c) summarizes the 3-dB bandwidth (blue plots for the left vertical axis) as a function of $1/(R_{load} + R_{pd})$. These plots have a linear relation as they are mainly determined by $f_{RC} = [2\pi(R_{pd} + R_{load})C]^{-1}$, where C consists of both the PhC-PD capacitance and the parasitic capacitance caused by the strip line and pads. The dashed lines are the theoretical curves obtained by assuming C = 16 and 110 fF, which are dominated by parasites, and the fit well with the experimental plots.

Another figure we evaluated was the product of η_{LV} and f_{RC}, which are in a trade-off relationship, because they are proportional to R_{load} and $(R_{pd} + R_{load})^{-1}$, respectively. This efficiency-bandwidth product (EBP) [V/W·Hz] (= [V/J]) can indicate the optical energy needed to generate the required voltage, regardless of the bit rate of the optical signal. The EBPs are denoted by green plots on the right vertical axis in Fig. 8 (d). A shorter L_{strip} enhances the EBP because f_{RC} increases while η_{LV} remains constant (See Fig. 8 (a)). The EBP values were in the 4–5 × 10^{11} and 2–3 × 10^{12} V/J ranges for L_{strip} = 2.5 and 0.2 mm, respectively. As a result, they can be translated to the required optical energies of 200 and 33 fJ/bit for L_{strip} = 2.5 and 0.2 mm, respectively, to obtain V_{pp} = 200 mV with an NRZ optical signal. We also theoretically discuss an ideal case where there is no parasitic capacitance. The bold dashed curves in Fig. 8 (d) denote f_{RC} and EBP in an ideal situation calculated by assuming only a PD junction capacitance of C = 0.6 fF. This makes the bandwidth higher than 10 GHz, which should be practically acceptable. Subsequently, the expected EBP exceeds 10^{14} V/J, corresponding to a required optical energy of less than 1 fJ/bit. These performances promise to surpass the performance of a conventional PD-TIA circuit. Such a situation can be realized by removing the strip line and pads used in the experiment, because they were simply needed for the EO-probing measurement. Our experimental and theoretical results for an ultrasmall PhC-PD have revealed the feasibility of an amplifier-less photoreceiver on a chip with a practically acceptable size, efficiency, bandwidth, and power consumption.

6. Conclusions

Ultralow capacitance PDs offer the opportunity to configure a resistor-loaded photoreceiver that does not require an

amplifier. To this end, we employed a PhC nanostructure in which we embedded a small InGaAs absorber, which allowed us to reduce the detector length to just 1.7 μm while demonstrating a high responsivity of 1 A/W and eye opening for a 40 Gbit/s signal. The theoretical device capacitance fell to less than 1 fF. We fabricated a resistor-loaded PhC-PD, and successfully demonstrated light-to-voltage conversion with an efficiency of up to 4 kV/W, which is comparable to recently available TIA-integrated photoreceivers. The GHz level operation bandwidth was also evaluated, and it would be enhanced simply by removing the parasitic elements and thus increasing the RC bandwidth above 10 GHz. These demonstrations clearly revealed a promising way of realizing a photoreceiver that operates with an optical energy of less than 1 fJ/bit without any amplifier energy. Such a receiver will enable us to develop a photonic network on chip architecture with an unprecedentedly high density.

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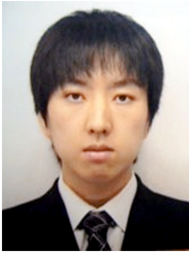
References

[1] M. Notomi, K. Nozaki, A. Shinya, S. Matsuo, and E. Kuramochi, "Toward fJ/bit optical communication in a chip," Optics Communications, vol.314, pp.3–17, 2014.
[2] C. Sun, M.T. Wade, Y. Lee, J.S. Orcutt, L. Alloatti, M.S. Georgas, A.S. Waterman, J.M. Shainline, R.R. Avizienis, S. Lin, B.R. Moss, R. Kumar, F. Pavanello, A.H. Atabaki, H.M. Cook, A.J. Ou, J.C. Leu, Y.-H. Chen, K. Asanović, R.J. Ram, M.A. Popović, and V.M. Stojanović, "Single-chip microprocessor that communicates directly using light," Nature, vol.528, no.7583, pp.534–538, 2015.
[3] Y.A. Vlasov, "Silicon CMOS-Integrated Nano-Photonics for Computer and Data Communications Beyond 100G," IEEE Commun. Mag., vol.50, no.2, pp.S67–S72, 2012.
[4] D. Okamoto, Y. Suzuki, K. Yashiki, Y. Hagihara, M. Tokushima, J. Fujikata, M. Kurihara, J. Tsuchida, T. Nedachi, J. Inasaka, and K. Kurata, "A 25-Gb/s 5 x 5 mm(2) Chip-Scale Silicon-Photonic Receiver Integrated With 28-nm CMOS Transimpedance Amplifier," J. Lightwave. Technol., vol.34, no.12, pp.2988–2995, 2016.
[5] S. Assefa, F.N. Xia, W.M.J. Green, C.L. Schow, A.V. Rylyakov, and Y.A. Vlasov, "CMOS-Integrated Optical Receivers for On-Chip Interconnects," IEEE J. Select. Topics Quantum Electron., vol.16, no.5, pp.1376–1385, 2010.
[6] X.Z. Zheng, D. Patil, J. Lexau, F. Liu, G.L. Li, H. Thacker, Y. Luo, I. Shubin, J.D. Li, J. Yao, P. Dong, D.Z. Feng, M. Asghari, T. Pinguet, A. Mekis, P. Amberg, M. Dayringer, J. Gainsley, H.F. Moghadam, E. Alon, K. Raj, R. Ho, J.E. Cunningham, and A.V. Krishnamoorthy, "Ultra-efficient 10Gb/s hybrid integrated silicon photonic transmitter and receiver," Opt. Express, vol.19, no.6, pp.5172–5186, 2011.
[7] D.A.B. Miller, "Device requirements for optical interconnects to silicon chips," Proc. IEEE, vol.97, no.7, pp.1166–1185, 2009.
[8] C. Debaes, A. Bhatnagar, D. Agarwal, R. Chen, G.A. Keeler, N.C. Helman, H. Thienpont, and D.A.B. Miller, "Receiver-less optical clock injection for clock distribution networks," IEEE J. Select. Topics Quantum Electron., vol.9, no.2, pp.400–409, 2003.
[9] S. Matsuo, A. Shinya, T. Kakitsuka, K. Nozaki, T. Segawa, T. Sato, Y. Kawaguchi, and M. Notomi, "High-speed ultracompact buried heterostructure photonic-crystal laser with 13 fJ of energy consumed per bit transmitted," Nature Photonics, vol.4, no.9, pp.648–654, 2010.
[10] K. Nozaki, S. Matsuo, T. Fujii, K. Takeda, M. Ono, A. Shakoor, E. Kuramochi, and M. Notomi, "Photonic-crystal nano-photodetector with ultrasmall capacitance for on-chip light-to-voltage conversion without an amplifier," Optica, vol.3, no.5, pp.483–492, 2016.
[11] K. Nozaki, A. Shinya, S. Matsuo, Y. Suzaki, T. Segawa, T. Sato, Y. Kawaguchi, R. Takahashi, and M. Notomi, "Ultralow-power all-optical RAM based on nanocavities," Nature Photonics, vol.6, no.4, pp.248–252, 2012.
[12] J. Joo, K.-S. Jang, S.H. Kim, I.G. Kim, J.H. Oh, S.A. Kim, G.-S. Jeong, Y. Kim, J.-E. Park, S. Kim, H. Chi, D.-K. Jeong, and G. Kim, "Silicon photonic receiver and transmitter operating up to 36 Gb/s for lambda similar to 1550 nm," Optics Express, vol.23, no.9, pp.12232–12243, 2015.
[13] T. Takemoto, H. Yamashita, F. Yuki, N. Masuda, H. Toyoda, N. Chujo, Y. Lee, S. Tsuji, and S. Nishimura, "A 25-Gb/s 2.2-W 65-nm CMOS Optical Transceiver Using a Power-Supply-Variation-Tolerant Analog Front End and Data-Format Conversion," IEEE J. Solid-State Circuits, vol.49, no.2, pp.471–485, 2014.
[14] H. Fukuyama, K. Sano, K. Murata, H. Kitabayashi, Y. Yamane, T. Enoki, and H. Sugahara, "Photoreceiver module using an InP HEMT transimpedance amplifier for over 40 Gb/s," IEEE J. Solid-State Circuits, vol.39, no.10, pp.1690–1696, 2004.
[15] A. Huber, D. Huber, T. Morf, H. Jäckel, C. Bergamaschi, V. Hurm, M. Ludwig, and M. Schlechtweg, "Monolithic, high transimpedance gain (3.3 kΩ), 40 Gbit s InP-HBT photoreceiver with differential outputs," Electron. Lett., vol.35, no.11, pp.897–898, 1999.
[16] K. Takahata, Y. Muramoto, H. Fukano, and Y. Matsuoka, "52 GHz bandwidth monolithically integrated WGPD/HEMT photoreceiver with large O/E conversion factor of 105 V/W," Electron. Lett., vol.35, no.19, pp.1639–1640, 1999.
[17] Finisar. Available: https://www.finisar.com/optical-components/xprv2022a
[18] R. Going, T.J. Seok, J. Loo, K. Hsu, and M.C. Wu, "Germanium wrap-around photodetectors on Silicon photonics," Opt. Express., vol.23, no.9, pp.11975–11984, 2015.
[19] L. Virot, P. Crozat, J.-M. Fédéli, J.-M. Hartmann, D. Marris-Morini, E. Cassan, F. Boeuf, and L. Vivien, "Germanium avalanche receiver for low power interconnects," Nature Communications, vol.5, p.4957, 2014.
[20] K. Takeda, T. Sato, A. Shinya, K. Nozaki, W. Kobayashi, H. Taniyama, M. Notomi, K. Hasebe, T. Kakitsuka, and S. Matsuo, "Few-fJ/bit data transmissions using directly modulated lambda-scale embedded active region photonic-crystal lasers," Nature Photonics, vol.7, no.7, pp.569–575, 2013.
[21] A. Shakoor, K. Nozaki, E. Kuramochi, K. Nishiguchi, A. Shinya, and M. Notomi, "Compact 1D-silicon photonic crystal electro-optic modulator operating with ultra-low switching voltage and energy," Optics Express, vol.22, no.23, pp.28623–28634, 2014.
[22] Lumerical. Available: https://www.lumerical.com/
[23] T. Nagatsuma, "Measurement of High-Speed Devices and Integrated-Circuits Using Electrooptic Sampling Technique," IEICE Trans. Electron., vol.E76c, pp.55–63, 1993.



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