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FOREWORD

Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

"Internet of Things (IoT)" has had a profound impact on business processes and daily life in recent years. Billions of IoT devices such as smart-phones, tablets and watches are networked and connected to cloud network. In the IoT age, the edge computing, which processes big data at each edge device, becomes important technique to reduce data traffic and save energy dissipation. Solid-state circuit design is essential for this and will be driven by the endless efforts of innovators, some of which are high-lighted in this special section.

It is my great honor to announce the publication of this special section on solid-state circuit design. This section contains 10 regular papers and 1 brief paper, devoted to the distinctive exploration of new techniques on integrated circuits. The first paper presents a 27.5–29.6 GHz fractional-N frequency synthesizer using reference and frequency doublers for 5G mobile communications. The second and third papers respectively propose a new high-linearity Gm-cell for a continuous-time $\Delta\Sigma$ analog-to-digital converter and a 7-GS/s complete DDFS (Direct Digital Frequency Synthesizer) solution, featuring a two-time interleaved resistive digital-to-analog converter. Two other papers demonstrate a quick-start method for pulse-width-controlled PLL and a new calibration technique for a current-mirror circuit. For human healthcare, a physical activity classification and metabolic-equivalent-monitoring SoC is presented. A precise real-usage-based reliability test for the NAND flash of SSDs is explored. Further, the performance difference between the storage-class memories (SCMs)/NAND flash hybrid SSD and the SCM-based SSD is investigated. For the compressed-sensing-based CMOS image sensor, an algorithm to generate a series of deterministic and ternary matrices is proposed. From the reliability perspective, a radiation-hardened flip-flop (FF) with stacked transistors, based on the adaptive coupling flip-flop (ACFF), is discussed. For a coordinate rotational digital computer (CORDIC), an arithmetic processor utilizing both the angle recoding (ARD) CORDIC algorithm and scaling-free (SCFE) CORDIC algorithm is shown in the final paper.

On behalf of the editorial committee, I would like to express my sincere appreciation to all the authors for their contributions and to all the reviewers for their critical inputs. In addition, I would like to thank the editorial committee for their work on this special section.

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Hideto Hidaka *(Nonmember)* received the B.E., M.E. and Ph. D degrees from the University of Tokyo, Japan in 1981, 1983 and 1994, respectively. He has been with Mitsubishi Electric Corp., Renesas Technology Corp., and Renesas Electric Corp. for R&D of high-density memory, embedded memory and MCU product platform. At Renesas Electronics he has been engaged in corporate technical management. He is an IEEE Fellow.