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A Unified Analysis of the Signal Transfer Characteristics of a Single-Path FET-R-C Circuit

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SUMMARY A frequently occurring subcircuit consists of a loop of a resistor (R), a field-effect transistor (FET), and a capacitor (C). The FET acts as a switch, controlled at its gate terminal by a clock voltage. This subcircuit may be acting as a sample-and-hold (S/H), as a passive mixer (P-M), or as a bandpass filter or bandpass impedance. In this work, we will present a useful analysis that leads to a simple signal flow graph (SFG), which captures the FET-R-C circuit's action completely across a wide range of design parameters. The SFG dissects the circuit into three filtering functions and ideal sampling. This greatly simplifies analysis of frequency response, noise, input impedance, and conversion gain, and leads to guidelines for optimum design. This paper focuses on the analysis of a single-path FET-R-C circuit's signal transfer characteristics including the reconstruction of the complete waveform from the discrete-time sampled voltage.

key words: *Sampling, sample-and-hold, passive mixer, sampling oscilloscope, N-path mixer, signal flow graph, frequency translation, conversion gain, noise figure, input impedance*

1. Introduction

The FET-R-C circuit is a primitive building block that appears in many systems. The circuit, Fig. 1(a), is composed of a series connection of a single Field Effect Transistor (FET), a resistor, and a capacitor, driven by a voltage or a current source. An additional resistor can be connected in parallel with the capacitor as an output load or to model leakage in the capacitance, or to define a filter's passband. The most well-known application of this circuit is a sample-and-hold (S/H) or a track-and-hold (T/H) in front of almost every analog-to-digital (A/D) converter, a fundamental building block in today's digital world which captures the input signal at the turn-off instant of the FET [1]–[3]. This simple circuit can also provide functions that include frequency translation of the incoming bandlimited signal. A representative application is a passive mixer (P-M) in an RF receiver that downconverts the input RF signal to IF or baseband [4]–[12], or in an RF transmitter that upconverts the signal [13]. Also in RF applications, this circuit is used as a tunable bandpass filter or bandpass impedance [14]–[17]. If employed in an instrument such as an equivalent-time oscilloscope, this circuit would comprise the sampling head [18]. Indeed, this sampling circuit topology has been used for more than 50 years [19], sometimes employing a diode bridge as the switch [2], [18], at other times a vacuum tube [20].

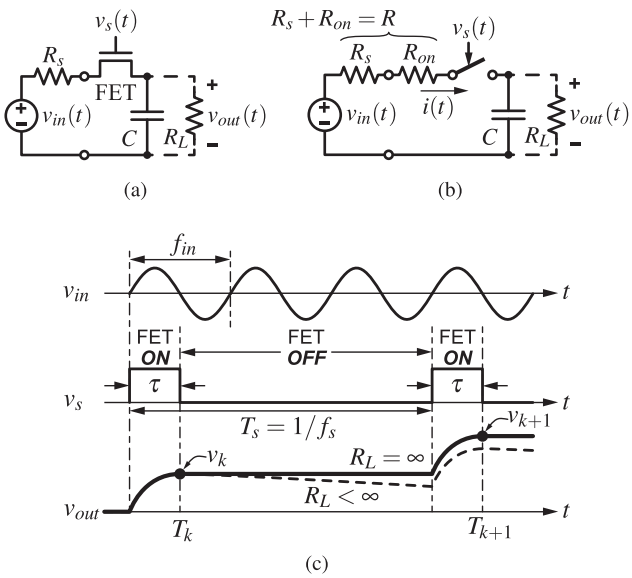

Fig. 1 An FET-R-C circuit in general. (a) Original FET-R-C circuit. (b) An FET is simplified to an ideal switch and ON resistance. (c) A waveform example of FET-R-C circuit.

While these circuits are widely employed, there exists no unified theory to guide the design; We venture two reasons: a) This circuit transforms analog quantities from continuous time into analog quantities in discrete time, so it *sits at the boundary* between two heterogeneous time domains. Each is characterized by different methods: e.g. the Laplace variable s is customary for continuous time description, but the z variable for discrete time. b) It is a *time-varying circuit* that periodically partitions itself into two disjoint pieces.

Existing analyses of the sample-and-hold often model it as an ideal impulse sampler followed by a zero-order hold function [21, Sec. 8.9] [22, Sec. 2.4]. This high-level abstraction suffices when the signal processing of interest occurs after sampling. But when the sample-and-hold circuit's internal signal processing is itself the object of interest, this abstraction falls short. Many papers have been devoted to the analysis of the transfer characteristics of the FET-R-C circuit's S/H action [23]–[28], while other papers develop the theory behind its mixing action [10], [29]–[34]. In the two-part paper [35], [36] we have provided, for the first time, a unified answer.

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The analysis of this circuit in the literature [1], [28], [29], [34], [37], is often limited in scope or focuses on a restricted structure, e.g. a purely capacitive load. The circuit invites a linear periodically time-variant (LPTV) analysis [38] which entails an infinite number of translated signals in frequency arising from periodic switching. Due to its mathematical complexity, however, the LPTV analysis does not always lend an intuitive understanding. Some approaches to analysis simplify their results through approximations at the expense of accuracy. While the correctness of the results is usually not in question because they can be checked against circuit simulation, for the purposes of circuit design we need an analysis that presents the circuit's operation in a form that is easily visualized, preferably with little loss of accuracy.

This paper will provide a brief introduction of some representative applications of the FET-R-C circuit. Then we will present a useful design-oriented analysis that leads to a signal flow graph (SFG), enabling a new visualization of the FET-R-C circuit's action across a wide range of design parameters and operating conditions. The SFG that describes the transfer characteristic gives us a complete understanding of the FET-R-C circuit behavior in a wide variety of applications, including a simple S/H, an N-path passive mixer, an N-path filter, a sampling oscilloscope, and so on. A signal flow graph for the reconstruction of the complete waveform from the discrete-time sampled voltage are discussed in detail.

2. FET-R-C Circuit Applications

2.1 Sample-and-Hold Circuit

Figure 2(a) is a sample-and-hold (S/H) circuit example that appears in front of almost every A/D converter to capture an incoming continuous signal at a sampling instant and to provide a stable voltage to the subsequent block. In this use, typically the input frequency f_{in} is within the 1st Nyquist band $[0, f_s/2]$, where f_s is a sampling frequency. Ideally, the S/H circuit should capture the input voltage at the sampling instant as in Fig. 2(b) with no residual effect of the previous samples. To meet this requirement the switch-ON (tracking) period τ should be long enough compared to the RC time constant of the FET-R-C circuit so that the output fully tracks the input by the time that the switch turns OFF. In the frequency domain, the input signal is aliased through the sampling action as shown in Fig. 2(c). If the input signal is bandlimited within the 1st Nyquist band, the original signal is reproduced from the discrete-time sampled signal.

2.2 Passive Mixer

The second example illustrated in Fig. 3(a) is a passive mixer. This use involves frequency translation. The passive mixer (P-M) is often used to downconvert the signal at radio frequency (RF) to baseband or intermediate frequency (IF). Without loss of generality the different input and output frequencies f_{in} and f_{out} are defined as

$$f_{in} = M \times f_s + f_{out}, \tag{1}$$

where M is an integer that defines an undersampling ratio. When $M = 1$, the input frequency around f_s is aliased to baseband through the sampling action as illustrated in Fig. 3(c). For this use the RC bandwidth of the FET-R-C circuit is typically designed to be narrower than f_{in}. Thus the output voltage does not fully track the input as illustrated in Fig. 3(b). Still the output baseband component is recovered by the P-M design with appropriate parameter choice. Our analysis leads to guidelines for optimum design [35], [36]. The P-M for RF application often uses a multi-path configuration that uses N identical FET-R-C circuits connected in parallel, each driven by a different phase of the clock. The clock signals use duty ratio $D = 1/N$ to have non-overlapping switch-ON periods. The behavior of this multi-path configuration is also precisely modeled by our analysis [36].

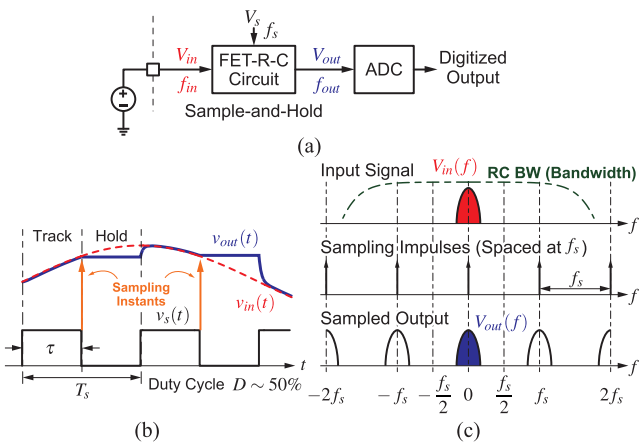


Fig. 2 (a) An example circuit diagram, (b) a time-domain and (c) a frequency-domain overview of the FET-R-C circuit in a sample-and-hold example.

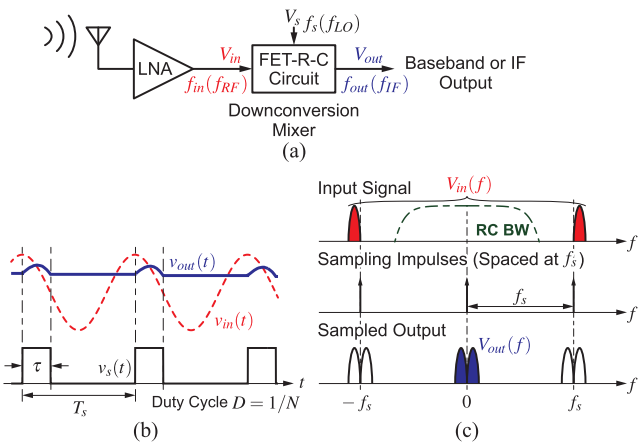


Fig. 3 (a) An example circuit diagram, (b) a time-domain and (c) a frequency-domain overview of the FET-R-C circuit in a passive downconversion mixer example.

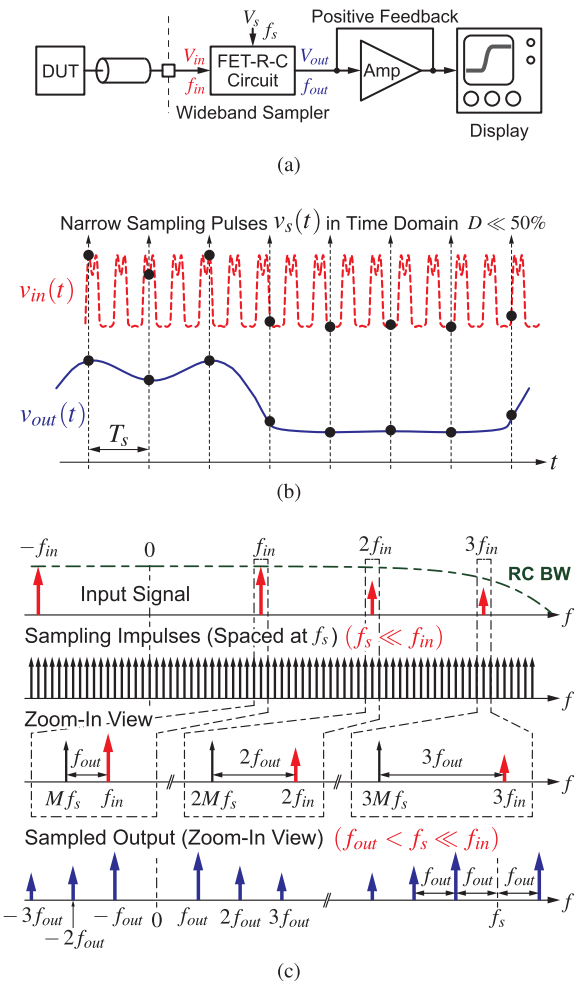


Fig. 4 (a) An example circuit diagram, (b) a time-domain and (c) a frequency-domain overview of the FET-R-C circuit in a sampling oscilloscope example.

2.3 Sampling Oscilloscope

Figure 4 illustrates an example of a sampling oscilloscope application. Since it is used to capture wideband periodic signal waveforms, the FET-R-C circuit has to be designed for wide bandwidth. Among other reasons to prevent disturbance of the device under test, impulse-like, narrow pulses are used to sample the voltage waveform of interest. Therefore the every voltage sample acquired by the FET-R-C circuit is a fraction of the input voltage being measured. Based on the literature a feedback circuit is used to compensate this attenuation, as illustrated in Fig. 4(a) [39]–[41]. Figure 4(b) shows the concept of the undersampling in time domain. A periodic input waveform is supposed to be sampled with a period of T_s, which is set to be a multiple of the period of the input waveform *plus a small time offset*. With this time offset, relative sampling position gradually shifts with respect to the input waveform. Typically, the sampling frequency $f_s = 1/T_s$ is much slower than the input frequency f_{in}, hence the undersampling ratio $M \gg 1$. A set of the sampled points

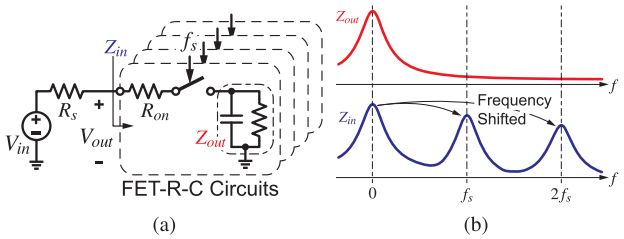


Fig. 5 (a) An example circuit diagram and (b) plots of output and input impedances Z_{out} and Z_{in} of the multi-channel FET-R-C circuit.

reconstructs the shape of the input waveform at much slower frequency, which is recognized as a waveform expansion in time domain through sampling. In frequency domain, this sampling action is explained with Fig. 4(c). Since the input is a periodic waveform, in frequency domain it is composed of harmonic frequency components that locate at integer multiples of the input fundamental frequency f_{in}. Supposing $f_s \ll f_{in}$, the sampling impulses are densely placed on the frequency axis as in Fig. 4(c). By closely looking at f_{in}, M-th sampling impulse is located at $f_{in} - f_{out}$ by choosing f_s to satisfy (1). Therefore, through the sampling action the signal at f_{in} is translated to f_{out} at the output. Similarly, the k-th harmonic component of the input is translated to kf_{out}. As a result, all the harmonic frequency components at kf_{in} within the acceptable bandwidth are translated to much slower frequency components at kf_{out} while preserving their relative position in frequency domain. That is, the input signal is compressed in frequency domain [42]. Therefore, through the sampling a high frequency and wideband input signal is reproduced as a lower frequency version while preserving its waveform shape in time domain.

2.4 Bandpass Impedance

Figure 5(a) illustrates an example of a bandpass impedance realized by a parallel connection of N-channel FET-R-C circuits. In contrast to the former three examples, this application does not depend on an input-to-output signal transfer function but instead uses the frequency response of the input impedance as a filter. A multi-channel implementation is commonly used. Supposing the output load impedance Z_{out} is a parallel RC: then the driving-point impedance Z_{in} at the input port becomes a frequency-shifted version of Z_{out} [14]–[16] as shown in Fig. 5(b). Since the impedance peak in frequency is determined by f_s, this has been used as a bandpass circuit with tunable center frequency.

3. Transfer Characteristic of the FET-R-C Circuit

Figure 1(b) illustrates a simplified equivalent circuit of the original FET-R-C circuit in Fig. 1(a), which is composed of an input voltage source $v_{in}(t)$ with its source resistance R_s, an FET, and an output load consisting of a capacitance C and a resistance R_L. The FET is modeled as an ON-resistance R_{on} in series with an ideal switch that has an infinite OFF-resistance and a zero ON-resistance. R_s and R_{on} in series

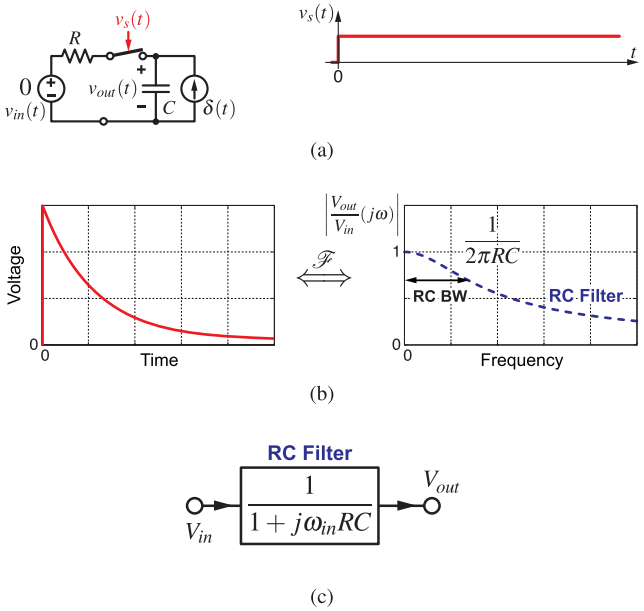


Fig. 6 (a) An FET-R-C circuit with an impulse input when the switch is kept ON, (b) its impulse and frequency responses and (c) its signal flow graph in frequency domain.

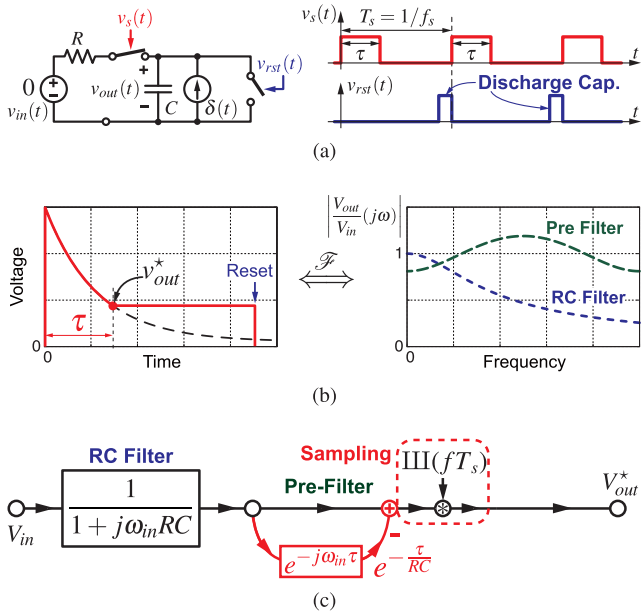


Fig. 7 (a) An FET-R-C circuit with an impulse input and a reset switch when the switch is driven by a clock signal, (b) its impulse and frequency responses and (c) its signal flow graph in frequency domain.

define a single resistance, $R = R_s + R_{on}$. Figure 1(c) shows example waveforms of a general FET-R-C circuit operation. The input voltage $v_{in}(t)$ of frequency f_{in} is fed into the FET-R-C and is sampled with the ideal switch that is actuated by $v_s(t)$ at a frequency $f_s = 1/T_s$. We assume that both transition times of $v_s(t)$ are sufficiently small to be ignored for simplicity, though our analysis can be extended to take into account non-zero transition time. Due to the periodically operated switch, this circuit is inherently a Linear Time-Variant (LTV) system. Over the switch-ON period, however, we can treat this circuit as time-invariant.

The detailed mathematical derivation of the signal transfer function and the SFG is given in [35]. In this paper we will introduce a more intuitive way to compose the SFG focusing on the case without a load resistance R_L.

First, as shown in Fig. 6(a), we start with the FET-R-C circuit with its switch always ON. This is simply an RC lowpass filter whose time-domain impulse response is an exponential decay as shown in the left-hand side of Fig. 6(b), given by

$$h_{RC}(t) = \frac{1}{RC} e^{-\frac{t}{RC}}. \tag{2}$$

By applying Fourier transformation we have the transfer function $H_{RC}(j\omega_{in})$:

$$H_{RC}(j\omega_{in}) = \frac{1}{1 + j\omega_{in}RC}. \tag{3}$$

Thus the SFG in frequency domain is just a transfer function of the RC lowpass filter as shown in Fig. 6(c).

Then as the second step, we assume that the switch FET is driven by a clock signal, whose period is $T_s = 1/f_s$ and duty cycle D is defined as $D \triangleq \tau/T_s$ as shown in Fig. 7(a). Here we also assume that the voltage sampled at C is discharged through the reset switch before the switch next truns ON. The time-domain impulse response of this circuit is an exponential decay interrupted at the moment of the switch turn-OFF. Here the voltage across the capacitance is sampled, then held until the reset switch turns ON. The voltage of interest is this sampled voltage $v^\star_{out}$[†]. The time-domain waveform within $0 < t \le \tau$ is given by

$$h_2(t) = \frac{1}{RC} e^{-\frac{t}{RC}} \times \Pi\left(\frac{t - \tau/2}{\tau}\right), \tag{4}$$

where $\Pi(t)$ is a unit rectangular window function as defined in [43, Chap. 4]. Thus $\Pi\left((t-\tau/2)/\tau\right)$ is a rectangular window function centered at $t = \tau/2$ whose height and width are 1 and τ, respectively. In frequency domain, the time-domain waveform (4) is transformed to

$$H_2(j\omega_{in}) = \frac{1}{1 + j\omega_{in}RC}\left(1 - e^{-\frac{\tau}{RC}} e^{-j\omega_{in}\tau}\right) \tag{5}$$

$$= H_{RC}(j\omega_{in}) \times H_{pre}(j\omega_{in}), \tag{6}$$

which is drawn by the SFG in Fig. 7(c) by the cascade of two continuous-time filters: an RC lowpass filter H_{RC} and a raised comb filter H_{pre}, which we call a pre-filter. Since the voltage of interest is the sampled $v^\star_{out}$, an ideal periodic impulse sampling at T_s appears after the pre-filter in Fig. 8(c), where, following the notation in [43, Chap. 5], the Dirac comb Ш is defined as

$$\text{Ш}(x) \triangleq \sum_{k=-\infty}^{+\infty} \delta(x - k). \tag{7}$$

[†]The superscript $\star$ indicates that the variable signifies a set of values that define a waveform in discrete time.

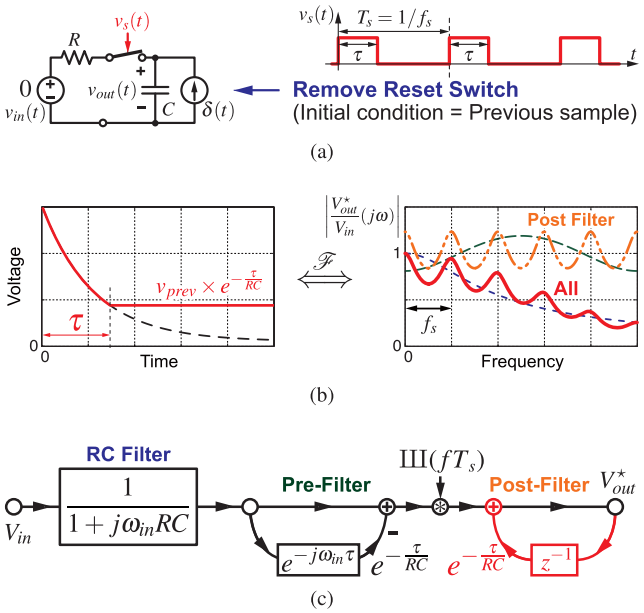


Fig. 8 (a) An FET-R-C circuit with an impulse input without reset when the switch is driven by a clock signal, (b) its impulse and frequency responses and (c) its signal flow graph in frequency domain.

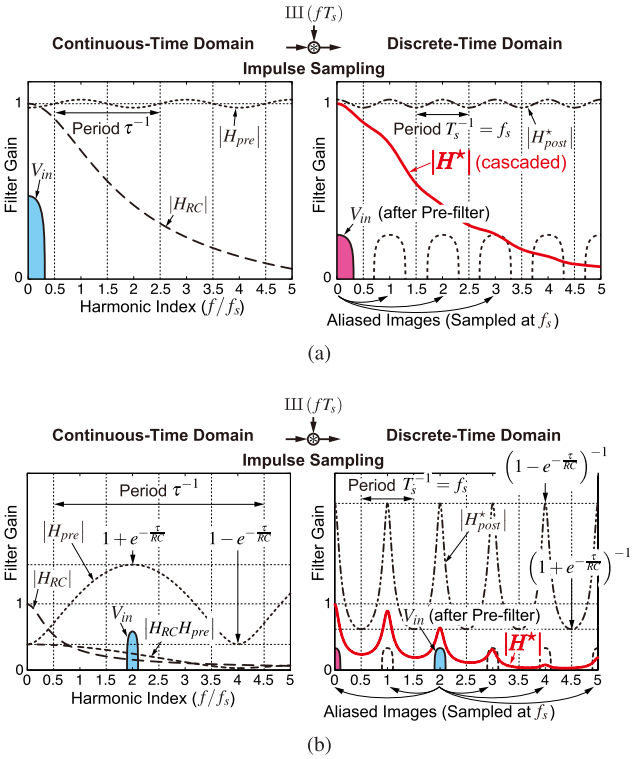


Fig. 9 Frequency-domain illustration of the FET-R-C circuit behavior. Examples with (a) $\tau/(RC) = 4.0$, $D = 0.50$ and (b) $\tau/(RC) = 0.5$, $D = 0.25$. © 2016 IEEE.

Although no impulse sampler is physically present in the circuit of Fig. 1(a), it appears implicitly in the act of capturing the instantaneous voltage on the capacitor at the moment the switch opens.

Then as the last step we remove the reset switch as shown in Fig. 8(a). Based on superposition principle the present voltage sample is a sum of a sampled output of the pre-filter and a decayed version of the previous sample. Therefore, after the impulse sampling there is a discrete-time integrator with a feedback gain $\exp(-\tau/(RC))$, which expresses the decaying effect of the previous sampled value on the present sample. This discrete-time filter is best described in the z-domain using the variable $z \equiv e^{j\omega_{in}T_s}$ such that

$$H^{\star}_{post}(z) = \frac{1}{1 - e^{-\frac{\tau}{RC}} z^{-1}}, \tag{8}$$

which we call a post-filter. When plotted on the continuous frequency axis as shown in the right-hand side of Fig. 8(b), the post-filter $H^{\star}_{post}$ exhibits another raised-comb shape.

As a whole, the signal transfer function of the FET-RC circuit is visualized by the SFG in Fig. 8(c), which is the same as that in [35, Fig. 4]. The transfer function $H^{\star}(j\omega_{in})$ from the continuous voltage V_{in} to the discrete-time sampled voltage $V^{\star}_{out}$ is given as a cascade of three functions

$$H^{\star}(j\omega_{in}) = H_{RC}(j\omega_{in}) \times H_{pre}(j\omega_{in}) \times H^{\star}_{post}(z). \tag{9}$$

The internal nodes of the SFG *do not* correspond to physically accessible nodes in the circuit. This SFG describes the *two-node circuit* as a *cascade of four operations*: a) A continuous-time RC lowpass filter H_{RC}, b) a continuous-time raised comb filter H_{pre}, followed by c) a sampler and d) a discrete-time lossy integrator $H^{\star}_{post}$. Figure 9 illustrates two examples of its frequency response, (a) with $\tau/(RC) = 4.0$ and $D = 0.50$ for use as a S/H, and (b) with $\tau/(RC) = 0.5$ and $D = 0.25$, which we will show signifies a P-M. The frequency response of H_{pre} is a raised comb with period $1/\tau$, because the loss in one feedforward branch in the SFG raises the transmission minima from zero to $(1 - \exp(-\tau/(RC)))$ as shown in the left-hand side of Fig. 9(b). The discrete-time integrator $H^{\star}_{post}$, on the other hand, is defined by feedback through a unit delay z^{-1} followed by the same loss $\exp(-\tau/(RC))$ as in the continuous-time comb filter. When plotted on the continuous f_{in} axis as shown in the right-hand side of Fig. 9(b), this lossy integrator's magnitude transfer function appears as a series of maxima, $1/(1 - \exp(-\tau/(RC)))$ alternating with minima, $1/(1 + \exp(-\tau/(RC)))$, a series of images of a discrete-time function on the continuous frequency axis that repeats at multiples of the sampling frequency f_s.

After passing through two continuous-time filters $H_{RC} \times H_{pre}$, the continuous voltage waveform is discretized through the periodic sampling at T_s. This is equivalent to a convolution of its spectrum with a frequency-domain impulse train spaced apart by $f_s = 1/T_s$. The convolution gives rise to spectral images of the filtered input, thereby realizing frequency translation. The sampled waveform is processed by the discrete-time filter $H^{\star}_{post}(z)$.

The feedback loop with a z^{-1} element in the post filter captures the memory of the previous sampled voltage. Thus

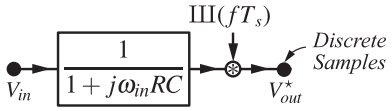


Fig. 10 A simplified signal flow graph for sample-and-hold applications.

the feedback gain $\exp(-\tau/(RC))$ of this loop expresses the decaying effect of the previous sampled value on the present sample. Since the function of $H^{\star}_{post}$ is periodic at f_s, all the images are subject to the same filter function, as shown in Fig. 9.

3.1 Simplification of the SFG

Equation (9) and the SFG in Fig. 8(c) form the basis of a unified treatment and understanding of the FET-R-C circuits. They can be further simplified for specific cases, which lead to straightforward insights into design. The following subsections explain the simplification procedure for two representative examples of a S/H and a P-M circuit. To distinguish these two uses, the ratio between the ON period τ and the RC time constant is used as an indicator. In [37], Soer *et al.* define $\tau/(RC) = 2$ as the boundary between these two operation modes based on the fact that noise power spectral density is limited mostly by R in the mixer but by C in the S/H[†]. We have presented a detailed noise analysis in [36], but for now we define this boundary condition as the point that the ripple in the passband of both H_{pre} and $H^{\star}_{post}$ filters is roughly ±10% (±1dB). This ripple increases with smaller $\tau/(RC)$ until, owing to the residual effect of the previous voltage sample, it dominates the passive sampling mixer as shown in Fig. 9(b). Now the peak transmission will occur at integer multiples of the sampling frequency only, a consequence of synchronous sampling and advantageous when the signal of interest is narrowband at f_s.

3.1.1 Simplification for S/H

The S/H circuit is used in front of A/D converters to capture the input voltage at sampling instants. Since the output voltage has to fully track the input at the sampling instant, the RC bandwidth must be wide enough. In practice, the switch ON period τ is 5~10×RC [22]. With this choice, $\exp(-\tau/(RC)) \approx 0$, which eliminates the feedforward path in the pre-filter of Fig. 8(c) and the feedback path in the post-filter. This means that the present voltage sample is not affected by the previous one. This is one of the requirements of an ideal sample-and-hold. As a result, the SFG collapses into an elementary RC filter as shown in Fig. 10. The transfer function from the input voltage to the sampled discrete-time output voltage is now written as

$$H^{\star}_{S/H}(j\omega_{in}) = \frac{1}{1 + j\omega_{in}RC}, \tag{10}$$

and illustrated in Fig. 9(a). Since $\exp(-\tau/(RC)) \approx 0$, the passband ripple in both H_{pre} and $H^{\star}_{post}$ disappears and their gain converges to 1. The cascade response is simply an RC lowpass. Thus the input voltage is merely subject to this RC filter H_{RC}, then sampled by an ideal sampler. This is a complete model of a practical sample-and-hold circuit, and we say that the FET-R-C circuit is operating in *S/H mode*.

3.1.2 Simplification for P-M

This use involves frequency translation. Passive mixers will downconvert a narrowband spectrum of interest to a low intermediate frequency, so the output frequency f_{out} is different from the input frequency f_{in}. Without loss of generality, we can use (1). It follows that $\exp(-j\omega_{in}T_s) = \exp(-j\omega_{out}T_s)$. A narrow sampling window τ must be used in these applications [10], [37], thus we can reasonably assume that $\tau \ll RC$, and $\exp(-\tau/(RC)) \approx 1 - \tau/(RC)$. The feedback branch in the post filter of the SFG (Fig. 8(c)) is now fully active and the previous sample strongly influences the present one. The frequency response is now as in Fig. 9(b). $\exp(-\tau/(RC)) \to 1$ causes large ripples both in H_{pre} and $H^{\star}_{post}$ and at their gain peak they compensate the attenuation by the RC filter exactly. The resultant cascade transfer function $H^{\star}$ exhibits a repeating bandpass characteristic. (9) can now be rewritten as

$$H^{\star}(j\omega_{in}, j\omega_{out}) \approx \frac{1}{1 + j\omega_{in}RC} \frac{1 + \frac{\tau}{RC} - e^{-j\omega_{in}\tau}}{1 + \frac{\tau}{RC} - e^{-j\omega_{out}T_s}}. \tag{11}$$

Using the identity $1 - e^{-jx} \equiv 2j \sin\left(\frac{x}{2}\right) e^{-j\frac{x}{2}}$, the right-hand side simplifies to

$$\frac{1}{1 + j\omega_{in}RC} \frac{\frac{\tau}{RC}\left(1 + j\omega_{in}RC\ \mathrm{sinc}(f_{in}\tau)e^{-j\pi f_{in}\tau}\right)}{\frac{\tau}{RC} + (1 - e^{-j\omega_{out}T_s})}. \tag{12}$$

Suppose $f_{in} \gg 1/(2\pi RC)$. Then the input voltage is diminished by a factor of $\sim (\tau/(RC))\,\mathrm{sinc}(f_{in}\tau)$ by RC and pre-filters. After sampling, its image at or near DC is amplified again by the post-filter by a gain of $(RC)/\tau$. Therefore, when the switch ON period τ is sufficiently narrow such that $\mathrm{sinc}(f_{in}\tau) \approx 1$, the signal attenuation by $\tau/(RC)$ before sampling is fully restored by the post-filter after sampling. Finally, assuming that an image of the input frequency f_{in} lies at f_{out} and $f_{out} \ll f_s = 1/T_s$, we can approximate $\exp(-j\omega_{out}T_s) \approx 1 - j\omega_{out}T_s$. This leads to a further simplification in the P-M's transfer function:

$$H^{\star}_{P\text{-}M}(j\omega_{in}, j\omega_{out}) = \frac{\mathrm{sinc}(f_{in}\tau)}{1 + j\omega_{out}\frac{RC}{D}} e^{-j\omega_{in}\frac{\tau}{2}}. \tag{13}$$

The simplified SFG for this mode of operation is shown in Fig. 11. The RC and pre-filters are merged into one sinc-shaped filter. The sinc and post-filters are distinguished by DC gains of $\tau/(RC)$ and $(RC)/\tau$, respectively, whose product is 1. The sampled voltage traverses the 1st-order lowpass filter whose bandwidth depends on both the RC time constant and the duty cycle D of sampling pulses. We call this operation mode as the passive mixer mode (*P-M mode*).

[†]They use the symbol $\Gamma = \tau/(RC)$ in their paper.

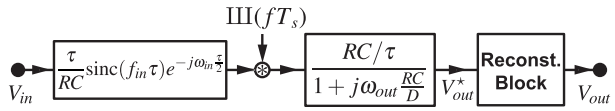


Fig. 11 A simplified signal flow graph for passive mixer and undersampling applications with a baseband frequency (ω_{out}) output. A reconstruction block is needed after the SFG to convert discrete-time samples to a continuous-time analog waveform. This block is explained in Sect. 3.2. © 2016 IEEE.

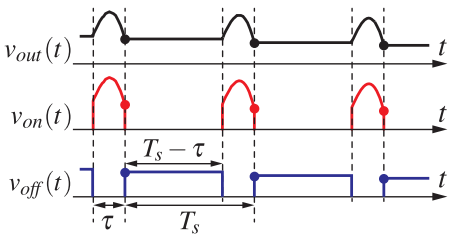


Fig. 12 Decomposition of the output waveform. © 2016 IEEE.

(13) is consistent with the result in [37], which however emerges from a cumbersome LPTV analysis.

3.2 Conversion from Discrete- to Continuous-Time

In the S/H use with A/D converters, the sampled discrete voltage is converted into a digital signal. Therefore the signal transfer function for the sampled output $H^{\star}(j\omega_{in})$ is sufficient. In the mixer use, on the other hand, the entire continuous-time voltage waveform across the capacitance C matters, because this waveform is processed by subsequent analog circuits such as filters. To take into account the conversion of discrete-time samples $V^{\star}_{out}$ to a continuous-time waveform V_{out}, a reconstruction block is needed in the SFG as illustrated in Fig. 11 for P-M mode.

For mixer use, while the switch is ON the FET-R-C output waveform is equal to the continuous output from a simple RC circuit. While the switch is OFF, on the other hand, the sampled output voltage is zero-order held. As illustrated in Fig. 12, the entire continuous-time waveform $v_{out}(t)$ is the piecewise summation of these two waveforms written as

$$v_{out}(t) = \begin{cases} v_{on}(t), & T_k - \tau < t \le T_k \\ v_{off}(t), & T_k < t \le T_{k+1} - \tau. \end{cases} \tag{14}$$

In this section we explain details of a formal procedure to construct this composite waveform in continuous-time.

A frequency-domain illustration of the SFG for this discrete- to continuous-time conversion procedure is summarized in Fig. 13 [35, Fig. 17], which is equivalent to the ones presented in [37], [44]. The upper half is for $V_{on} = \mathcal{F}[v_{on}(t)]$ generation and the lower half is for $V_{off} = \mathcal{F}\left[v_{off}(t)\right]$. Since for a simple RC circuit $v_{on}(t)$ is divided into a steady-state component $v_{ss}(t)$ and a transient component $v_{tran}(t)$, the upper part is further segmented into two paths for $\hat{V}_{ss}$ and $\hat{V}_{tran}$ respectively, where $V_{on} = \hat{V}_{ss} + \hat{V}_{tran}$.

Firstly, Fig. 14 illustrates how $V_{off}(f)$ is calculated in

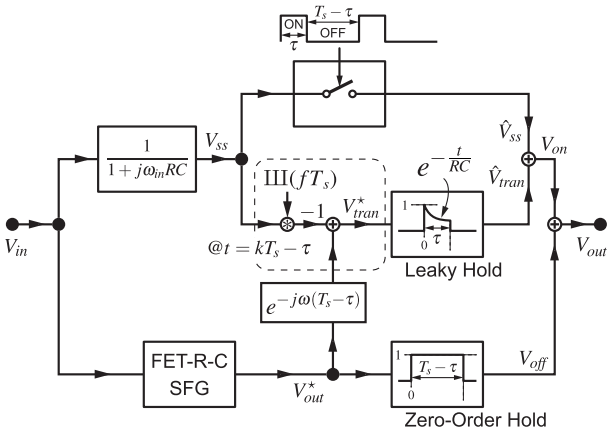


Fig. 13 A signal flow graph of the discrete-time to continuous-time waveform reconstruction in the FET-R-C circuit. © 2016 IEEE.

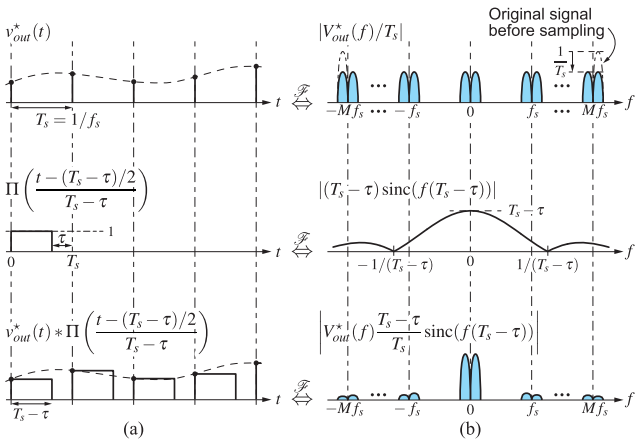


Fig. 14 Time- and frequency-domain calculations of zero-order-held while the switch is in OFF state.

the time and frequency domains. As shown in (a), while the switch is OFF $v_{off}(t)$ is a zero-order-held version of the discrete-time sampled voltage $v^{\star}_{out}(t)$, which is given by a convolution of $v^{\star}_{out}(t)$ and a rectangular window function given by $\Pi\left((t-(T_s-\tau)/2)/(T_s-\tau)\right)$. Since a convolution in time domain is a multiplication in frequency domain, V_{off} in frequency domain is illustrated as in Fig. 14(b), and is given by

$$V_{off}(f) = V^{\star}_{out}(f)\frac{T_s-\tau}{T_s}\,\mathrm{sinc}\left(f(T_s-\tau)\right)e^{-j\pi f(T_s-\tau)}. \tag{15}$$

Frequency f depends on which aliased frequency component in Fig. 14(b) is of interest. This frequency selection will be discussed later in this section.

Secondly, while the switch is ON the steady-state part of the output waveform in time domain $\hat{v}_{ss}(t)$ is recognized as the multiplication of the continuous waveform $v_{ss}(t)$ and a pulse train whose pulse width and period are τ and T_s respectively, as illustrated in Fig. 15(a). Since this pulse train in time domain is a result of a convolution of a rectangu-

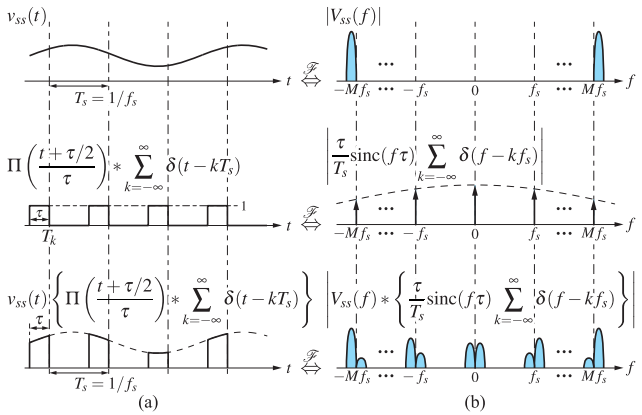


Fig. 15 Time- and frequency-domain calculations of steady-state waveform component while the switch is in ON state.

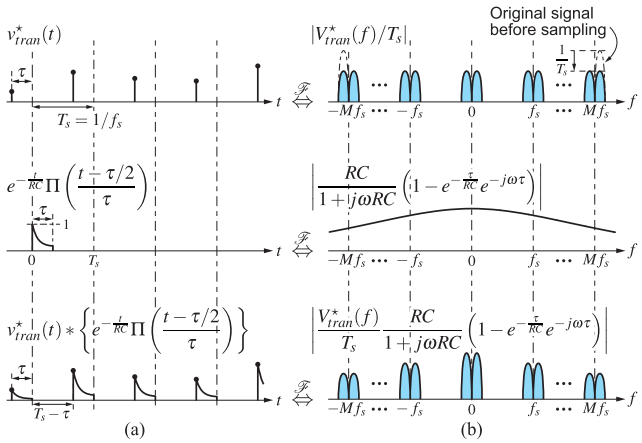


Fig. 16 Time- and frequency-domain calculation of transient waveform component while the switch is in ON state.

lar window function $\Pi((t+\tau/2)/\tau)$ and a unit impulse train $\sum_{k=-\infty}^{\infty}\delta(t-kT_s)$, in frequency domain it is given by

$$\tau\,\mathrm{sinc}(f\tau)e^{j\pi f\tau}\times\frac{1}{T_s}\sum_{k=-\infty}^{\infty}\delta(f-kf_s), \tag{16}$$

as shown in Fig. 15(b). Therefore, the frequency-domain representation of $\hat{V}_{ss}(f)$ is given with a convolution by

$$\hat{V}_{ss}(f)=V_{ss}(f_{in})*\left[\frac{\tau}{T_s}\,\mathrm{sinc}(\zeta\tau)e^{j\pi\zeta\tau}\times\sum_{k=-\infty}^{\infty}\delta(\zeta-kf_s)\right]. \tag{17}$$

Since the steady-state waveform V_{ss} has f_{in} component only and is attenuated by the RC filter at f_{in}, $V_{ss}(f_{in})$ in the above equation is a function of f_{in} and is given by $V_{ss}(f_{in}) = V_{in}(f_{in})/(1+j2\pi f_{in}RC)$. A frequency f in (17) again depends on which aliased frequency component is of interest. Here in this equation, the frequency of interest f is an outcome of a multiplication between the original f_{in} and an impulse at kf_s through a convolution as illustrated in Fig. 15(b).

Thirdly, the transient part of the output waveform $\hat{v}_{tran}(t)$ is an exponentially-decaying waveform within switch-ON. Its initial voltage $v^{\star}_{tran}(t)$ is a sum of the initial voltage of the steady-state waveform $v_{ss}(kT_s-\tau)$ and the previous sampled voltage. Thus in time domain, this discrete-time initial voltage at $t=kT_s-\tau$ is given by

$$\begin{aligned}v^{\star}_{tran}(t)&=\sum_{k=-\infty}^{\infty}\left[-\{v_{ss}(kT_s-\tau)-v_{k-1}\}\right]\\&=-v_{ss}(t)\times\sum_{k=-\infty}^{\infty}\delta(t-kT_s+\tau)+\sum_{k=-\infty}^{\infty}v_{k-1},\end{aligned} \tag{18}$$

and is transformed to

$$V^{\star}_{tran}(f)=-V^{\star}_{ss}(f)+V^{\star}_{out}(f)e^{-j2\pi f(T_s-\tau)}. \tag{19}$$

Supposing $v_{k-1}=v_{out}(T_{k-1})$, $T_s-\tau$ shift in time domain, which corresponds to the multiplication of $\exp(-j2\pi f(T_s-\tau))$ in frequency domain, is applied to $V^{\star}_{out}$ as is also shown in the SFG in Fig. 13. $V^{\star}_{ss}(f_{in})$ is a sampled version of $V_{ss}(f_{in})$ at $t=kT_s-\tau$ and is written as

$$V^{\star}_{ss}(f)=V_{ss}(f_{in})*\sum_{k=-\infty}^{\infty}\delta(\zeta-kf_s)e^{j2\pi\zeta\tau}. \tag{20}$$

Since $V^{\star}_{ss}(f_{in})$ is a discrete-time sampled voltage, it has aliased frequency components as illustrated in Fig. 16(b). The entire time-domain waveform of the transient component $\hat{v}_{tran}(t)$ is expressed by a convolution of the initial voltage $v^{\star}_{tran}(t)$ and a windowed exponential decay function $\exp(-t/(RC))\times\Pi((t-\tau/2)/\tau)$ as illustrated in Fig. 16(a). With Fourier transformation

$$\mathcal{F}\left[e^{-\frac{t}{RC}}\Pi\left(\frac{t-\tau/2}{\tau}\right)\right]=\frac{RC}{1+j2\pi fRC}\left(1-e^{-\frac{\tau}{RC}}e^{-j2\pi f\tau}\right). \tag{21}$$

Thus in frequency domain $\hat{V}_{tran}(f)$ is given by

$$\begin{aligned}\hat{V}_{tran}(f)&=-\frac{1}{T_s}\left(V^{\star}_{ss}(f)-V^{\star}_{out}(f)e^{-j2\pi f(T_s-\tau)}\right)\times\\&\quad\frac{RC}{1+j2\pi fRC}\left(1-e^{-\frac{\tau}{RC}}e^{-j2\pi f\tau}\right)\end{aligned} \tag{22}$$

From the SFG in Fig. 13 and using (15), (17), and (22), the entire continuous output waveform in the frequency domain is

$$V_{out}(f)=V_{off}(f)+\hat{V}_{ss}(f)+\hat{V}_{tran}(f). \tag{23}$$

In the following subsections, we will discuss the procedures to extract the f_{out} and f_{in} components, respectively.

3.2.1 Extraction of f_{out} Component

Both in S/H and passive mixer uses, the wanted output frequency f_{out} is normally at baseband. For V_{off} and $\hat{V}_{tran}$, we can obtain f_{out} component just by replacing f with f_{out} in (15) and (22). $V^{\star}_{ss}(f_{out})$ in (22) is then calculated by using $\zeta=-Mf_s$ in (20) supposing (1) and that f_{out} is at baseband.

Therefore, $\hat{V}_{tran}(f_{out})$ is given by

$$\hat{V}_{tran}(f_{out}) = -\frac{1}{T_s}\left(\frac{V_{in}(f_{in})}{1+j2\pi f_{in}RC}e^{-j2\pi M f_s\tau} - V^{\star}_{out}(f_{out})e^{-j2\pi f_{out}(T_s-\tau)}\right) \times \frac{RC}{1+j2\pi f_{out}RC}\left(1-e^{-\frac{\tau}{RC}}e^{-j2\pi f_{out}\tau}\right). \quad (24)$$

Similarly for $\hat{V}_{ss}$, we also replace ζ in (17) with $-Mf_s$. Thus $\hat{V}_{ss}(f_{out})$ is

$$\hat{V}_{ss}(f_{out}) = \frac{V_{in}(f_{in})}{1+j2\pi f_{in}RC}\frac{\tau}{T_s}\,\mathrm{sinc}(Mf_s\tau)e^{-j\pi Mf_s\tau}. \quad (25)$$

In a practical S/H use where $M = 0$ and $f_{out} = f_{in}$, we use $\tau/(RC) \sim 5$ to 10. Under this assumption, $\exp(-\tau/(RC)) \approx 0$, then $V^{\star}_{out} = H^{\star}_{S/H}V_{in}$ where $H^{\star}_{S/H}$ is given by (10). Thus we can approximate $\hat{V}_{tran}(f_{out})$

$$\hat{V}_{tran}(f_{out}) \approx -\frac{V^{\star}_{out}}{T_s}\left(1-e^{-j2\pi f_{out}(T_s-\tau)}\right)\frac{RC}{1+j2\pi f_{out}RC} = -(1-D)\frac{j2\pi f_{out}RC}{1+j2\pi f_{out}RC}V^{\star}_{out}\,\mathrm{sinc}\left(f_{out}(T_s-\tau)\right)e^{-j\pi f_{out}(T_s-\tau)}. \quad (26)$$

Under the same assumption, $\hat{V}_{ss}$ is given by

$$\hat{V}_{ss}(f_{out}) = D\frac{V_{in}(f_{in})}{1+j2\pi f_{in}RC} = DV^{\star}_{out}(f_{out}). \quad (27)$$

As a result, for S/H $V_{out}(f_{out})$ is given by

$$V_{out}(f_{out}) \approx V^{\star}_{out}(f_{out})\left\{D + \frac{1-D}{1+j2\pi f_{out}RC}\,\mathrm{sinc}\left(f_{out}(T_s-\tau)\right)e^{-j\pi f_{out}(T_s-\tau)}\right\}. \quad (28)$$

$f_{out} = f_{in}$ spans within the 1st Nyquist band $[0, f_s/2]$ in typical S/H uses. In a special case when f_{in} is low frequency near DC, the above equation further simplifies to

$$V_{out}(f_{out}) \approx V^{\star}_{out}(f_{out}). \quad (29)$$

With a practical design of the narrowband P-M, we can reasonably assume that $\tau \ll RC$, $f_{out} \ll 1/(2\pi RC) \ll f_{in}$, and $f_{out} \ll f_s$. Thus with the narrowband output f_{out} at baseband, the OFF state output voltage V_{off} is approximated as

$$V_{off}(f_{in}, f_{out}) \approx (1-D)V^{\star}_{out}(f_{in}, f_{out}). \quad (30)$$

Since $1/(2\pi RC) \ll f_{in}$, the terms $V_{in}(f_{in})/(1+j2\pi f_{in}RC)$ both in $\hat{V}_{ss}$ and $\hat{V}_{tran}$ are heavily attenuated and have negligible contributions. Thus $\hat{V}_{ss} \approx 0$, and $\hat{V}_{tran}$ is approximated using $\exp(-\tau/(RC)) \sim 1-\tau/(RC)$ as

$$\hat{V}_{tran}(f_{in}, f_{out}) \approx DV^{\star}_{out}(f_{in}, f_{out}). \quad (31)$$

Thus, from (23) the entire continuous output waveform in frequency domain is given by

$$V_{out}(f_{in}, f_{out}) \approx V^{\star}_{out}(f_{in}, f_{out}). \quad (32)$$

Therefore, both in S/H and P-M modes, when the output frequency is a low frequency at baseband, the transfer functions from the input to the f_{out} component in the output continuous waveform are approximated with the same transfer functions for discrete-time outputs as follows:

$$H_{S/H}(j\omega_{in}) \approx H^{\star}_{S/H}(j\omega_{in}) \quad \text{and} \quad (33)$$

$$H_{P\text{-}M}(j\omega_{in}, j\omega_{out}) \approx H^{\star}_{P\text{-}M}(j\omega_{in}, j\omega_{out}), \quad (34)$$

where $H^{\star}_{S/H}$ and $H^{\star}_{P\text{-}M}$ are given by (10) and (13), respectively.

3.2.2 Extraction of f_{in} Component

To calculate a driving-point impedance, which has been detailed in [36], we need to derive the f_{in} component of the output voltage $V_{out}(f_{in})$. As in the case for f_{out} extraction f_{in} components of V_{off} and $\hat{V}_{tran}$ are given simply by replacing f with f_{in} in (15) and (22). For $V^{\star}_{ss}$ and $\hat{V}_{ss}$, we replace ζ in (20) and (17) with 0 to have f_{in} component. With no approximations, from (23) we have

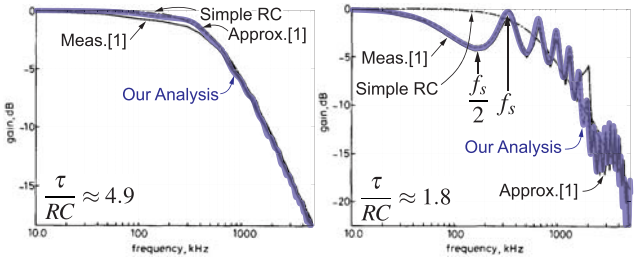
$$V_{out}(f_{in}) = \frac{V_{in}(f_{in})}{1+j2\pi f_{in}RC}\{D + (1-D)\,\mathrm{sinc}(f_{in}T_s(1-D))e^{-j\pi f_{in}(T_s-\tau)}H^{\star}(j\omega_{in})\}, \quad (35)$$

where $H^{\star}(j\omega_{in})$ is given by (9). The first term of the above equation corresponds to the steady-state output waveform for switch-ON period, and the second term to the RC-filtered waveform of the zero-order held version of the sampled voltages for switch-OFF period.

4. Experimental Comparison

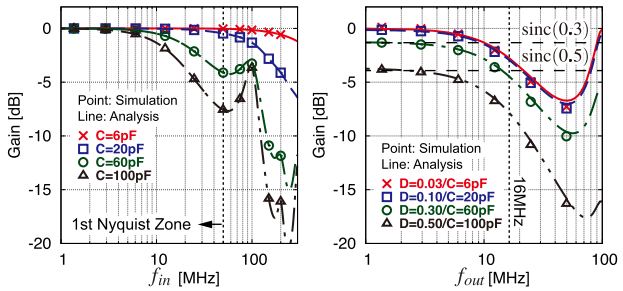
First, we verify the accuracy of the unified FET-R-C transfer function in (9) by comparing it with measurements presented in [1, Fig. 10], which plot the frequency response with a fixed RC time constant and two different switch-ON periods τ. Figure 17 compares the frequency response from our unified transfer function with measured results for $R = 1250\,\Omega$, $C = 180\,\mathrm{pF}$, and $f_s = 340\,\mathrm{kHz}$. Figure 17(a) uses $\tau = 1.1\mu\mathrm{s}$, which corresponds to the S/H mode because $\tau/(RC) \approx 4.9$; (b) uses $\tau = 400\mathrm{ns}$ when $\tau/(RC) \approx 1.8$, which places the operation closer to P-M mode. In these figures, the gain calculated by (9) is overlaid with solid thick lines on top of the curves from [1]. In the case of (a), the FET-R-C transfer characteristic closely follows a simple RC lowpass filter, as expected from our analysis. In the case of (b), on the other hand, a ripple characteristic is expected due to the non-negligible $\exp(-\tau/(RC))$ terms in the pre- and post-filters. The complete agreement with the measurement results proves the accuracy of our analysis.

Next, we compare our analysis with periodic steady-state simulation in Spectre RF [45]. For the simulation, we used the circuit of Fig. 1(b) with an ideal switch, a voltage source, a resistor, and a capacitor. Figures 18(a) and (b) plot the transfer function for S/H and P-M modes calculated using (9) with lines, and the simulation results with points.



(a) (b)

Fig. 17 Gain of the FET-R-C circuit calculated from compared with the measurement results in [1]. Our analysis results are overlaid on his measurement results for (a) wider pulse width example and (b) narrower pulse width example. © 2016 IEEE.



(a) (b)

Fig. 18 Gain calculated from (9), compared with simulation when $R = 50\,\Omega$, $R_L = \infty$. (a) S/H mode example with $f_s = 100\,\text{MHz}$, $f_{out} = f_{in}$, and $D = 0.5$. (b) P-M mode example with $f_s = 100\,\text{MHz}$, $f_{in} = Mf_s + f_{out}$, and $M = 1$. $D/(RC)$ is held constant at $2\pi \times 16\,\text{Mrad/s}$. © 2016 IEEE.

$R = R_s + R_{on} = 50\,\Omega$ is used. The sampling frequency is $f_s = 100\,\text{MHz}$ for convenience. In Fig. 18(a) D is fixed to 0.5 for the S/H example as the sampling capacitance C is varied from 2 pF to 100 pF to shrink the RC bandwidth progressively. When C becomes larger than 60 pF, ripple appears in the transfer characteristics as $\exp(-\tau/(RC))$ becomes non-negligible. This now departs from an ideal S/H. In Fig. 18(b), the input frequency is $f_{in} = M \cdot f_s + f_{out}$ where $f_s = 100\,\text{MHz}$ and $M = 1$, assuming use as a passive sampling mixer is intended. This graph plots the results by changing both capacitance C and duty cycle D while keeping the effective bandwidth of the P-M constant, $D/(2\pi RC) \approx 16\,\text{MHz}$ (see (13)). It is seen that the −3dB bandwidth in all cases remains constant at 16 MHz and the gain to an output translated in frequency to DC is sinc(D). In both S/H and P-M cases, these comparisons show complete agreement between simulation and analysis.

5. Conclusion

This paper has presented a useful design-oriented analysis of FET-R-C circuits. A simple signal flow graph (SFG) captures the FET-R-C circuit's action completely across a wide range of parameters. Based on our analysis, the FET-R-C circuit behavior may be understood as the cascade of three filtering functions interposed with an ideal sampling action. The SFG pinpoints where the sampling action is located among these filters, thus precisely describing the signal transfer characteristic including frequency translation. It becomes clear how, by changing parameter values, the same circuit can work as either a wideband S/H or as a bandpass P-M. The signal transfer characteristic of the single-path FET-R-C circuit has been described and verified by circuit simulations and comparisons with published measurements. The waveform reconstruction procedure for the complete waveform from the discrete-time sampled voltage has been described in detail.

Acknowledgments

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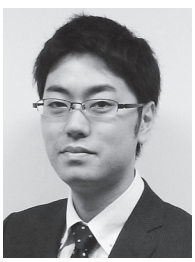

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