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Column-Parallel ADCs for CMOS Image Sensors and Their FoM-Based Evaluations

Shoji KAWAHITO[†a)], ***Member***

SUMMARY This paper reviews architectures and topologies for column-parallel analog-to-digital converters (ADCs) used for CMOS image sensors (CISs) and discusses the performance of CISs using column-parallel ADCs based on figures-of-merit (FoM) with considering noise models which behave differently at low/middle and high pixel-rate regions. Various FoM considering different performance factors are defined. The defined FoM are applied to surveyed data on reported CISs using column-parallel ADCs which are categorized into 4 types; single slope, SAR, cyclic and delta-sigma ADCs. The FoM defined by (noise)^2(power)/(pixel-rate) separately for low/middle and high pixel-rate regions well explains the frontline of the CIS' performance in all the pixel rates. Using the FoM defined by (noise)^2(power)/(intrascene dynamic range)(pixel-rate), the effectiveness of recently-reported techniques for extended-dynamic-range CISs is clarified.

key words: *CMOS image sensor, column-parallel ADC, cyclic ADC, delta-sigma modulation, single-slope ADC, SAR ADC, figure of merit*

1. Introduction

Since the beginning of 2000s, the major image sensor products have been gradually shifted from CCD (charge coupled device) image sensors to CMOS image sensors (CISs). Currently, more than 95% of image sensors are produced with CIS technology. The shifting of image sensor technology from CCD to CMOS is regarded as an evolution from "ANALOG" to "DIGITAL" in imaging semiconductor devices. Current CMOS image sensors often use an image signal readout architecture using column-parallel analog-to-digital converters (ADCs) [1]–[78]. The column-parallel ADC allows us to read out image signals from the pixel array with less noise and higher bandwidth (or higher pixel rate) to process them with on-chip sophisticated digital image processing circuits and to transfer the image data to outside at very high pixel rate with no degradation of signal quality. In CCD image sensors which use analog signal readout from the chip meeting high bandwidth and low noise simultaneously is the most difficult task. Because the column-parallel ADC is a key element for CISs the performance of CISs is often dominated by the architectural choice of the column-parallel ADC. Figure 1 shows an example of layout pattern of a CIS and a column-parallel cyclic ADC used in the CIS chip. To implement the ADC at the column of fine-pitched pixel array of the CIS, the ADC elements must be embedded into the narrow column (e.g., width of 5.6μm in Fig. 1) and arranged as an array of many elements (e.g., 824 elements in Fig. 1). The ensemble of all the ADC elements provides very high image data rate for the image signal readout while maintaining the speed (bandwidth) of the ADC operation at each column to be very low. The overall performance of designed CISs is maximized by exploiting these features of column-parallel ADCs. At the same time, the choice of the column-parallel ADC and the design of it must be carefully done because the ADC must be designed under very sever constraints due to the fine column pitch.

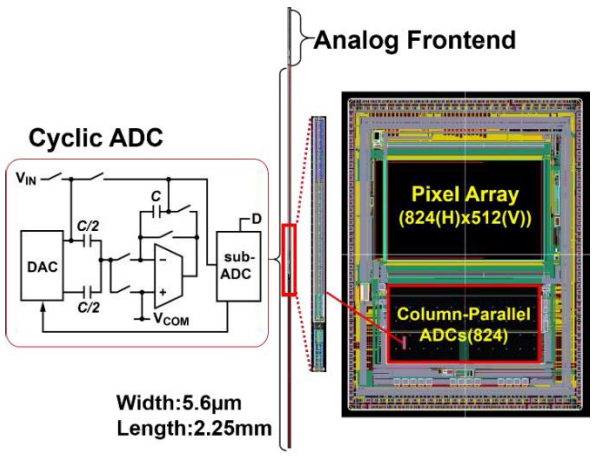

Fig. 1 CMOS Image Sensor and a column-parallel ADC.

The aim of this paper is to review architectures and topologies for column-parallel ADCs reported and discuss how the right ADC type is chosen depending on the specification of the CISs. To do this, new models for evaluating the column-parallel ADC performance are proposed and figures of merit (FoM) based on the models are defined. The validity of the FoM defined are examined by applying the FoM to the performance data of CISs reported.

2. CMOS Image Sensors and Requirements for Column-Parallel ADCs

2.1 CIS Architecture

A typical block diagram of CISs is shown in Fig. 2 (a). A column-parallel ADC, a 1-D array with many ADC elements is placed at the bottom of the pixel array. Each ADC element receives a pixel output signal through a vertical signal line and converts the analog signal to a digital signal at

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[†]The author is with Research Institute of Electronics, Shizuoka University, Hamamatsu-shi, 432–8011 Japan.
a) E-mail: kawahito@idl.rie.shizuoka.ac.jp
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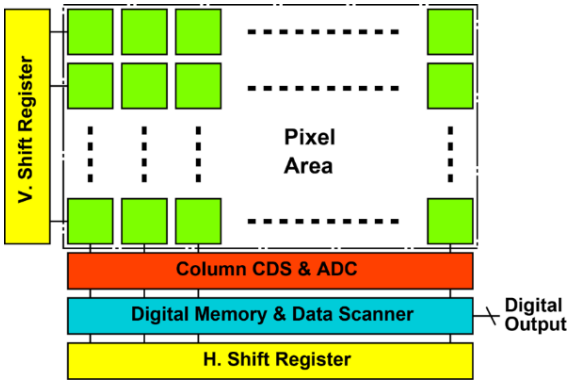
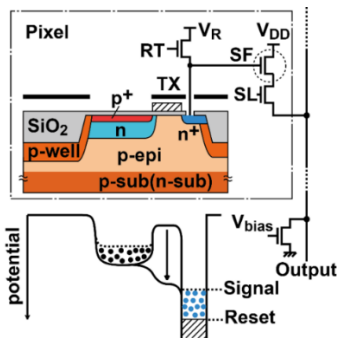
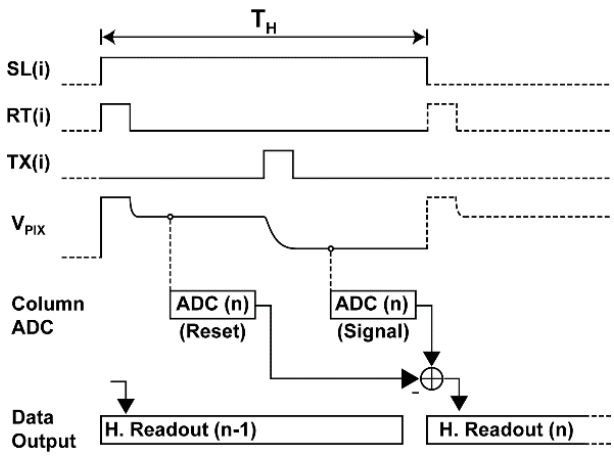


(a) Block diagram of a typical CMOS Image Sensor (CIS)



(b) CIS pixel and operation



(c) Operation timing for CDS, ADC and horizontal data transfer.

Fig. 2 CIS, column-parallel ADC, and operation timing.

the front-end part of the column readout circuits. A typical pixel diagram of CISs is shown in Fig. 2 (b). The CIS pixel consists of a pinned photodiode and 4 transistors for an amplifier (source follower), resetting, selecting and charge transferring. The signal readout timing diagram is shown in Fig. 2 (c). One readout cycle of reading a set of pixels for the *i*-th row consists of (1) selecting the pixel (SL(i):High), (2) resetting the charge sensing node (RT(i):High), (3) sampling and A/D conversion for the reset level of the pixel output, (4) photo-charge transfer from a photodiode to the charge sensing node (TX:High), (5) sampling and A/D conversion for the photo-signal level of the pixel output, and (6) digital correlated double sampling (CDS) for pixel noise cancelling. The image data for each column is once stored in a memory and the data is scanned horizontally in the time slot of the next readout cycle for reading the data of one row to the outside of the sensor chip.

Table 1 T_H, R_p, and R_b of high-definition video imaging (Aspect ratio = 16 : 9, N_B = 12 [bit], r_{VO} = 0.01, r_{HO} = 0.02)

	HD (720p)	FHD (1080p)	QHD (1440p)	4K (2160p)	8K (4320p)		
Pixel #(H)	1280	1920	2560	3840	7680		
Pixel #(V)	720	1080	1440	2160	4320		
Frame Rate[fps]	60	60	60	60	60	120	480
T_H [μs]	22.9	15.3	11.5	7.6	3.8	1.9	0.48
R_p[GHz]	0.06	0.13	0.23	0.51	2.05	4.1	16.4
R_b[Gbps]	0.7	1.5	2.7	6.2	24.6	49.2	197

2.2 Requirements for Column-Parallel ADC

In CMOS image sensors with N_v (# of vertical pixels) x N_H (# of horizontal pixels) pixels, the readout cycle time of one row, T_H is given by

$$T_H = \frac{1}{N_V(1 + r_{VO})f_f} \tag{1}$$

where r_{VO} is the factor of blanking time for vertical header codes and vertical optical black and f_f is the frame rate. The pixel rate, which is the required rate of reading all the pixels within a given frame rate is expressed as

$$R_p = N_H N_V(1 + r_{VO})(1 + r_{HO})f_f \tag{2}$$

where r_{HO} is the factor of blanking time for horizontal header codes and horizontal optical black. If each pixel has an N_B-bit gray-scale levels using N_B-bit A/D conversion, the output bit rate is given by

$$R_b = N_B N_H N_V(1 + r_{VO})(1 + r_{HO})f_f \tag{3}$$

In Table 1, typical values of T_H, R_p, and R_b in high-definition video imaging is summarized. Never-ending demands for better quality and reality in imaging require image sensors and column-parallel ADCs with extreme performances. For instance, in full-spec 8K image sensors with the frame rate of 120fps, one horizontal readout cycle time of $< 2\mu$s is required and the time for A/D conversion in the column ADC must be $< 1\mu$s if two times of the A/D conversion are carried out for the digital CDS. Special demands for slow-motion playback in 8K featuring a frame rate of 480fps requires further faster A/D conversion. The choice of ADC architecture, circuit topology for that and design effort are very important task for the developments of image sensors with these extreme specifications.

2.3 Technology Factors Relevant to the Evaluation of CISs and Column-Parallel ADCs

Recent progress of CIS process and device technology

greatly improve the performance of CISs, and it influences the architectural choice of the column parallel ADCs. For the performance evaluation of a column-parallel ADC and the CIS using it, knowing what process/device technology factors are used is necessary in order to examine the reason of the improvements. These technology factors are as follows:

[A] Process Node

A fine process technology contributes to the performance of the CIS and column-parallel ADC, particularly for low-power consumption in digital-rich types of ADCs.

[B] Backside Illumination (BSI)

For attaining high quantum efficiency in CISs with fine pixel pitch, backside illumination (BSI) structures have been introduced since around the middle of 2000s. The BSI can contribute not only to enhance the sensitivity but also to improve the interconnection capability between the pixel array and the peripheral circuit area. This is because the BSI allows to use all the areas on top of pixels for the interconnections. This greatly helps to improve the CIS performance if high pixel rate is required.

[C] 3D Stacking

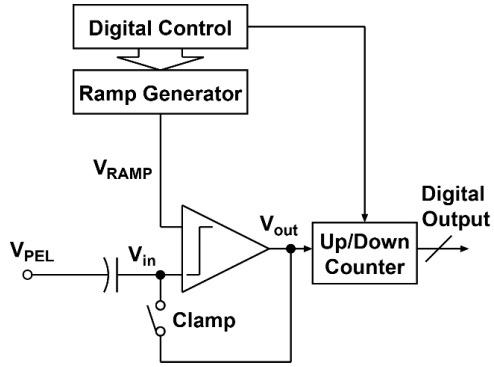
3D stacking technology introduced since around the beginning of 2010s, of course, greatly contributes to the performance improvements of CISs. The 3D stacking of a sensor layer and processing circuit layer allows us to attain efficient interconnections between the pixels and the column-parallel ADCs and also between the column-parallel ADCs and the processing circuits. Based on the 3D stacking, the major architecture of ADC may change from column parallel to pixel parallel in near future, and actually CISs with pixel-parallel ADCs with excellent performances have been reported [80]. In this paper, however, discussion is focused only on CISs using column-parallel ADCs.

[D] Global Shutter

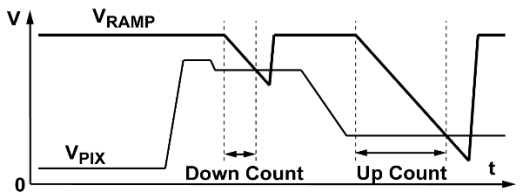
Developments of global-shutter CISs are becoming active recently. In the case of conventional rolling-shutter CISs, the architecture for reading pixel signals to the peripheral circuit area cannot be flexibly changed because of changing the order of reading pixel signals may cause a motion artifact. The use of global-shutter pixel may contribute to a flexible and efficient pixel signal readout architecture and a better resulting performance of CISs.

3. Architectures of Column-Parallel ADCs

Many different architectures and circuit topologies for column-parallel ADCs have been reported. The major architectures are categorized into 4 types; (a) single-slope ADC, (b) successive approximation ADC, (c) algorithmic- or cycle-based ADC, and (d) delta-sigma modulation ADC. In addition to these, recent CISs often employs column-parallel ADCs with extended intrascene dynamic range. In this section, principle, operation and feature of the typical column-parallel ADCs are reviewed.



(a) Schematic Diagram



(b) Timing Diagram

Fig. 3 Single-slope ADC for digital CDS using an up/down counter.

3.1 Single-Slope ADC

Figure 3 shows a typical single-slope ADC (SS-ADC) for column implementation [2], [9]. Single-slope ADCs are very popular for a column-parallel ADC in CISs because of its very simple circuit configuration and good linearity. At each column, a comparator and up-down counter only are necessary. The ramp-signal generator is common for all the columns. A ramp signal is applied two times for reset level and signal level as shown in Fig. 3 (b) and the two single-slope A/D conversions for the reset and signal levels are carried out by an up-counting and down-counting, respectively, using an up-down counter to perform a digital CDS so that the resulting output is the difference of them.

The time of the N_B-bit single-slope A/D conversion $T_{ADC,SS}$ for the signal level using a counting clock frequency of f_{CK} is given by

$$T_{ADC,SS} = \frac{2^{N_B} + C_{CDS}}{f_{CK}} \tag{4}$$

where C_{CDS} is a counting margin for doing the digital CDS. In the SS-ADC, the A/D conversion time for the reset level can be very small when compared with that for the signal level. To do this, auto-zeroing technique is used in the comparator as shown in Fig. 3 (b) to cancel the fixed pattern noise component of the reset level. Since the A/D conversion time of the SS-ADC is proportional to the exponential of N_B, a relatively long time is necessary particularly if high gray-scale resolution is required. In order to use the SS-ADC for a high-definition 12-bit CIS, a technique using very high counting clock is developed. In the 17.7Mpixel 120fps

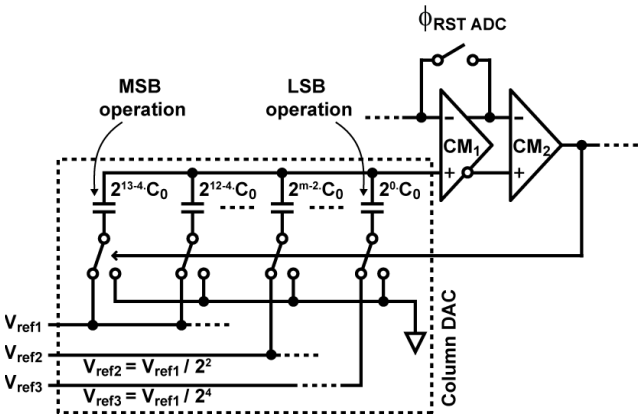
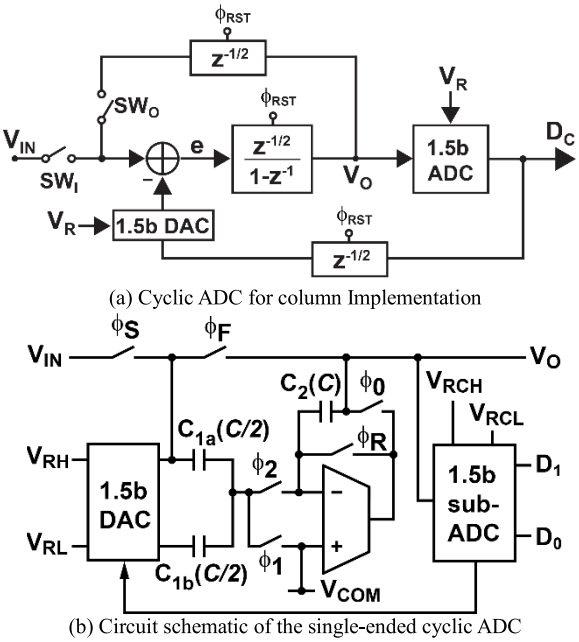


Fig. 4 DAC and Comparator for 14-bit SAR ADC for column implementation.



(a) Cyclic ADC for column Implementation

(b) Circuit schematic of the single-ended cyclic ADC

Fig. 5 Cyclic-based ADCs for column Implementation.

12b CIS [17], the counting clock frequency of 2.376GHz is used and 12-bit A/D conversion time of 1.72μs and T_H of 7.4 μs are attained.

In CISs using the SS-ADC, a comparator is an only analog component used at a column, and the power consumption of the CISs using the SS-ADC is believed to be relatively low. However, if high speed and high N_B are required, it should be also noted that the ramp-signal generator for delivering accurate ramp signal to all the columns and counters with high-frequency clocks consumes pretty large power. For faster and reduced counter clock frequency in single-slope ADCs, many two-step approaches have been investigated [12]–[14], [16]. Extra carefulness is necessary to use the two-step conversion if a good linearity comparable to the single-step single-slope ADC.

3.2 Successive Approximation ADC

A successive approximation ADC, or successive approximation register ADC (SAR-ADC) is useful as a column ADC if high-speed operation is required. SAR-ADCs using a capacitor-array DAC are widely used. A possible problem of the SAR-ADC is that large area is occupied by the capacitor-array DAC if high N_B is required. A technique to cope with this problem as shown in Fig. 4 is developed for a column-parallel 14-bit SAR-ADC [33]. In a straightforward 14-bit DAC, the ratio of maximum to minimum capacitances is 2^{13} : 1 and if the minimum unit capacitance is C_0, the total of 2^{14} elements each of which is C_0 are necessary. The DAC in Fig. 4 uses three reference voltages, and by applying smaller reference voltages ($1/2^2$ and $1/2^4$ of the largest reference voltage) to the LSB sides of operation, the maximum/minimum capacitor ratio is relaxed to 2^9 : 1, and this reduces the area required for the DAC to be $1/2^4$ of the straight-forward case if the same C_0 is used. The column SAR ADC consumes relatively low power because the comparator is an only component that consumes DC power in the column while attaining relatively fast conversion because N_B-bit A/D conversion is done by N_B steps.

In the column SAR-ADC, complicated switching circuits for the capacitor-array DAC must be implemented at the narrow column and very careful layout design is necessary for attaining specified linearity.

3.3 Cyclic ADC and Cyclic-based Pipelined ADC

For faster and higher N_B, the cyclic ADC or also called an algorithmic ADC is also a useful architecture for column ADCs. Though cyclic ADCs were recognized to be complicated circuits, a very-simplified cyclic ADC using the single-ended integrator-based circuits as shown in Fig. 5 (a) and (b) has been introduced [58] and it allows us to use the cyclic ADCs in a relatively narrow ADC array pitch [66]. A cyclic ADC consists of a low-resolution ADC (sub-ADC) whose digital outputs drive a low-resolution DAC to give a quantized analog estimate of the input. This DAC output is then subtracted from the input, which is amplified by gain of 2, to give a residue. The ideal relationship of the output of the i-th cycle and that of the previous cycle is given by.

$$V_o(i) = 2V_o(i-1) - D_C(i)V_R \tag{5}$$

where $D_C(i) \in \{-1, 0, 1\}$, $(i = 0, 1, \ldots, N-1)$ is the 1.5-bit code of the i-th cycle and V_R is the reference voltage which gives the full analog scale level of the ADC. The operation of the 1.5-bit ADC to produce $D_C(i)$ is described as

$$D_C(i) = \begin{cases} 1 & (V_o(i) \geq V_R/4) \\ 0 & (-V_R/4 < V_o(i) < V_R/4) \\ -1 & (V_o(i) \leq -V_R/4) \end{cases}. \tag{6}$$

At the first cycle, an analog input signal (V_{IN}) is given at the input by turning SW_I on (see Fig. 5 (a)), i. e., $V_o(0) = V_{IN}$., and since the second cycle, the integrator output is sampled and fed back to the input by turning SW_O on to perform

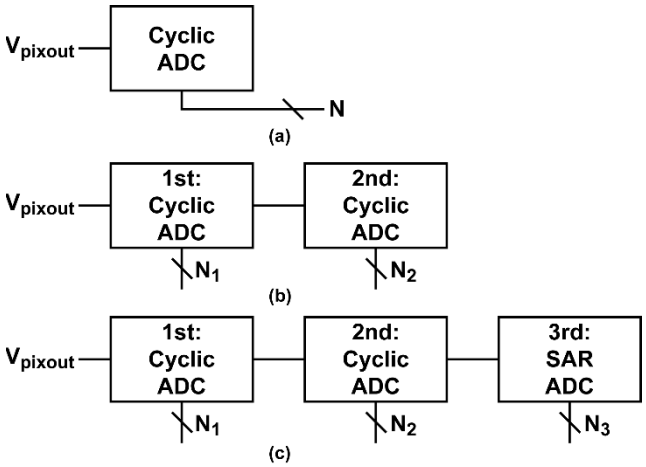


Fig. 6 Variations for Pipelined Multi-Stage Cyclic-based ADC

the cyclic or algorithmic A/D conversion given by Eq. (5). In this 1.5-bit cyclic ADC, $N_B - 1$ cycles give the resolution of N_B bits. Because of the gain of two at each cycle, the influence of the analog errors at latter cycles are relaxed. These property allows us to implement a high-speed column ADC with high resolution. For power-efficient design of the column cyclic ADC, the N_B-bit cyclic ADC is divided into two cyclic ADC stages for the former N_1 cycles and latter N_2 cycles where $N_1 + N_2 = N_B - 1$ as shown in Fig. 6 (b). These two stages are operated in a pipelined fashion by extending over the 2nd-stage conversion into the next horizontal readout cycle of the CISs. This technique effectively reduces the sampling rate of the ADC analog cores. The 2nd cyclic ADC stage receives the residue output of the 1st cyclic ADC where the gain of 2^{N1} is applied. This greatly relaxes the tolerance to the analog errors in the 2nd stage and allows us to design a power-efficient ADC with high sampling rate. This two-stage pipelined cyclic ADC is applied to a 1.3Mpixel 2000fps 12-bit CIS [61] and 33Mpixel 120fps 12-bit/14-bit CISs [65], [69] and extreme performances in high-speed camera and 8K broadcasting camera have been demonstrated. In the 12-bit CIS, the division into two cyclic ADCs to perform the first 4 cycles and the latter 8 cycles is the best of choice for the optimization of power efficiency, and the power efficiency of the designed two-stage cyclic ADC is 2.5-times better than that of the single-stage cyclic ADC. By dividing the cyclic-based ADC into three stages each of which is a low-resolution ADC and operating these in a pipelined fashion as shown in Fig. 6 (c), further power-efficient high-sampling rate design of the column ADC is possible. In this case, since the last low-resolution ADC stage does not need to generate an analog residue, a power-efficient SAR-ADC is used. This three-stage (Cyclic-Cyclic-SAR) ADC is applied to a 33Mpixel 240fps 12-bit CIS for 8K cameras with a function of slow-motion playback [71].

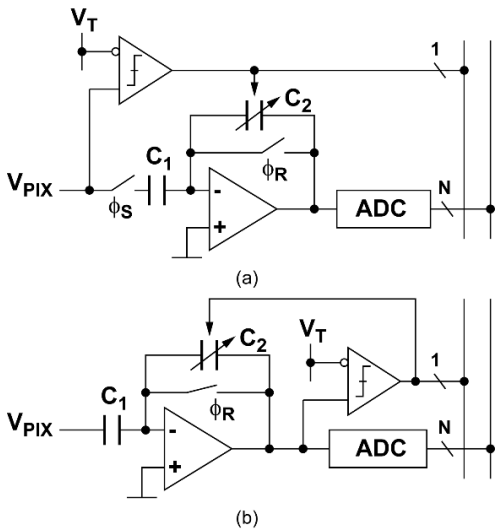


Fig. 7 Adaptive-Gain Amplification for Extended Dynamic Range

3.4 Column-Parallel ADCs for Extended Intrascene Dynamic Range

Noise reduction is one of the most important functions in readout circuits for CMOS image sensors. The input-referred noise of CMOS image sensors can be reduced by high-gain amplification at the frontend of readout circuits. However, the frontend amplification with high gain for noise reduction was conventionally done at the cost of reduced dynamic range. Recently, many techniques for noise reduction while maintaining the intrascene dynamic range have been reported. Adaptive-gain amplification as shown in Fig. 7 is one of effective ways for low-noise extended dynamic range CISs [23], [78]. The gain is given by C_1/C_2. In Fig. 7 (a), the pixel output is first compared with a given threshold of V_T and if the amplitude is smaller than V_T, large gain of 8, for instance, is used by setting $C_2 = C_1/8$. If the amplitude is larger than V_T, the gain of unity is used by setting $C_2 = C_1$. If V_T is chosen as 1/8 or a little smaller than the analog maximum range of the column ADC, a large gain of 8 is adaptively used for small amplitude pixel signal without saturating at the ADC input for an incidental large amplitude pixel signal. In Fig. 7 (b), the gain adaptation is done by looking at the amplifier output when the gain is set to high. If the amplitude of the amplifier output is larger than the threshold V_T, the amplifier output is limited by a limiting circuit (not shown in Fig. 7 (b)), and the gain of the amplifier is reset to unity.

There are a few other techniques for the column-parallel ADC with noise reduction while maintaining the intrascene dynamic range. A pseudo multiple sampling technique using a single-slope ADC samples the pixel output many times and averages their ADC outputs to produce a noise-reduced resolution-increased digital signal [15]. A dual-gain A/D conversion using a single-slope ADC and two slope gains to the same pixel output is also a simple and

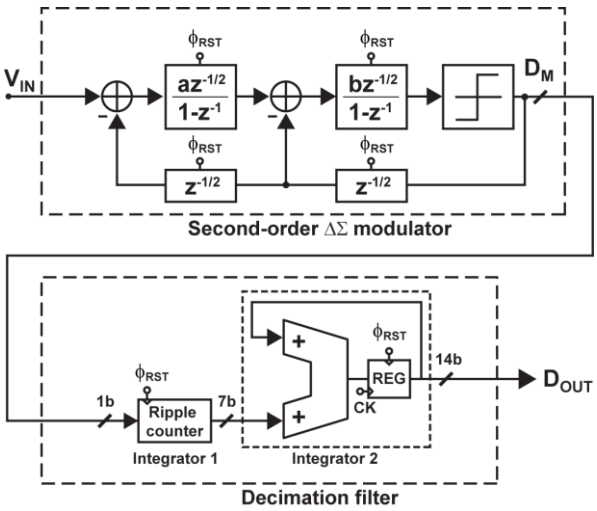


Fig. 8 2nd-Order Delta-Sigma ADC for column Implementation.

effective technique for obtaining reduced noise and extended intrascene dynamic range at relatively high pixel rate [20].

3.5 Delta-Sigma Modulation ADC

A/D Converters using over-sampling techniques are also very useful for column ADCs with noise reduction and extended dynamic range. A 2nd-order incremental delta-sigma modulator ADC as shown in Fig. 8 is of a reasonable choice because of the balance between the circuit complexity and the efficiency for noise shaping to obtain high gray-scale resolution [68]. In this type of circuits, the oversampling and low-pass filtering effect by the decimation filter has an effect of white noise reduction and an effect for extended dynamic range is self-contained. An issue for this 2nd-order delta-sigma modulator is that it requires many sampling clock cycles if very high bit-resolution is required. The bit-resolution, N_B is determined by the number of sampling clock cycles, M as follows:

$$N_B = \log_2 \frac{M(M+1)}{2} \text{ [bit]} \tag{7}$$

For N_B of 12, 14 and 16 bits, M of 90, 181 and 362 are required, respectively.

For more efficiently obtaining high bit-resolution with smaller number of sampling clock cycles, an ADC technique using 1st-order incremental delta-sigma modulator shown in Fig. 9 can be used. In this ADC, the first step for the 1st-order incremental delta-sigma modulation is done for the input with M sampling clock cycles and the second step for the residue output (integrator output) R_{OUT} in Fig. 9 is done by another N_{B2}-bit A/D converter. This type of A/D conversion is called an extended counting ADC [81]. The author calls this technique the folding-integration ADC [74] if this is used as a column-parallel ADC of CISs because the value of this ADC as used at the column of image sensors is due to the efficient noise reduction effect of the analog

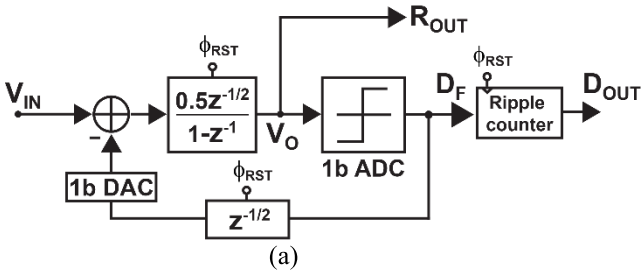


Fig. 9 First-order Incremental Delta-Sigma Modulator for Folding Integration (or Extended Counting).

integrator used in the delta-sigma modulation with multiple sampling of the input and the folding effect to maintain the amplitude of the integrator within an analog range determined by a amplitude of the 1-bit DAC. As a result, this ADC has an efficient noise reduction effect for both thermal noise and 1/f noise of in–pixel source-follower amplifiers and peripheral readout circuits while extending the dynamic range [83]. In this ADC, the bit-resolution is given by

$$N_B = \log_2 \frac{M}{2} + N_{B2} \text{ [bit]}. \tag{8}$$

With the help of a high-resolution ADC for the residue output, a very high-resolution column-parallel ADC is realized with smaller number of sampling clock cycles for the input. In the CIS chip using this ADC with 13-bit cyclic ADC for the residue output, maximally 19-bit resolution using M of 128 [73] and 17b DNL of +1.4LSB/−0.9LSB using M of 32 [75] has been demonstrated.

4. Definition of Figures of Merit of CMOS Image Sensors with Column-Parallel ADCs

For performance evaluation of CMOS image sensors using column-parallel ADCs, figures-of-merit (FoM) calculated with their specification and attained performance are useful. Though the aim of calculating the FoM is to evaluate mainly the performance of the column-parallel ADC, the merit of image sensor's entire performance is considered. The following FoM considering noise, power dissipation, and pixel rate is often used [85].

$$FoM_1 = \frac{Noise \times Power}{R_p} \times 10^9 [\mathrm{e}^- \cdot \mathrm{nJ}] \tag{9}$$

This FoM is useful for evaluating the performance of CISs if the power dissipation is proportional to the pixel rate and the noise is controlled independent of the pixel rate. However, such an assumption is not always met particularly if the pixel rate is very high and the dominant noise is thermal noise or other noise whose spectrum is spreading to high-frequency range.

FoM of more reflecting the noise behavior of CISs is defined here. The power consumption of CISs is mainly the sum of those of the pixel array, front-end amplifier if used, column ADC, column logic and I/O. All these components'

power consumption can be considered to be proportional to the horizontal pixel number, vertical pixel number and frame rate, i.e., their product or the pixel rate. Among the above, analog readout circuits like a front-end amplifier and column ADC are designed for reducing the power by optimizing the capacitor size C_T used for these analog circuits at the cost of thermal noise increase. Therefore, the power consumption of CISs is expressed as

$$Power = K_1 R_p + K_2 C_T R_p \tag{10}$$

where K_1 and K_2 are proportional constants.

The behavior of noise in CISs is complicated. If the pixel rate is low enough and the thermal or white noise components of the readout noise is controlled to be very low by using bandwidth limitation techniques, and then the temporal readout noise is dominated by 1/f noise of MOS transistors of the in-pixel source follower and it can be regarded as independent of the pixel rate. However, if the pixel rate is relatively high, the signal bandwidth becomes higher and thermal noise due to MOS transistors used in the analog readout circuits may dominate. The thermal noise is band-limited by capacitors used for the analog readout circuits and the noise power or mean squared noise $\overline{V_{n,T}{}^2}$ is observed as a form of $K_3(kT/C_T)$ where K_3 is a constant, k the Boltzmann constant, T the absolute temperature and C_T the capacitance for bandwidth limitation. In very high pixel rate, for instance, which is required for full-spec 8K image sensors, other noise components may dominate the noise level. In CISs with column-parallel readout channels, the bandwidth is related to one readout cycle time of one row and the noise power if the noise source is white noise is expressed as

$$\overline{V_{n,S}{}^2} = K_4 S_N \frac{1}{T_H} \cong K_4 S_N N_V f_f \tag{11}$$

where S_N is the noise power spectrum density per unit frequency and K_4 is the proportional constant. In high pixel-rate image sensors of which the horizontal data scanning is done with a pipelined fashion as shown in Fig. 2 (c), one can assume that the dominant noise source is due to switching noise caused by high-speed digital data scanning and reading to the outside of the sensor chip. If such a noise source at each column is independent, or there is no noise correlations between columns, an assumption that the noise power spectrum density is assumed to be the sum of each noise power spectrum generated at each column and is proportional to the number of columns N_H, i. e.,

$$S_N = K_5 N_H \tag{12}$$

where K_5 is a proportional constant. Then the noise power is given by

$$\overline{V_{n,S}{}^2} \cong K_4 K_5 N_H N_V f_f = K_6 R_p \tag{13}$$

where K_6 is a proportional constant. By taking all the noise components into account, a general form of the CIS noise is expressed as

$$\overline{V_n{}^2} \cong K_3 \frac{kT}{C_T} + \overline{V_{n,F}{}^2} + K_6 R_p \tag{14}$$

where $\overline{V_{n,F}{}^2}$ is the mean squared noise mainly due to pixel's 1/f noise components of MOS transistors. In a situation that thermal noise dominates and the power dissipation is optimized for reducing thermal noise of amplifiers, the product of the mean squared noise (Eq. (14)) and power (Eq. (12)) is approximated as

$$\overline{V_n{}^2} \times Power \cong K_3 \frac{kT}{C_T} \times K_2 C_T R_p = K_7 R_P \tag{15}$$

where K_7 is a proportional constant. At low pixel rate, if the pixel 1/f noise dominates, the squared noise-power product is expressed as

$$\overline{V_n{}^2} \times Power \cong \overline{V_{n,F}{}^2} \times (K_1 R_p + K_2 C_T R_p) = K_8 R_P \tag{16}$$

where K_8 is a proportional constant. The situations of Eq. (16) and Eq. (15) are met for low and relatively-high pixel-rate CISs, respectively. At very high pixel rate where the digital-system noise dominates, the mean squared noise-power product is expressed as

$$\overline{V_n{}^2} \times Power \cong K_6 R_p \times (K_1 R_p + K_2 C_T R_p) = K_9 {R_P}^2 \tag{17}$$

where K_9 is a proportional constant. These observations suggest us a new definition of FoM. For the pixel rate below R_{pc} where R_{pc} is the corner pixel rate for the FoM model change, the FoM given by

$$FoM_{2L} = \frac{Noise^2 \times Power}{R_p} \times 10^9 [(\mathrm{e}^-)^2 \cdot \mathrm{nJ}] \tag{18}$$

should be used and if the CIS is evaluating at high pixel rate ($> R_{pc}$), the FoM defined as

$$FoM_{2H} = \frac{Noise^2 \times Power}{{R_p}^2} \times 10^9 [(\mathrm{e}^-)^2 \cdot \mathrm{nJ/GHz}] \tag{19}$$

should be used.

If attaining high intrascene dynamic range (*IDR*) valuable for CISs, an FoM defined as

$$FoM_{3L} = \frac{Noise \times Power}{IDR \times R_p} \times 10^{12} [\mathrm{e}^- \cdot \mathrm{pJ/DRU}] \tag{20}$$

should be used if the pixel rate is not very high, where DRU (dynamic range unit) is a unit of calculating the *IDR* given by

$$IDR = \frac{Signal_{Max}/AG}{Noise}\ [\mathrm{DRU}] \tag{21}$$

where $Signal_{Max}$ is the maximum signal amplitude expressed as the number of electrons, and AG is the analog gain applied to attain the best of noise. The division by AG to calculate the *IDR* is because applying the analog gain of AG to reduce the noise in front of A/D conversion reduces the *IDR* by a factor of AG. If a technique for extending the IDR is used and the input-referred signal amplitude is maintained even if an analog gain AG is applied, the AG should

be set to unity in Eq. (21). This FoM is recently often used for evaluating CISs with introducing new techniques for extended dynamic range [20], [23], [82].

If the pixel rate is very high ($> R_{pc}$), the FoM given by

$$FoM_{3H} = \frac{Noise \times Power}{IDR \times {R_p}^2} \times 10^{12}[\mathrm{e}^- \cdot \mathrm{pJ/DRU} \cdot \mathrm{GHz}] \tag{22}$$

should be used instead of Eq. (20). The definition of the FoM in Eq. (20) is quite similar to the FoM used for evaluating stand-alone ADCs [84] where the FoM is defined as an idea that $(DynamicRange)^2 \times (Power)/(Bandwidth)$ of the ADC is constant if the ADC is designed by the same architecture, topology, and technology [84].

Another FoM considering the merit of high gray-scale resolution column ADC can be defined by the analogy from Eq. (20) as

$$FoM_4 = \frac{Noise \times Power}{ADR \times R_p} \times 10^{12}[\mathrm{e}^- \cdot \mathrm{pJ/Conv.\text{-}step}] \tag{23}$$

where ADR is the ADC code range and the conversion-step is a minimum step of the gray-scale levels. If an N_B-bit column ADC is implemented in the CIS, $ADR = 2^{N_B}$ (and the conversion-step = 1LSB) is used here.

5. FoM-Based Performance Evaluation of Column-Parallel ADCs for CISs

In order to check the validity of FoM defined in Sect. 4 and to evaluate the performance of column-parallel ADCs used in the actually implemented CISs, performance data of CISs papers presented and published at major international conferences (Int. Solid-State Circuits Conf. (ISSCC), VLSI Circuits Symp., Int. Image Sensor Workshop (IISW), European Solid-State Circ. Conf. (ESSCIRC)) and international journals (IEEE J. Solid-State Circ., IEEE Trans. Electron Devices, MDPI Sensors) are surveyed. CISs which employ column-parallel ADCs are picked up. The column-parallel ADCs are categorized into 4types, i.e., "Single-Slope" [1]–[24], "SAR" [25]–[42], "Cyclic" [43]–[66], and "Delta-Sigma" [67]–[78]. The group of ADCs using the 1st-order incremental delta sigma modulator and extended conversion for the residue output [73]–[78] is categorized in the "Delta-Sigma".

Figure 10 shows the noise versus pixel rate of CISs reported. Recently, techniques for extremely-low-noise CISs whose noise level is below 0.5e- have been reported. However, most of those are demonstrated with experimentally-implemented CIS chips, or quanta CIS using 1-bit ADC except for Ref. [78]. By excluding Ref. [78], one can observe that the front-line of noise level in low-noise CISs is around 1e- and it is constant up to the pixel rate of 600 to 700MHz. At very high pixel rate, as suggested by the model described in Sect. 4, attaining very low noise becomes difficult because

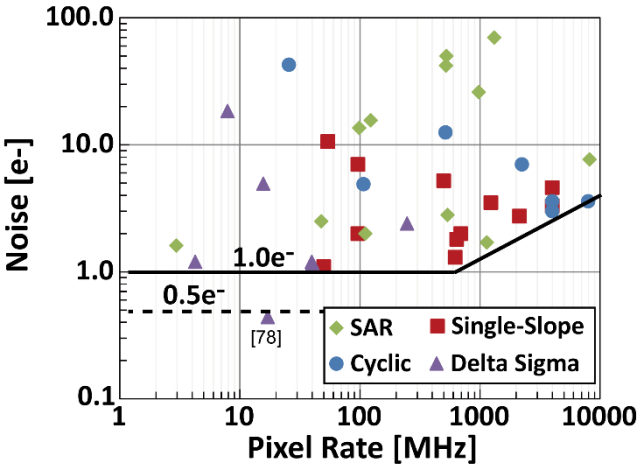


Fig. 10 Noise versus pixel rate plot of CISs reported

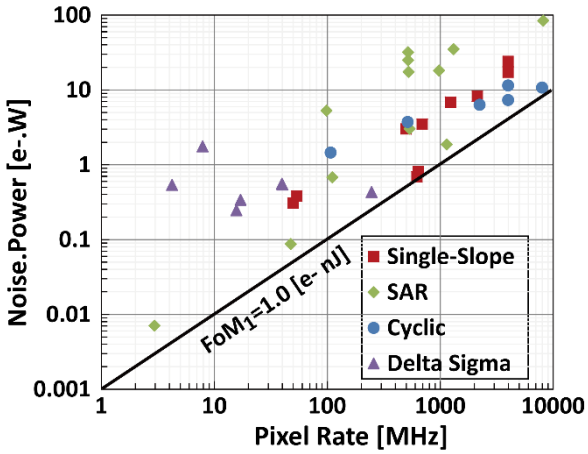


Fig. 11 Plot for common FoM (noise · power versus pixel rate).

of the noise generation due to high-speed digital signal readout which is done at the background of analog readout processing. According to Eq. (13), the noise is proportional to $\sqrt{R_p}$ in this region and this model looks valid in the pixel rate of above 700MHz in Fig. 10.

Figure 11 shows a plot for the evaluation based on the FoM commonly used, i.e., the plot of (noise)x(power) versus (pixel rate). The diagonal line shows FoM_1 defined in Eq. (9). The front-line of the best FoM in this definition is currently around 1.0 [e- nJ]. This FoM looks valid for rough observation of the progress of CIS technology because the best FoM at different pixel rates are well aligned in the line for the FoM_1.

Figure 12 shows a plot of $(\mathrm{noise})^2$x(power) versus (pixel rate). The diagonal line in the region of pixel rate of < 700MHz shows FoM_{2L} defined in Eq. (18). The front-line of the best FoM in this definition is currently around 1.5 $[(\mathrm{e}\text{-})^2$ nJ] due to the development of CISs of Ref. [23] reported in 2017 which uses a global shutter pixel and dual-gain amplified single-slope ADC and Ref. [20] reported in 2015 which uses BSI, 3D-Stacking, and a single-slope ADC. Be-

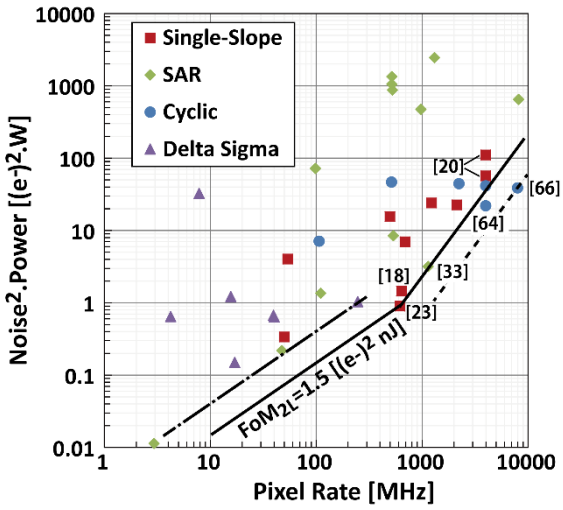


Fig. 12 Plot for FoM2 (noise^2 · power versus pixel rate).

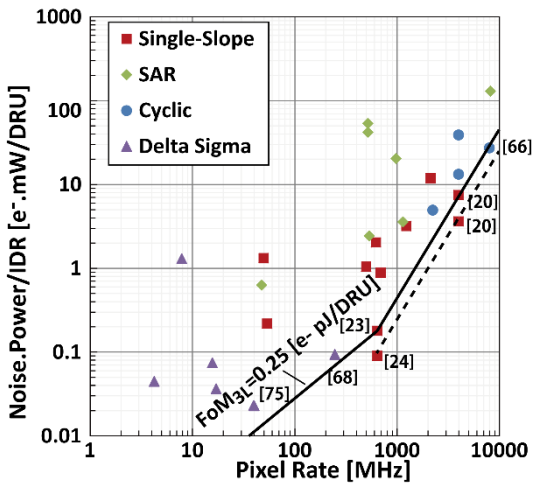


Fig. 13 Plot for FoM3 (noise · power/intrascene-DR versus pixel rate).

fore these development, the front-line looks around 4 [(e-)^2 nJ]. For higher pixel-rate region (~> 1000MHz), the FoM_{2H} defined in Eq. (19) well explains the front line if a CIS using BSI, 3D-Stacking and a 3-Stage pipelined cyclic-based ADC in Ref. [66] is excluded.

Figure 13 shows a plot of (noise) x (power)/(intrascene dynamic range) versus (pixel rate). The diagonal line in the region of pixel rate of < 700MHz shows FoM_{3L} defined in Eq. (20). The frontline of the best FoM in this definition is currently around 0.25 [e- pJ/DRU], and the CISs of Ref. [23] using dual-gain adaptive amplification and Ref. [68] using incremental 2nd-order Delta-Sigma ADC are on the frontline. The data of Ref. [24] is obtained by the same CIS chip in Ref. [23]. Because it is not clear the reason why two-times better FoM than that in Ref. [23] is obtained in spite of using the same chip and same operation, the data point of Ref. [24] is once excluded in the discussion here. For higher pixel-rate region (~> 1000MHz), the FoM_{3H} defined in Eq. (22) well explains the frontline. In this region, the CIS

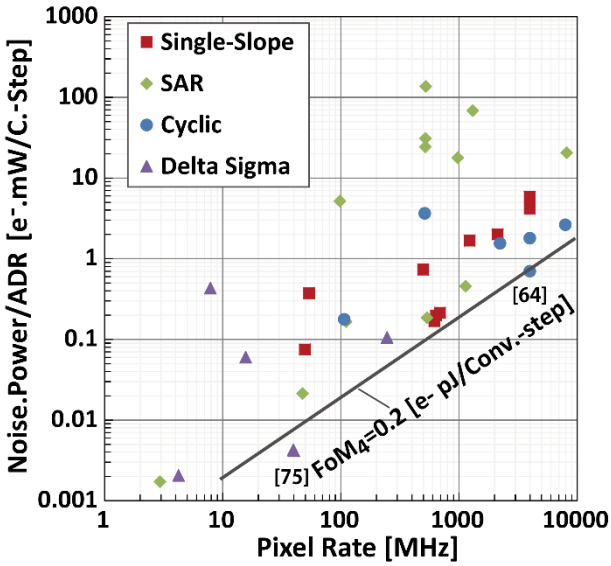


Fig. 14 Plot for FoM4 (noise · power/gray-scale-range versus pixel rate)

of Ref. [20] using a global shutter, 3D-stacking at peripheral area, and adaptive dual-slope ADC is on the frontline. The CIS in Ref. [66] using BSI, 3D-stacking and a 3-stage pipelined cyclic-based ADC is also on the frontline. From these observation, we can conclude that column ADC architectures using techniques for extending dynamic range described in Sect. 3 are all successful for attaining totally well-balanced high performance considering factors of low noise, low power dissipation, high dynamic range, high frame rate and high resolution (large pixel number).

Figure 14 shows a plot of (noise) x (power)/ (ADC code range) versus (pixel rate). In this metrics, the value of obtaining high gray-scale resolution is stressed and the CISs using 14-bit cyclic [64] and 17-bit delta-sigma [75] ADCs are on the frontline of this definition of FoM, i. e., FoM_4 for the regions of both high and low pixel rates, respectively.

6. Conclusions

In this paper, column-parallel analog-to-digital converters for CMOS image sensors are reviewed and their performances are discussed using metrics calculated by figures of merit (FoM). Models for separately evaluating the performance of the CISs in low/middle and high pixel-rate regions are proposed and several FoM considering different performance factors are defined. The defined FoM are applied to surveyed data on CISs reported and the following conclusions are obtained:

- The performance of CISs should be evaluated with different metrics to high pixel-rate regions (~> 1000MHz) from those to low or middle pixel-rate regions.
- The conventional FoM (commonly-used FoM) calculated by (noise) x (power) /(pixel-rate) is useful for observing entirely the trend of performance frontline of CISs.
- The FoM calculated by (noise)^2 x (power) /(pixel-rate) which considers a model on thermal noise and digital sys-

tem noise well explain the frontline technologies separately in low/middle and high pixel-rate regions.
- The FoM calculated by (noise) x (power)/ (intrascene dynamic range)/ (pixel-rate) well explains the effectiveness of the recently-reported techniques for extending dynamic range.
- The FoM calculated by (noise) x (power)/ (gray-scale range)/ (pixel-rate) is useful for evaluating the value of having high gray-scale resolution, and cyclic-based and delta-sigma ADCs are on the frontline for high and low pixel-rate regions, respectively.

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Shoji Kawahito received the Ph.D. degree from Tohoku University, Japan in 1988. He is a Professor at Shizuoka University since 1999 and a co-founder and the CTO of Brookman Technology Inc. established in 2006. He has published over 300 papers in peer-reviewed journals and international conference proceedings. He holds 89 Japanese Patents and 55 US Patents. Dr. Kawahito has received plenty of awards including the Walter Kosonocky Award in 2013, the JST President Award for leading the success of university-spin-off venture company in 2014, and IEICE Electronics Society Award in 2010. He is an IEEE Fellow and an ITE Fellow. He has served as the TPC chair of the 2011 and 2017 IISW and the chair of the IEEE SSCS Japan Chapter in 2013 and 2014 and a TPC member of the ISSCC from 2009 to 2012.