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Heteroepitaxial Growth of GaAs/Ge Buffer Layer on Si for Metamorphic InGaAs Lasers*

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SUMMARY We demonstrate heteroepitaxial growth of GaAs/Ge buffer layers for fabricating 1.3-μm range metamorphic InGaAs-based multiple quantum well (MQW) lasers in which the Ge buffer layer is grown using a metal-organic Ge precursor, iso-butyl germane, in a conventional metal-organic vapor phase epitaxy reactor. This enables us to grow Ge and GaAs buffer layers in the same reactor seamlessly. Transmission electron microscopy and X-ray diffraction analyses indicate that dislocations are well confined at the Ge/Si interface. Furthermore, thermal-cycle annealing significantly improves crystalline quality at the GaAs/Ge interface, resulting in higher photoluminescence intensity from the MQWs on the buffer layers.
key words: *heteroepitaxial growth, Ge buffer, MOVPE, Si substrate*

1. Introduction

As silicon is an inefficient light source material because of its indirect bandgap, integration of III-V compound semiconductor materials (e.g. GaAs, InP, and their alloys) is seen as a way of realizing highly integrated photonic circuits. Direct growth of high-quality III-V layers on Si substrate is the key to low-cost and large-scale fabrication of efficient light sources in photonic integrated circuits. However, a major issue has been high-density dislocations in the III-V layer on Si due to the lattice constant mismatch (~4% with GaAs, ~8% with InP). To avoid this problem, Ge buffer layers have been placed between the GaAs layer and Si substrate because the lattice constants of Ge and GaAs are almost the same [1]–[7], while epitaxial growth of Ge layers on Si substrate has been studied in connection with fabrication of photodetectors [8]–[10]. This method is compatible with the standard silicon-based complementary metal-oxide-semiconductor (CMOS) process. A lot of effort has gone into reducing the threading dislocation density (TDD) of Ge epitaxial layers on Si substrate by using selective area growth [10]–[12], cyclic annealing [10], [12], etc.; the TDD has been reduced from $\sim 10^9$ to $\sim 10^7$ cm^{-2} or less. Moreover, GaAs layers on Ge have also been widely studied. GaAs-on-Ge-based high-efficiency photovoltaics for space applications have been developed [13], [14]. Furthermore, several research groups have developed laser diodes (LDs) on Si substrate by using Ge buffer layers with InAs quantum dots (QDs) [3], [5]–[7]. These LDs exhibited high output power with a relatively long cavity around 1 mm [3], [7], which is suitable for use in conjunction with modulators. However, for datacom applications, it is crucial to reduce the cavity length so that the LDs can be used as directly modulated LDs (DMLs) in order to suppress power consumption and to enhance bandwidth. Indeed, DMLs with cavity lengths less than 200 μm are widely used in this application [15], [16]. In this context, we have to develop multiple quantum well (MQW) lasers on Si because there are difficulties shortening the cavity length of the QD lasers due to their small modal volume.

For datacom applications with a 2-km reach, it is important to develop 1.3-μm range lasers with single mode lasing. One candidate is an InP-based MQW laser on Si. However, the large lattice constant mismatch of ~8% makes it difficult to achieve high-quality active layers. To overcome this problem, we have proposed an InGaAs-based MQW LD structure using a GaAs/Ge buffer layer on Si substrate, as shown in Fig. 1. To elongate the emission wavelength of the MQWs to 1.3 μm, the GaAs/Ge/Si structure incorporates an InGaAs metamorphic buffer layer. The details of the metamorphic buffer and performance of the LDs on GaAs substrate are described elsewhere [17]–[19].

In this paper, we describe heteroepitaxial growth of GaAs/Ge layers on Si substrate by using metal organic vapor phase epitaxy (MOVPE) system that is used for making commercial lasers. Note that all of the previous LDs on GaAs/Ge/Si structures were grown using different equipment; chemical vapor deposition (CVD) for the Ge buffer layer growth and molecular beam epitaxy (MBE) for the AlGaAs/GaAs. When we use a conventional MOVPE reactor, sometimes it is difficult to introduce monogermane (GeH_4) widely used in CVD system as a Ge precursor since GeH_4 is a self-decomposable and explosive material. There are some reports on using metal-organic Ge precursors such as tert-butyl germane [20] and iso-butyl germane (IBGe) [21]–[23]; these materials can be easily introduced into MOVPE systems. We used IBGe as a precursor to fabricate Ge buffer layers and conventional precursors (TEGa, TMIn, and AsH_3) for III-V compound semiconductors. We obtained a low TDD Ge buffer layer by employing post-growth annealing. Cyclic annealing improved the crystalline quality of the interface between the GaAs and Ge buffer layers. These growth and annealing tech-

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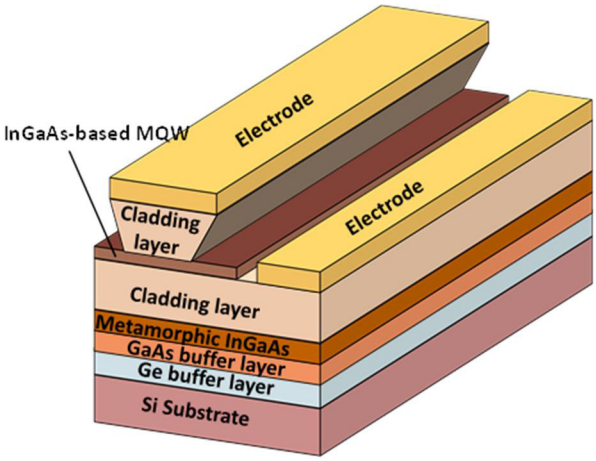

Fig. 1 Proposed LD structure

niques enabled us to obtain strong photoluminescence from InGaAs/GaAs MQWs on Si substrate.

2. Experiment

The Ge and GaAs buffer layer were grown on Si substrate in a MOVPE system. To avoid generating antiphase domains (APDs), we used a 2" Si (100) substrate with several degrees (4 or 6°) of misorientation toward the [111] direction [24]–[26]. Before MOVPE growth, the Si substrate was dipped into diluted HF solution to remove the native oxide. It was put into the MOVPE reactor immediately after that.

The growth sequence for the Ge and GaAs buffer layers is illustrated in Fig. 2. The sequence consists of three parts; (1) thermal cleaning, (2) 1st and 2nd Ge buffer layer growth and annealing, and (3) GaAs buffer layer growth. The thermal cleaning of the substrate was performed above 900°C at 70 torr in an H_2 atmosphere for 20 min to remove the remaining native oxide and form a double-stepped Si surface. After thermal cleaning, the substrate was cooled down to 400°C and the 1st 600-nm-thick Ge buffer layer was grown using IBGe. This relatively low growth temperature for the 1st Ge buffer layer was chosen in order to suppress three-dimensional growth. The grown Ge buffer layer was annealed for 20 mins at various temperatures ranging from 650 to 880°C in an H_2 atmosphere. After that, Ge buffer layer growth and annealing were performed again. A GaAs buffer layer was then grown on the Ge buffer layer at 500°C. AsH_3 and TEGa were used as the group V and III material sources, respectively. AsH_3 was introduced into the MOVPE reactor 5 mins prior to GaAs growth in order to make an As-terminated Ge layer surface.

After the GaAs/Ge buffer layer growth, we conducted thermal cycle annealing (TCA) to enhance dislocation bending and annihilation [27]–[29]. Moreover, we grew InGaAs/GaAs MQWs on the GaAs/Ge buffer layer to estimate the crystalline quality from their photoluminescence (PL).

The surface morphologies of the Ge and GaAs buffer layers were characterized by scanning electron microscopy

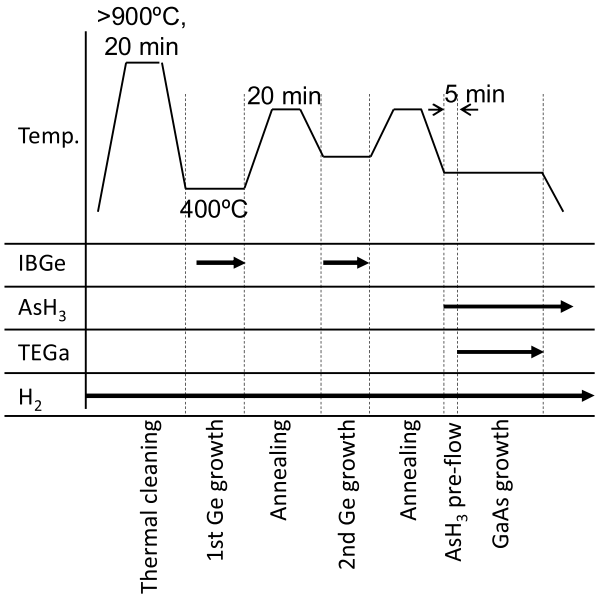

Fig. 2 Growth sequence of Ge and GaAs buffer layers

(SEM) and atomic force microscopy (AFM). To estimate the threading dislocation densities, X-ray diffraction (XRD), XRD reciprocal space mapping (XRD-RSM), X-ray rocking curve (XRC), and etch pit observations were performed. Cross-sectional transmission electron microscopy (TEM) was used to observe the dislocations. Room temperature (RT) PL measurements were performed for characterizing the optical properties of InGaAs/GaAs MQWs on the buffer layers.

3. Results and Discussion

3.1 Ge Buffer Layer Growth and Annealing

We examined the crystalline quality of the Ge buffer layer grown on Si substrate. Figure 3 shows a 5-μm-square AFM image of the as-grown Ge layer on the 6°-misoriented Si (100) substrate. Stripe-shaped surface roughness parallel to the $[0\bar{1}1]$ direction can be observed; the root-mean-square (RMS) surface roughness was 5.7 nm. The direction was perpendicular to misorientation direction. The angle of the stripe from the substrate surface was 6.1 +/−0.3°. This angle is almost the same as the substrate misorientation angle. For comparison, we grew a Ge layer on a misoriented Ge (100) substrate. In this case, stripe-shaped surface roughness was also observed on the Ge layer surface grown at the same temperature. However, step bunching was not observed when the growth temperature was 600°C or higher. This means that the roughness was mainly due to not dislocation, but rather step bunching.

Figure 4 shows bird-eye-view SEM images and corresponding AFM images of the as-grown and annealed Ge buffer layers. The bunched surface mentioned above was also observed on the as-grown surface by SEM. After 20-min of annealing, the surface roughness of the Ge layer was

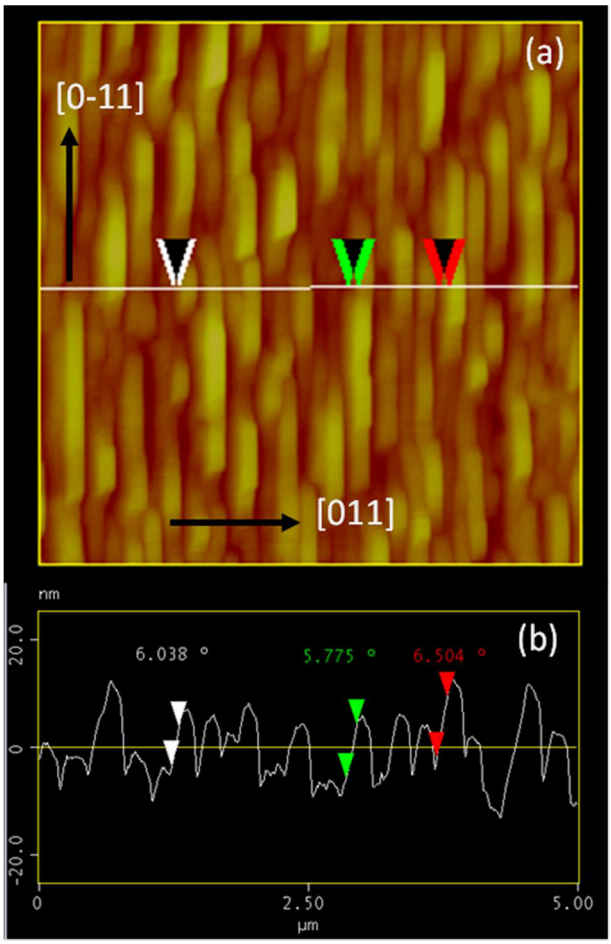

Fig. 3 AFM image of grown Ge buffer layer on 6°-misoriented Si substrate (a) plan view and (b) cross section

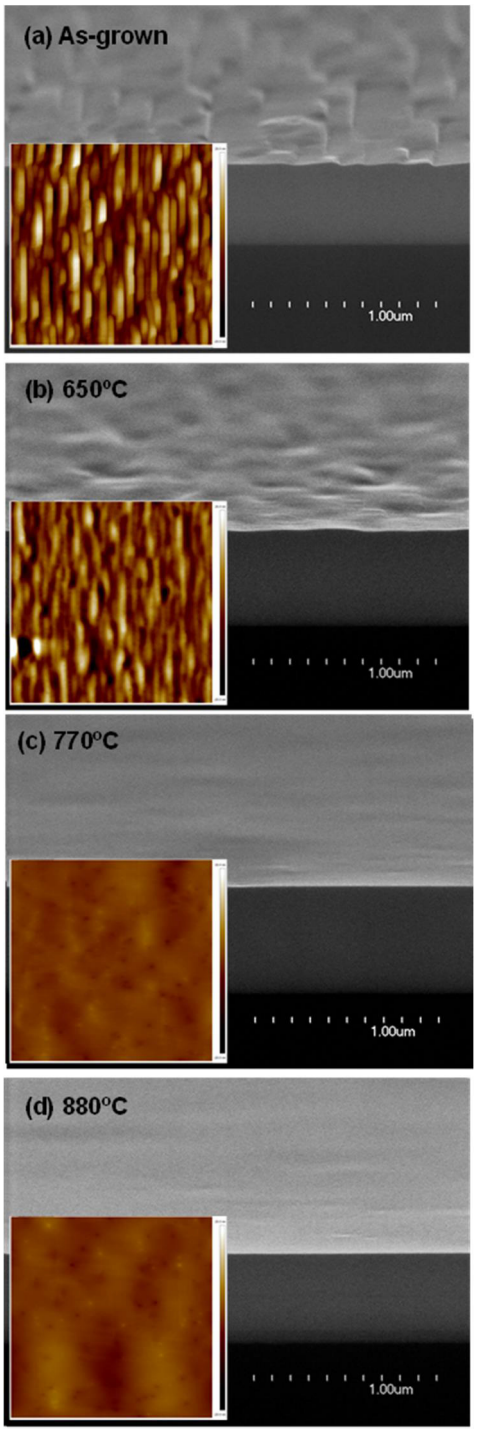

Fig. 4 Bird-eye view SEM images of (a) as-grown and annealed Ge buffer layer at (b) 650, (c) 770, and (d) 880°C. Insets are 5-μm-square AFM images.

reduced.

Figure 5 shows the measured XRC curves of the Ge buffer layer at different annealing temperatures. The full-width at half-maximum (FWHM) value of the as-grown Ge layer was 910 arcsec. After annealing, the FWHM values dramatically decreased to below 300 arcsec. This means that the threading dislocation density (TDD) decreased because of the post growth annealing. We estimated the TDDs of these Ge layers from the FWHM of the XRCs [30]. The relationship between FWHM and TDD is roughly

$$TDD = \left(\frac{\beta}{3b}\right)^2, \tag{1}$$

where β and b are the FWHM and Burgers vector, respectively. Supposing a 60° dislocation as a threading dislocation, Burgers vector can be calculated as $b = a/\sqrt{2}$ (a is the lattice constant of buffer layer). Figure 6 shows the relationship between the annealing temperature and estimated TDD. The surface roughness values measured by AFM are also plotted. The as-grown Ge layer had a TDD of 1.4×10^9 cm^{-2}. When the annealing temperature was 770 and 880°C, the estimated TDD was below 10^8 cm^{-2}. The largest reduction in TDD, 7.6×10^7 cm^{-2}, occurred at 770°C. The 770°C-annealed Ge buffer layer had the smallest surface roughness, 1.1 nm.

We also measured omega-2theta (004) XRD as shown in Fig. 7 (a). Since the TDD of the as-grown Ge layer was quite high, its diffracted peak was broad. By increasing the annealing temperature, the peak narrowed and shifted

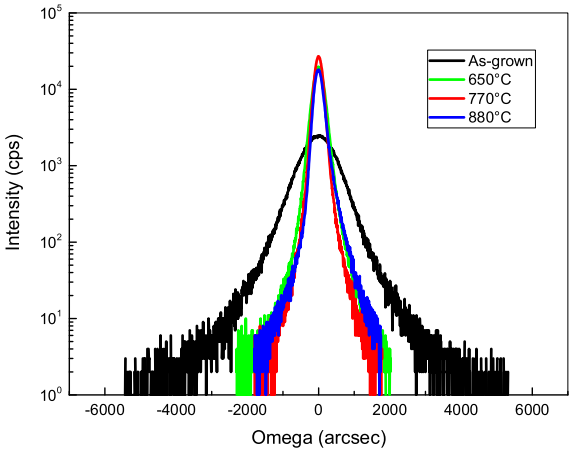

Fig. 5 XRC curves for various annealing temperatures.

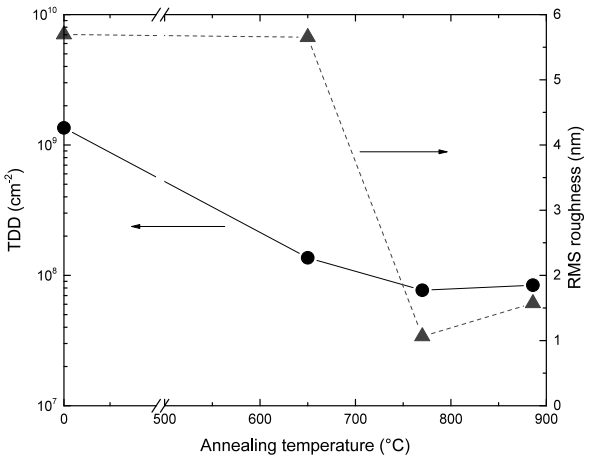

Fig. 6 RMS roughness and estimated TDD for various annealing temperatures. An annealing temperature of 0°C means as-grown.

toward a wider angle. This means that the crystalline quality of the Ge layer was improved and tensile strain was induced by the thermal expansion coefficient mismatch and the temperature difference. When the annealing temperature was 880°C, the Ge diffracted peak was asymmetric; the XRD intensity gently decayed at wider angles. We assumed that this was due to intermixing of Si and Ge atoms at their interface. Similar results are also observed in $(\bar{2}\bar{2}4)$ reciprocal space maps (RSMs) as shown in Fig. 7 (b)–(e). Due to the tensile strain caused by thermal expansion coefficient mismatch and/or layer tilt, the Ge layer's diffraction spots are plotted above the lines, which represent full relaxation. When the annealing temperature was 770°C, the maximum shrinkage of the Ge layer's diffraction spots was observed. From these results, we concluded that 770°C is the optimized annealing temperature to improve crystalline quality.

To reduce surface roughness, we performed a second Ge buffer layer growth and annealing. Figure 8 (a) and (b) show 5-μm-square AFM images of the Ge buffer layer before and after the 2nd growth and annealing. The RMS surface roughness was reduced, from 1.1 nm to 0.64 nm, as

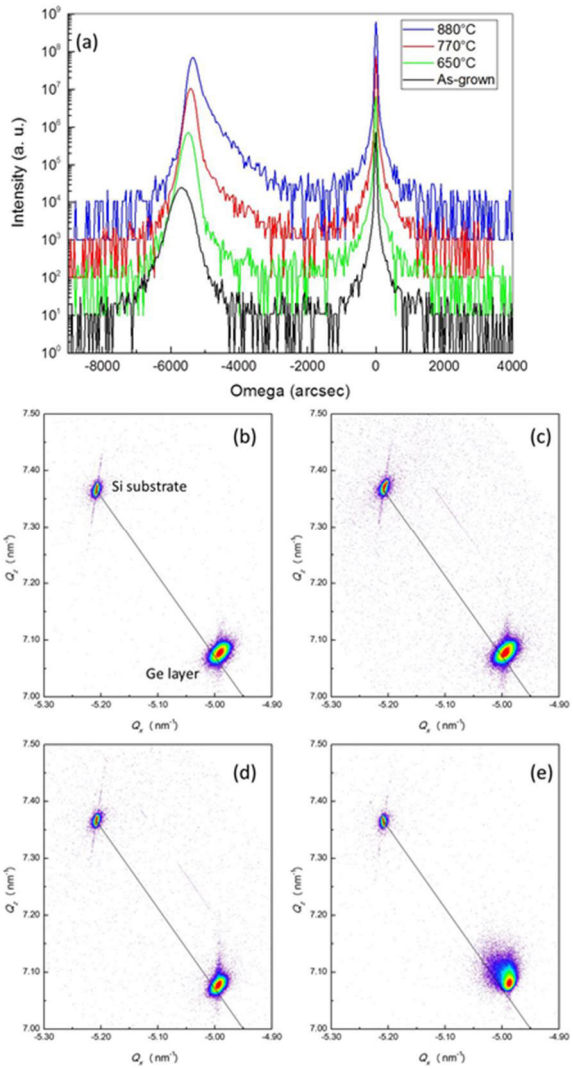

Fig. 7 **(004)** XRD curves at various annealing temperatures (a) and $(\bar{2}\bar{2}4)$ RSMs of (b) as-grown and annealed Ge buffer layer at (c) 650, (d) 770, and (e) 880°C. Lines in (b)–(e) represent full relaxation.

a result of the 2nd Ge buffer layer growth and annealing. This small level of roughness is suitable for GaAs growth on the surface. We also measured the etch pit density (EPD) of the Ge buffer layer. CH_3COOH : HNO_3 : HF : I_2 = 67 mL : 20 mL : 10 mL : 30 mg etchant was used to reveal any threading dislocations [10]. The AFM image of the etched Ge surface is shown in Fig. 8 (c). The EPD was $7.5 \pm 1.4 \times 10^7$ cm^{-2}. This value is close to the TDD estimated by using XRC as mentioned above.

3.2 GaAs Buffer Layer Growth and Annealing

A GaAs buffer layer was grown on the Ge buffer layer using AsH_3 and TEGa at 500°C. AsH_3 was introduced 5 min prior to TEGa in order to make an As-terminated Ge surface. Figure 9 shows a cross-sectional TEM image of grown GaAs/Ge layers on Si substrate. As shown in this image, many dislocations appear at the Ge/Si interface. The

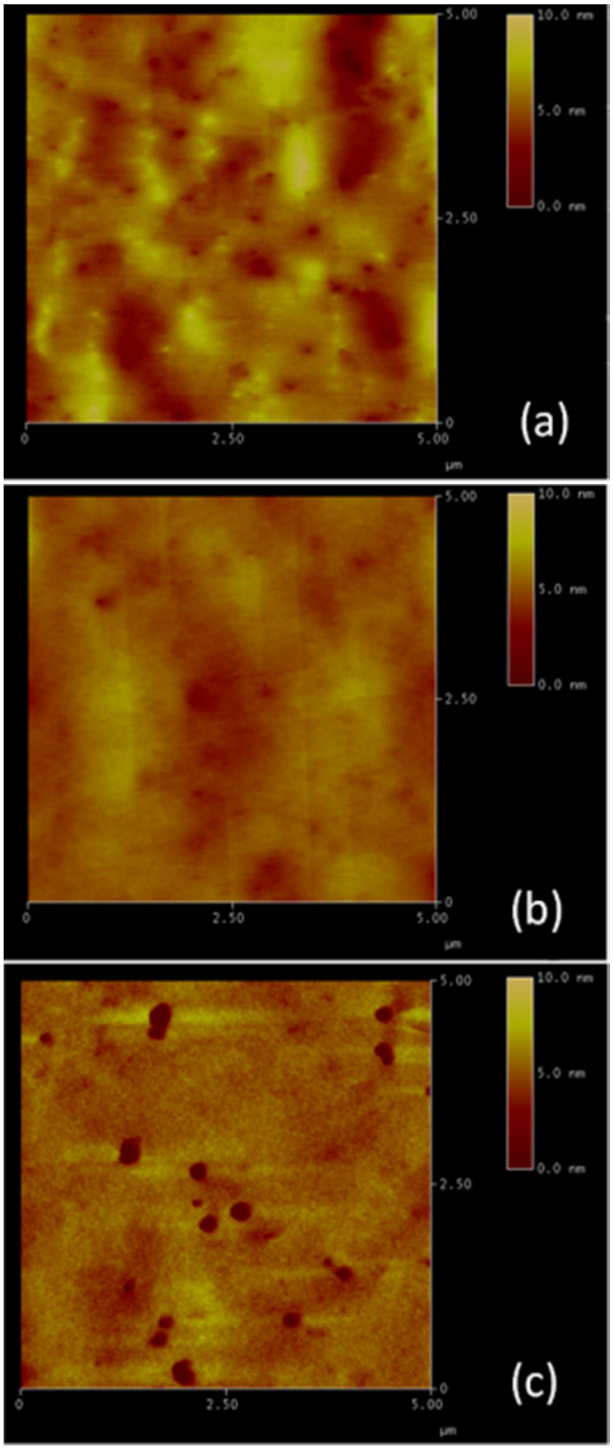

Fig. 8 AFM images of annealed Ge buffer surface. (a) Before 2nd growth and annealing, (b) after 2nd growth and annealing, and (c) after 2nd growth and annealing with etching by $CH_3COOH:HNO_3:HF:I_2$.

dislocations are terminated within a very thin Ge layer just above the interface and only a small fraction of them propagate toward the GaAs/Ge interface. However, a large number of dislocations were generated at GaAs/Ge interface even though their lattice constants are almost the same.

To eliminate dislocations at the GaAs/Ge interface, we

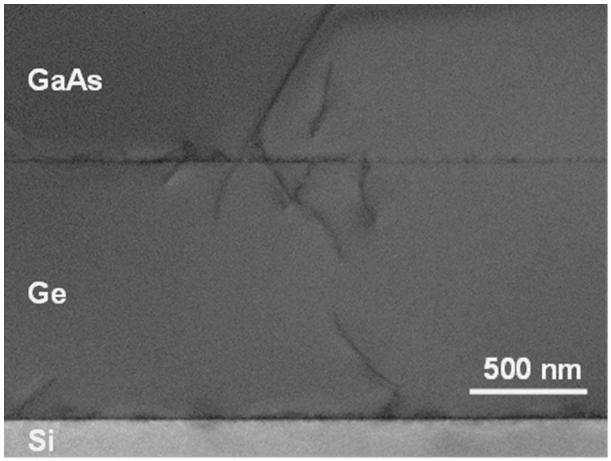

Fig. 9 Cross-sectional TEM image of as-grown GaAs/Ge/Si structure.

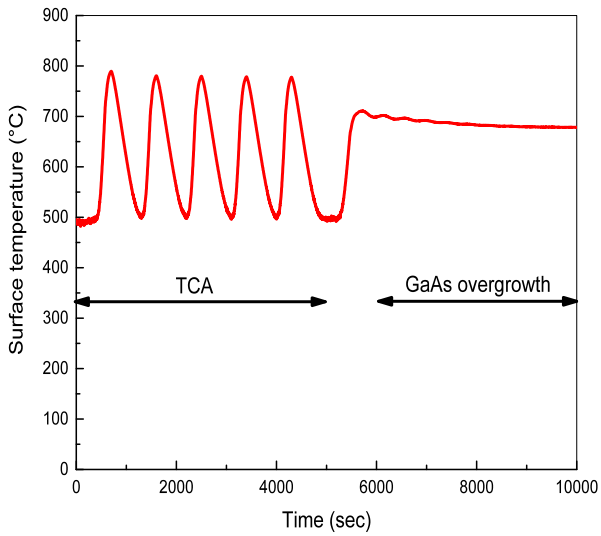

Fig. 10 Temperature history during TCA and GaAs overgrowth process of GaAs/Ge/Si structure.

performed five cycles of TCA in the MOVPE reactor after growth of a 100-nm-thick GaAs layer on the Ge buffer layer. After TCA, the GaAs layer was overgrown on the buffer layers. Figure 10 shows the temperature history during TCA as measured by a pyrometer on the MOVPE reactor. The highest and lowest temperatures were 800 and 500°C, respectively. Figure 11 shows a cross-sectional TEM image of the GaAs/Ge layers after performing TCA. The dislocations between the Ge and GaAs layers were efficiently suppressed.

InGaAs/GaAs MQWs were grown in the MOVPE reactor after the TCA and GaAs overgrowth. Figure 12 shows a cross-sectional TEM image of the MQW grown on the GaAs/Ge/Si structure with TCA. The MQW was correctly constructed with an InGaAs well and GaAs barrier layers. Figure 13 shows the PL spectra from the MQWs on the buffer layers with and without TCA. The PL spectrum from MQWs on a GaAs substrate is plotted as a reference. All samples were excited with a 532-nm YAG laser. PL

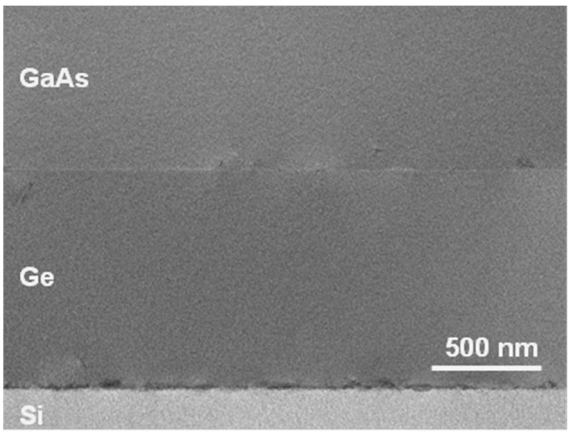

Fig. 11 Cross-sectional TEM image of cyclic annealed GaAs/Ge/Si structure.

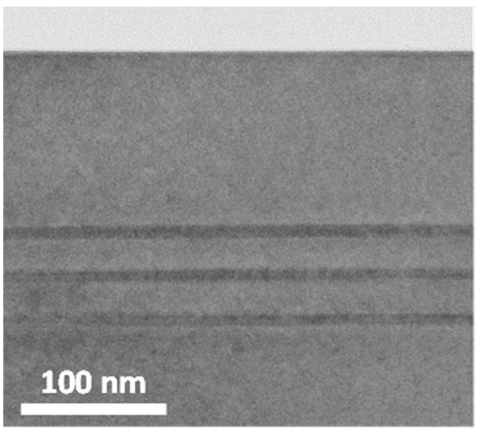

Fig. 12 Cross-sectional TEM image of MQW grown on GaAs/Ge/Si structure with TCA.

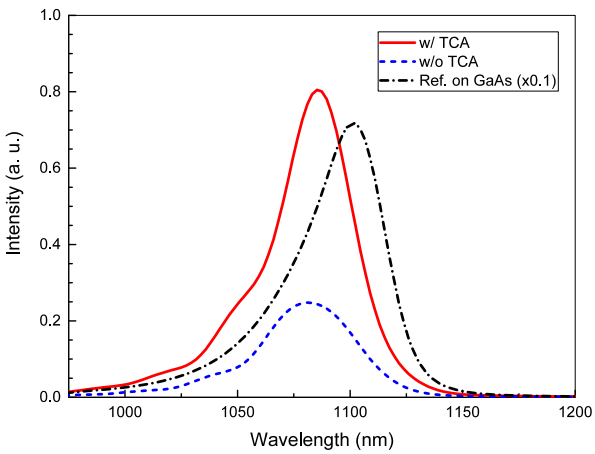

Fig. 13 PL spectra from MQWs on GaAs/Ge/Si structure. The PL spectrum from MQWs on a GaAs substrate is plotted as a reference.

peak intensity increased by a factor of three as a result of using TCA. This result indicates that wavelengths were different. This might be caused by the different strain, composition, or thickness in the MQWs. The PL peak intensity of the MQWs on GaAs/Ge/Si with TCA was 11% of that of the MQWs on the GaAs substrate. This means that some dislocations penetrated the MQW on the GaAs/Ge buffer layer. The introduction of TCA could make the GaAs/Ge/Si structure suitable as a buffer layer for LDs. However, for high-performance (high-speed, high-reliability) LDs, further improvements in the buffer layer using dislocations filters (e.g. strained layer superlattices [27], [31]–[33] or aspect ratio trapping [5], [34]–[36]) are necessary.

The GaAs/Ge buffer layer seems to be a good candidate for fabrication of LD structures on Si substrate. Our next challenge to developing MQW LDs emitting at 1.3 μm is growth of a metamorphic InGaAs buffer layer on the GaAs/Ge layers. Since all metamorphic InGaAs LDs were grown on on-axis GaAs (100) substrate [17]–[19], it is necessary to develop techniques that enable us to grow metamorphic InGaAs layers on misoriented substrates or anti-phase-domain-free GaAs layers on on-axis Si substrates.

4. Conclusions

We demonstrated MOVPE growth of GaAs/Ge buffer layers on Si substrate by using GaAs/Ge and Ge grown in the same MOVPE reactor, as an efficient manufacturing process.

The Ge buffer layer that was grown by MOVPE at low temperature (400°C) had a very rough surface due to step bunching and a high density of threading dislocations ($\sim 10^9$ cm^{-2} as estimated by XRC). By conducting post-growth annealing in an H_2 ambient in the MOVPE reactor, the surface roughness and TDD were suppressed. After growth of the second Ge buffer layer and annealing, the surface roughness and EPD were 0.64 nm and 7.6×10^7 cm^{-2}, respectively.

The GaAs layer on the Ge buffer layer was also characterized. The cross-sectional TEM images revealed high-density dislocations at the interface between the as-grown GaAs and Ge layer. TCA effectively suppressed the dislocations, and it increased the photoluminescence intensity from the MQWs on the top of the GaAs/Ge buffer layers by a factor of three.

These results suggest that MOVPE-grown GaAs/Ge/Si structures are well-suited for integrating light sources on Si substrate.

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