

Advanced Top-Down Fabrication Process of A-IGZO TFT for Roll-to-Roll Backplane

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SUMMARY Amorphous indium-gallium-zinc-oxide (a-IGZO) thin film transistor (TFT) was fabricated by an advanced self-aligned imprint lithography (ASAIL) method with a hybrid etching process. The SAIL is a top-down method to fabricate a TFT using a three-dimensional multilayer etch mask having all pattern information for the TFT. The hybrid etching process was newly applied in the original SAIL process for the purpose of reducing plasma damage of a-IGZO channel layer during plasma etching in the ASAIL process. This research demonstrated that the a-IGZO TFT could be successfully fabricated by the ASAIL process. In particular, the hybrid etching process applied in this paper can be utilized for the back-channel-etch type a-IGZO TFT and further extended for the roll-to-roll backplane process.

key words: TFT, IGZO, imprint, roll-to-roll, OLED, rollable

1. Introduction

Recently, active-matrix organic light-emitting diodes (AMOLEDs) have been widely studied using plastic substrates such as polyimide (PI), polyethylene naphthalate (PEN), and polyethylene terephthalate (PET) [1]. Not only are foldable OLED displays already close to commercialization, but also large-area rollable OLED displays are evolving into future core display technologies [2]. Although a number of methods for mass production of the rollable OLED displays have been studied, there are still no established manufacturing technologies. Since rollable displays use plastic-based substrates, it is expected that the manufacturing process becomes more difficult and the production cost will astronomically go up as the size of the display increases [3]. In this study, we have studied a roll-to-roll (R2R) backplane process technology for the rollable displays which can realize high resolution, low cost, and high throughput. To date, various R2R processes have been attempted to implement OLED displays. These attempts are related to the R2R deposition of OLEDs or thin-film encapsulation (TFE) process [4]. However, little R2R research has been done on the thin-film transistor (TFT) backplane for OLED displays. Fortunately, the self-aligned imprint lithography (SAIL) process has been studied by Hewlett Packard (HP) in 2003 as a similar backplane development study for

an e-paper display [5]. This device has integrated a backplane using a-Si TFT of bottom gate type, but even now, the related research and development has been no longer in progress. In this study, we newly propose an a-IGZO TFT fabrication process using an advanced self-aligned imprint lithography (ASAIL) method which is considered to be the most efficient and unique process to fabricate TFT backplane for large-area rollable OLED display. We report the electrical characteristics of a-IGZO TFT fabricated by the ASAIL process. The results of this study are expected to be the basis for future development of complete R2R process for rollable OLED displays.

2. Experimental

2.1 Master Template and PDMS Mold

The most important part in this study is in the fabrication of a master template for the imprint lithography process. For the design of the master template, a commercial 3D modeling software was used to simulate and verify the process procedure. As shown in Fig. 1, the master template was fabricated to have the information of a unit TFT. A 6" (100) silicon wafer was the substrate for the master template and the channel width and length of the TFT were both 100 μm . The master template for the unit TFT has a four-story structure and each floor contains information for patterning the TFT using the top-down ASAIL process. The height of each floor was $2 \pm 0.1 \mu\text{m}$ and the total height of the four-story structure was $6 \pm 0.1 \mu\text{m}$, based on the first floor. The patterning of each layer was performed with conventional photolithography and deep reactive ion etching (RIE) processes. The master template was laser-scribed at $25 \times 25 \text{ mm}^2$ to facilitate handling of the substrate during this experiment. In order to fabricate a-IGZO TFT using the ASAIL process, it is necessary to prepare an imprint mold as well as the master template. For the ASAIL process, the reverse-patterned polydimethylsiloxane (PDMS) mold can be prepared by coating PDMS resin on the master template and then detaching it directly.

The master template was treated with a self-assembled monolayer (SAM) to provide hydrophobicity to the surface. It facilitates the pattern transfer and detachment of the PDMS mold off the master template. To verify the hydrophobicity of the surface, the surface energy was checked by measuring the contact angle. The PDMS (Sylgard 184,

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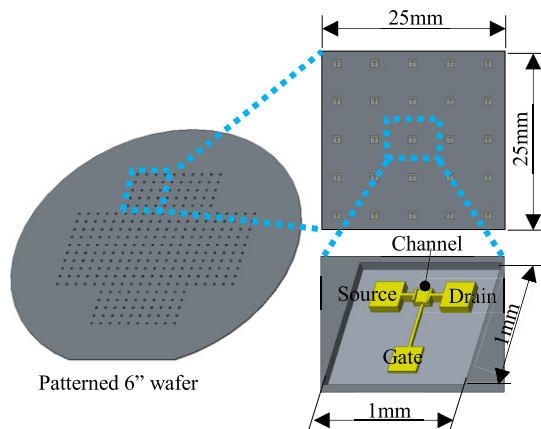


Fig. 1 Master template with four-story structure on Si wafer.

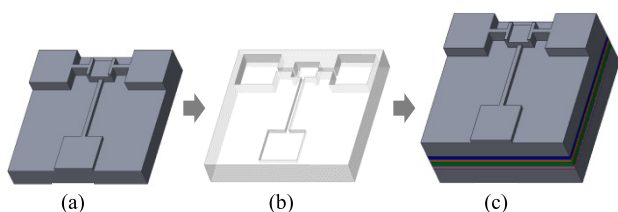


Fig. 2 Schematic of pattern transfer from master template to PDMS mold and resin; (a) master template, (b) PDMS mold, (c) imprinted resin.

Corning, USA) base was mixed with its curing agent at a ratio of 10:1, and the solution was coated onto the master template, followed by a degassing process for 40 minutes. After degassing, thermal curing was performed for 30 minutes on a hot plate maintained at 85°C. The PDMS mold was then separated and confirmed whether the master-template pattern was well transferred. Figure 2 shows the master template, imprint mold, and the imprinted resin on a substrate using the mold. The pattern transfer from master template to mold and imprinted resin was carefully checked and quantified by measuring the transfer yield (transferred pattern size/template-pattern size \times 100%). The transfer yield was measured 94~97%.

2.2 Preparation of TFT Thin Films and Imprint Resin Mask

A series of thin films constituting a-IGZO TFT were sequentially deposited on a glass substrate. At first, Al thin film was deposited as the gate electrode layer by dc sputtering to 100 nm thickness. The SiO₂ thin film was then deposited as the gate insulator to the thickness of 200 nm by PECVD. The semiconducting a-IGZO layer (50 nm) was deposited using a rf magnetron sputtering method. For the deposition, we utilized a target having the composition of In₂O₃:Ga₂O₃:ZnO = 1:1:1 mol%. After the IGZO deposition, a rapid thermal annealing process was performed at 300°C for 1 hour with 200 sccm of N₂ gas. The source/drain electrode layer was 100 nm-thick Cr thin film, which was deposited by a thermal evaporation method. Af-

ter the vacuum deposition of the thin films was completed, NOA63 (Norland, USA) UV-curable resin was uniformly spin-coated to the thickness of 12 \pm 1 μ m. The PDMS mold was then placed on the multilayered sample and pressed uniformly with an imprinting machine. The UV-curable resin was cured under UV at 1.6–2.0 J/cm² of exposure energy (λ = 365 nm). After completion of the first UV exposure, the PDMS mold was removed from the sample, and the second exposure was performed to maintain the pattern shape and complete curing. The imprinted resin pattern is identical to the pattern of the master template as shown in Fig. 2. The three-dimensional four-story imprinted resin is designed to have all the pattern information of the TFTs to be fabricated. The imprinted resin was thinned down by a dry etching until a floor was fully removed to reveal the upper floor pattern. The exposed resin pattern in every floor works as the etch mask for the TFT fabrication.

2.3 TFT Fabrication Process Using ASAIL

The ASAIL process for TFT fabrication is composed of eight steps as shown in Fig. 3. After imprinting the resin on the multilayered sample using the PDMS mold as shown in Fig. 3 (a), the resin pattern was first checked that the three-dimensional structure of the master template was well transferred. As shown in Fig. 3 (b), the imprinted sample was placed in the RIE equipment and dry etching was performed using Ar plasma until the first-floor resin was completely removed to have thin-film layers exposed. Figure 3 (c) shows the structure obtained after the full dry etching of the multilayer thin films until the surface of the glass substrate was exposed. The Cr and a-IGZO thin films were dry-etched using Cl₂ gas. The SiO₂ and Al thin films were etched using CF₄ and BCl₃+Cl₂ gases, respectively. Figure 3 (d) shows the removal of the second-floor resin in the gate area, which results in the exposure of the Cr surface. The Cr/IGZO/SiO₂ layers was then sequentially removed to reveal the Al gate electrode structure, as shown in Fig. 3 (e). Next, the third-floor resin in the TFT channel region was opened [Fig. 3 (f)], and the exposed Cr layer was removed by a hybrid etching method using dry and wet etching in succession to expose the a-IGZO surface [Fig. 3 (g)]. Finally, the resin remaining on the source/drain electrode was removed completely to form a bottom-gate type a-IGZO TFT, as shown in Fig. 3 (h).

2.4 Inspection and Analysis of Fabricated TFT

The imprinted and etched pattern shapes of the multilayer thin film for the unit TFT device were confirmed by scanning electron microscopy (SEM) after each of the eight processes shown in Fig. 3 was completed. The X-ray photoelectron spectroscopy (XPS) analysis of the a-IGZO film was performed to check the change in the elemental composition before and after the plasma processes.

Electrical characteristics of the fabricated a-IGZO TFTs were analyzed by a semiconductor parameter analyzer (Agilent 4155B) to measure the transfer curve, output cur-

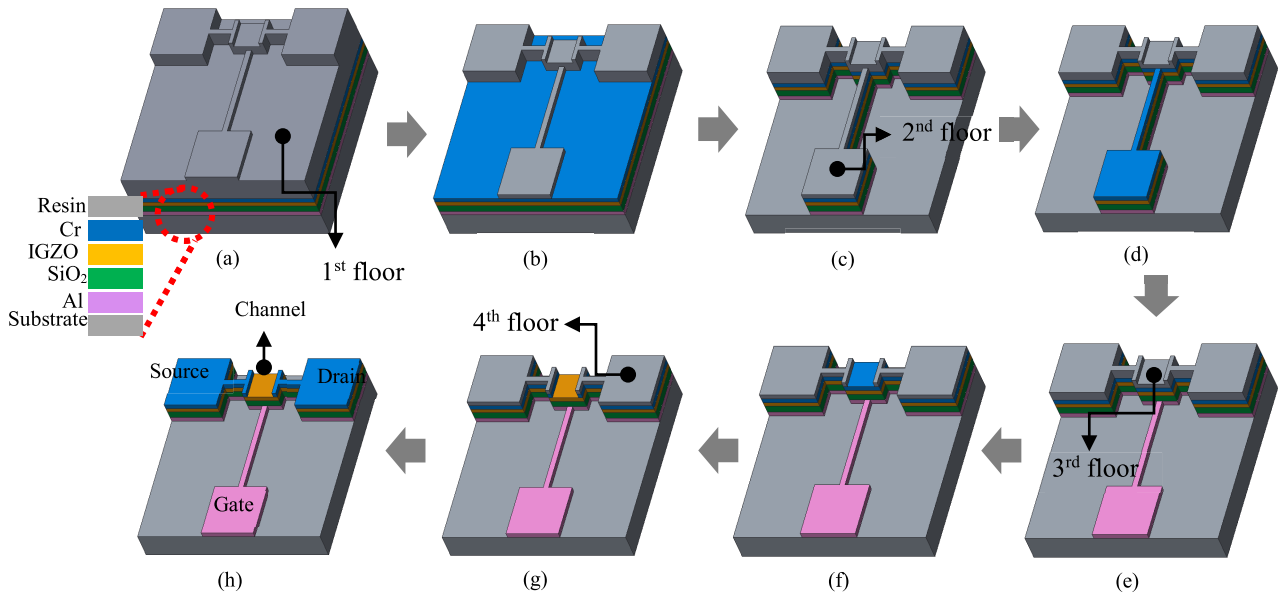


Fig. 3 Fabrication process of a-IGZO TFT using ASAIL process; (a) imprinted resin by patterned PDMS mold, (b) first-floor resin open, (c) full dry etching of thin films (Cr, IGZO, SiO₂ and Al) in the open region, (d) second-floor resin open for gate electrode, (e) dry etching of thin films (Cr, IGZO and SiO₂) for gate electrode, (f) third-floor resin open for channel, (g) hybrid etching of Cr thin film for channel, (h) final TFT structure after fourth-floor resin removal.

rent, on/off ratio, and field effect linear mobility.

3. Results and Discussion

Figure 4 (a) shows an optical microscopic image of the master template. The contact angle was measured as 98.2° after the SAM treatment to lower the surface energy. It was confirmed that the pattern transfer to the PDMS mold was improved by the SAM treatment of the surface. The SEM images of Figs. 4 (b) and 4 (c) showed that the transfer yields (transferred pattern size/designed pattern size × 100%) for the PDMS mold and imprinted resin were 94~97% and 95~96%, respectively. This result means that the final imprinted resin-pattern size is about 7~11% smaller than the original master-template pattern. Therefore, it is necessary to increase the original design pattern by about 10% in order to finally obtain the designed pattern size of the imprinted resin. Since the ASAIL process in this study is a self-aligned process, no separate alignment is necessary and therefore the pattern size change during the imprint process is not a problem. According to the literature, a typical TFT fabrication process using a R2R photolithography has been reported to produce misalignment of 5~10 μm at each process step [6]. Furthermore, when considering the mechanical deformation of the plastic substrates such as PI, PEN, or PET, the alignment error is expected to be about 100 μm when the substrate width is 100 mm. This misalignment problem could become more severe when high temperature processes are applied. In general, the R2R process for the TFT fabrication utilizes wet printing processes as well as a photolithography process [7], [8].

However, these processes still suffer from pattern accuracy, pattern misalignment, and insufficient electrical char-

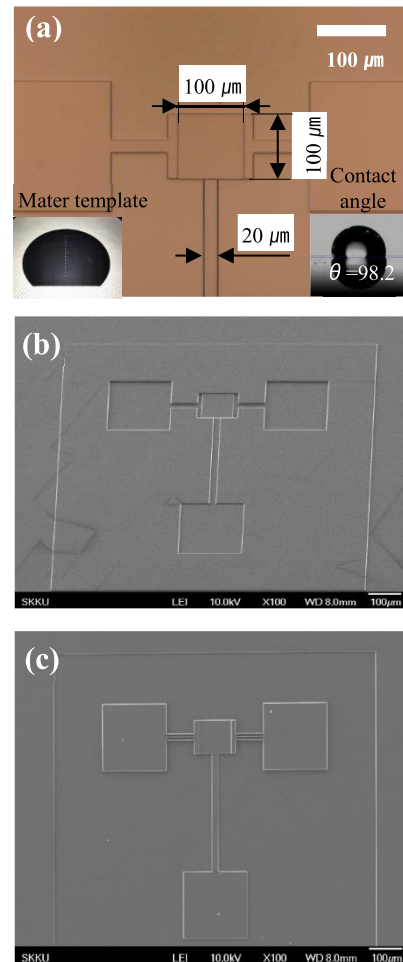


Fig. 4 Optical and SEM images of master template and reversed PDMS mold; (a) master template, (b) PDMS mold, (c) imprinted resin.

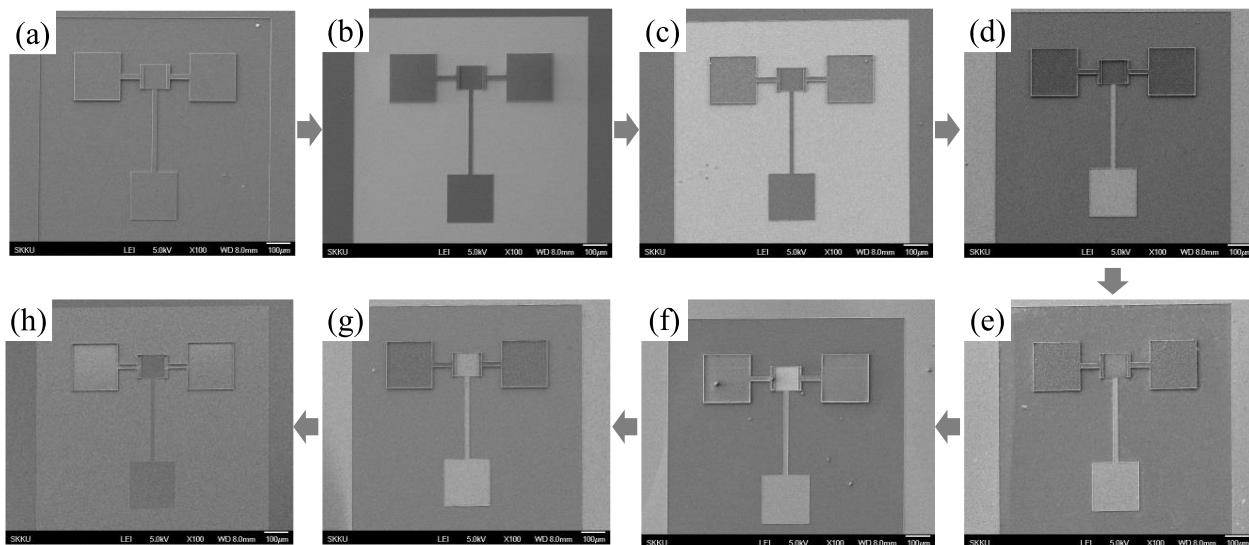


Fig. 5 SEM images of a-IGZO TFT during ASAIL process; (a) imprinted resin by patterned PDMS mold, (b) first-floor resin open, (c) full dry etching of thin films (Cr, IGZO, SiO₂ and Al) in the open region, (d) second-floor resin open for gate electrode, (e) dry etching of thin films (Cr, IGZO and SiO₂) for gate electrode, (f) third-floor resin open for channel, (g) hybrid etching of Cr thin film for channel, (h) final TFT structure after fourth-floor resin removal.

acteristics due to the nature of the solution process. Although the R2R photolithography method has been studied to solve these problems, the alignment difficulty, low productivity, and high equipment cost have not been solved yet [9].

The ASAIL process used in this study can fabricate a TFT using sequential etching processes to remove the resin and multilayer film after resin imprinting without the need for alignment unlike other TFT fabrication methods. Detailed process results by the ASAIL process are as follows. Figure 5 (b) shows the exposed Cr layer outside the TFT area by etching the first-floor resin layer in the structure shown in Fig. 5 (a). The outer area of the TFT was sequentially removed by dry etching of Cr, IGZO, SiO₂, and Al layers to obtain the structure shown in Fig. 5 (c). Figures 5 (d) and 5 (e) show the Cr and Al metal layers exposed by etching the gate line region, respectively. As shown in Fig. 5 (f), the resin of channel area was dry-etched to reveal the Cr metal surface, which was then removed by a hybrid etching process consisting of sequential dry and wet etching to have the a-IGZO layer exposed as shown in Fig. 5 (g). Figure 5 (h) shows that the Cr layer, which serves as the source/drain electrode, was exposed by etching the fourth-floor resin in the source/drain region. In this study, XPS analysis was performed to analyze the damage of the a-IGZO layer that may occur when the Cr electrode on the a-IGZO layer is etched in Cl₂ plasma.

Table 1 shows the XPS measurement results. In order to open the a-IGZO layer by dry-etching all the overlying Cr layer, the surface of the a-IGZO layer is inevitably exposed to Cl₂ plasma. When the a-IGZO surface is exposed to the plasma, the atomic percentages of In and Ga are reduced as shown in Table 1 of the analysis results. The role of Ga

Table 1 Atomic compositions of each element in the IGZO layer measured by XPS before and after the plasma treatment.

Treatment	rf power	Atomic percentage (%)			
		In	Ga	Zn	O
RTA	N/A	8.35	32.09	7.41	43.77
	10W	4.31	19.71	6.28	37.74
Cl ₂ Plasma	20W	6.59	25.54	9.34	44.99

*RTA : Rapid Thermal Annealing

is not only to suppress the generation of excessive carriers but also help to increase stability of a-IGZO TFT, while In works for increasing the electron mobility in the a-IGZO TFT. Therefore, it was confirmed that the decrease in the Ga and In atomic compositions after the plasma treatment affects the characteristics of a-IGZO TFT.

In order to solve the damage problem caused by plasma, dry etching was first applied to the upper part of the a-IGZO layer and the remaining 10–20 nm thick a-IGZO layer was wet-etched to minimize damage to the layer. It has been reported that the a-IGZO TFT performance can be improved by preventing the damage caused by the plasma for a back-channel-etch TFT structure using this hybrid etching method [10].

Figure 6 (a) shows typical transfer characteristics of the a-IGZO TFT fabricated by the ASAIL method. The measured electrical property was V_{th} of 10.46 V, sub-threshold swing (S.S.) of 0.45 V/decade, field-effect mobility (μ_{FE}) of 0.27 cm²/V-s, and current on/off ratio (I_{on}/I_{off}) of 8.97 × 10⁸. Figure 6 (b) depicts the output characteristic curves mea-

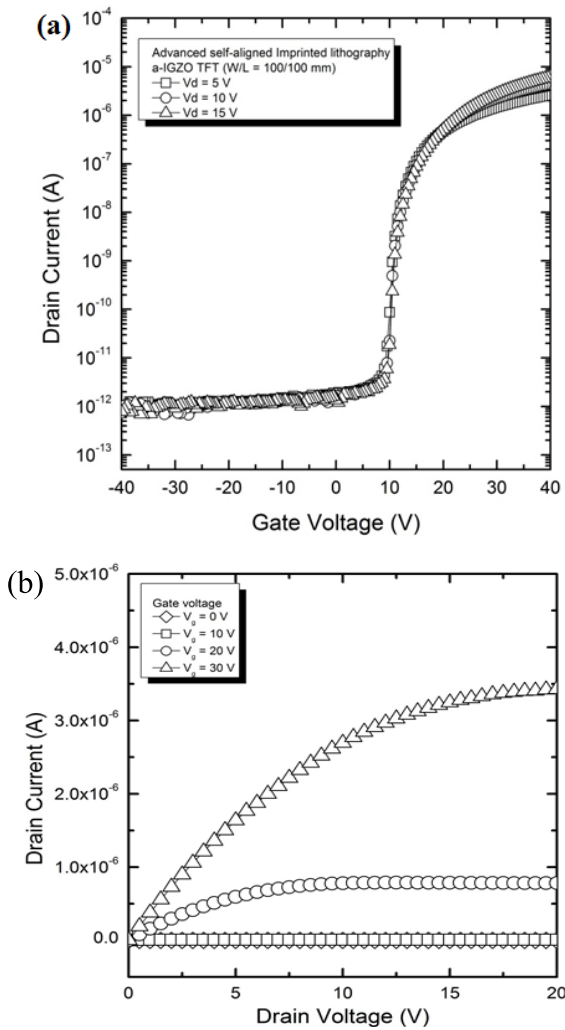


Fig. 6 Characteristic curves of a-IGZO TFT fabricated by ASAIL process; (a) transfer characteristics, (b) output characteristics.

sured with varying drain voltage from 0 V to 20 V and gate voltage from 0 V to 30 V with a step of 10 V.

4. Conclusions

In this study, a-IGZO TFT was successfully demonstrated using the new ASAIL method. For the ASAIL process, a three-dimensional master template and replicated imprint molds were fabricated. The imprint mold was used to imprint a resin pattern having the same structure as the master template on the multilayer thin films composed of the IGZO TFT materials. Since the three-dimensional resin pattern is designed to serve as multiple etching masks, the a-IGZO TFT fabrication process does not require a separate photolithography process and is carried out using only the etching processes. Particularly, in this study, a hybrid etching method combining dry and wet etching was adopted to prevent a-IGZO from being damaged by plasma during the ASAIL process.

The a-IGZO TFT fabricated by the ASAIL process

showed good switching characteristics and it was confirmed that this process can be used to fabricate the a-IGZO TFT more easily. In particular, the ASAIL process has a great advantage that it can be applied to a roll-to-roll process because it enables the fabrication of TFTs by only the imprint and etching processes without precise pattern alignment.

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