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Arrayed Waveguide Gratings and Their Application Using Super-High-Δ Silica-Based Planar Lightwave Circuit Technology

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SUMMARY This paper reviews our recent progress on arrayed waveguide gratings (AWGs) using super-high-Δ silica-based planar lightwave circuit (PLC) technology and their application to integrated optical devices. Factors affecting the chip size of AWGs and the impact of increasing relative index difference Δ on the chip size are investigated, and the fabrication result of a compact athermal AWG using 2.5%-Δ silica-based waveguides is presented. As an application of super-high-Δ AWGs to integrated devices, a flat-passband multi/demultiplexer consisting of an AWG and cascaded MZIs is presented.

key words: *planar lightwave circuits, arrayed waveguide gratings, integrated optics devices, glass waveguides*

1. Introduction

An arrayed waveguide grating (AWG) is a key device in the commercial deployment of dense wavelength division multiplexing (DWDM) systems. As increasing the number of add/drop nodes as an advance in DWDM systems, compact and low-cost multi/demultiplexers are highly demanded. Thus, it is important to make an AWG circuit smaller. Reducing the size of optical circuit is also favorable for achieving new functions by integrating various devices/elements. Increasing the relative index difference Δ between core and cladding is an effective way to achieve smaller chip size. For silica-based waveguides, higher index-contrast waveguides (typically 1.5% or larger-Δ) than the conventional value are generally called "super-high Δ" waveguides [1]. While silica-based waveguides of typically 0.8%-Δ [2] have been widely used for AWGs because of its low propagation loss and small fabrication errors preferable for obtaining low crosstalk of around −30 dB, 1.5–2.5%-Δ AWGs with silica-based waveguides [1], [3]–[12] and 2%-Δ AWGs with SiON waveguides [13] have also been demonstrated as recent applications of super-high-Δ waveguides. The chip area size for Δ=1.5–2.5% can be reduced to around one third to one tenth that of a conventional 0.8%-Δ AWG.

Meanwhile, in metropolitan and access area networks, multi/demultiplexers must have a flat and wide spectral response to allow the concatenation of many multi/demultiplexers. The techniques for flattening the passband of AWGs can be basically divided in two types, i.e. obtaining a rectangular focusing field profile and combining two synchronized routers. The latter type using a combination of two synchronized routers [14]–[18] is a promising approach to obtain low loss as well as wide passband. This type can be regarded as one of integrated waveguide devices combining an AWG and another device in one chip. Low-loss and flat-passband characteristics have been achieved with a Mach-Zehnder interferometer (MZI) or a three-arm interferometer for the input of an AWG [16], [18] in a compact chip. Significantly flat spectra have been attained by using back-to-back AWGs, first applied as a coarse WDM filter [17], although the loss due to transition between the slab and array typically becomes twice that of a single AWG.

This paper describes AWGs using super-high-Δ silica-based planar lightwave circuit technology and their application to integrated optical devices. Section 2 shows compact AWGs using super-high-Δ waveguides. Some factors affecting the chip size of AWGs and the impact of increasing the Δ on the chip size of AWGs are investigated. A compact athermal AWG is demonstrated by using 2.5%-Δ silica-based waveguides. Section 3 shows an application of super-high-Δ AWGs to integrated devices. A flat-passband multi/demultiplexer consisting of an AWG and cascaded MZIs is presented to achieve low insertion loss and steep passband characteristics.

2. Compact AWG Using Super-High-Δ Waveguides

2.1 Basic Structure

Figure 1 illustrates the basic optical circuit of an AWG. The optical circuit consists of an input waveguide, input and output slabs, waveguide array, and output waveguides. The waveguide array, which acts as a dispersive element, is de-

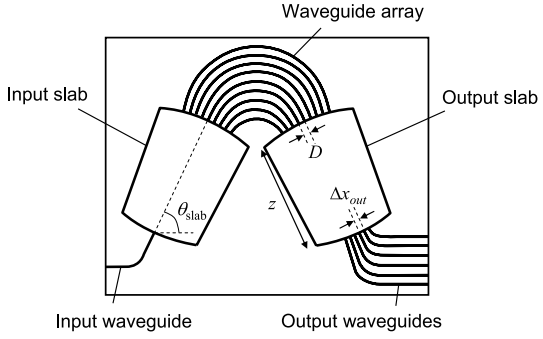

Fig. 1 Optical circuit of AWG.

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signed with waveguides having a constant waveguide length difference to adjacent waveguides ΔL. When the light is launched into the input waveguide, it spreads out in the input slab and is coupled to the waveguides in the array. After passing through the array, each beam of light interferes constructively or destructively according to the phase condition in the output slab. The interfering light constructively focuses onto one of the output waveguides according to its wavelength λ. The operation of an AWG can be described by the following grating equation:

$$2\pi m = \frac{2\pi}{\lambda} n_a \Delta L + \frac{2\pi}{\lambda} \frac{n_s D x_{out}}{z} \quad (1)$$

where m is the integer representing the grating order, n_a and n_s are the effective refractive indices for the waveguides in the array and slabs, D is the interval of the waveguides in the array at slab-to-array interface, z is the focal length of the output slab and x_{out} is the position of the output waveguide along the edge of the output slab from the center.

2.2 Impact of Relative Index Difference Δ on AWG Chip Size

The chip size of the AWG is dominated by many factors. The following factors directly affect the geometrical layout of the AWG:

i) Design parameters z, D, and ΔL

The length difference between adjacent waveguides in the array, ΔL, depends on the free spectral range (FSR) of AWG and the effective refractive index of the waveguide array n_a. As far as the change of Δ is at most several percents, the change of n_a is very small. Thus, ΔL substantially depends on only the FSR. Typically, larger FSR leads to smaller ΔL. However, larger FSR also leads to larger slab focal length z. Hence, the chip size typically tends to increase for larger FSR. On the other hand, increasing Δ is effective to reduce the slab focal length z. The z is expressed as

$$z = \frac{n_a}{n_g} \frac{n_s D}{m} \frac{\Delta x_{out}}{\Delta \lambda} \quad (2)$$

where $n_g = n_a - \lambda dn_a/d\lambda$ is the group index of the waveguides in the array, Δx_{out} is the interval of the output waveguides at the connection to the output slab, and $\Delta\lambda$ is the wavelength channel spacing. The core size of channel waveguides can be reduced as Δ increases and it leads to the reduction of D and Δx_{out}, whereas the changes of n_a, n_s, and n_g are very small. Consequently, z can also be reduced as Δ increases. Quantitatively, the normalized frequency V is given by [19]

$$V = k_0 w \sqrt{n_{co}^2 - n_{cl}^2} = k_0 n_{co} w \sqrt{2\Delta} \quad (3)$$

where n_{co} and n_{cl} are the refractive indices of core and cladding, w is the core width and k_0 is the wave number in vacuum. From this relation, the core width w can be reduced with a factor of $\Delta^{-1/2}$ when the V is designed to be constant so that the shape of field profile becomes similar. Thus, when an AWG is designed so as to obtain almost the same passband profile with different Δ, the intervals D and Δx_{out} can be also reduced with a factor of roughly $\Delta^{-1/2}$. Therefore, the slab focal length can be reduced with a factor of Δ^{-1}.

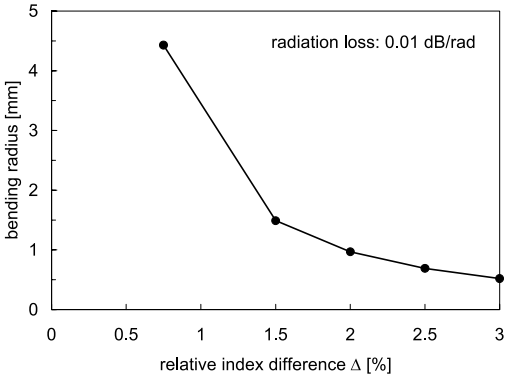


Fig. 2 Bending radius at radiation loss of 0.01 dB/rad.

ii) Allowable bending radius of curve waveguides

Allowable bending radius of curved waveguides can be also reduced as Δ increases. The calculated bending radius as a function of Δ is plotted in Fig. 2, assuming that radiation loss is allowed to be 0.01 dB/rad. The allowable bending radius becomes 0.7 mm for 2.5%-Δ, while the radii for 0.8%-Δ and 1.5%-Δ are 4.5 mm and 1.5 mm, respectively.

iii) Type of array geometry

The type of array structure is roughly divided into transmission type, reflection type [20] and arrow-head type [21]. The chip size can be reduced by using the reflection type because only one slab is needed and the areas for input/output waveguides and waveguide array can be drastically reduced. The arrow-head type, that is a kind of transmission type, is effective to reduce bending area in waveguide array. The latter two types need reflection mirrors on the edge of all waveguides in the array, which need precise control in positions to suppress crosstalk due to phase errors. In this paper, only the transmission type will be treated.

As mentioned above, some factors affecting the chip size of an AWG depend on Δ. Moreover, in an actual circuit, the layout also strongly depends on the required performance such as the number of channels, channel spacing, passband shape, etc. Hence, the chip sizes of AWGs with different Δ were estimated assuming that the AWGs have almost the same spectral response. The design parameters for estimating the chip area sizes are listed in Table 1. Figure 3 plots the estimated area sizes of chips as a function of Δ. The slab focal length z was assumed to be proportional to Δ^{-1}, and the waveguide intervals at slab-array interface to be proportional to $\Delta^{-1/2}$. The arranging angle of slab θ_{slab}, defined as Fig. 1, was determined so that the waveguides in the array did not intersect each other. θ_{slab} should generally be changed for different Δ because geometrical design parameters such as D, z, and ΔL do not have the same proportion for different Δ. Although the assumption was only regarded as

Table 1 Design parameters for estimating chip area size.

Relative index difference Δ	0.8%	1.5%	2.5%	4%
Number of channels	16			
Channel spacing	100 GHz			
Grating order m	40			
Number of waveguides in array	200			
Minimum bending radius	4.5 mm	1.5 mm	0.7 mm	0.3 mm
Slab focal length z	18.8 mm	10.0 mm	6.0 mm	3.8 mm
Length difference in waveguide array ΔL	42.35 μm	42.18 μm	41.94 μm	41.57 μm
Arranging angle of slab θ_{slab}	60°	70°	90°	90°

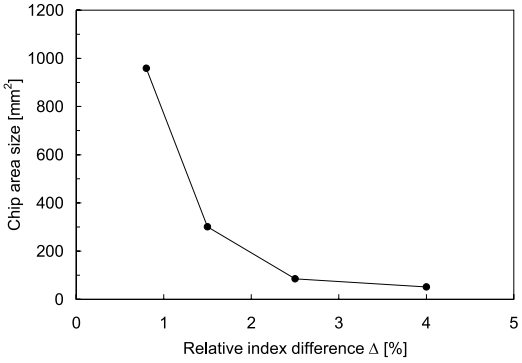


Fig. 3 Estimated area size of 16-channel 100-GHz-spacing AWG chip.

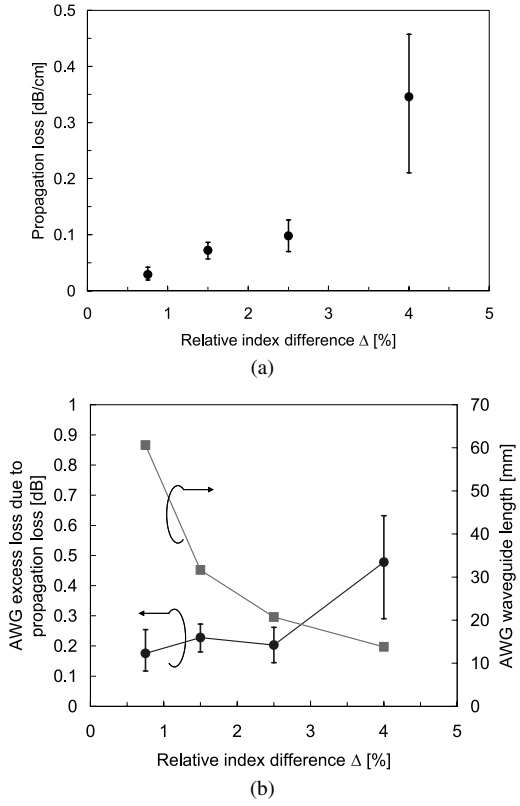


Fig. 4 Measured propagation loss for Ge-doped channel waveguides for various Δ. (a) propagation loss per centimeter and (b) estimated excess loss and average waveguide lengths of 16-channel AWGs. $\lambda = 1.55\,\mu$m.

an example, the chip area for 2.5%-Δ is reduced by around one tenth compared with the conventional 0.8%-Δ.

2.3 Formation Process of Super-High-Δ Waveguide

Test chips including long waveguides were fabricated to estimate propagation loss for various Δ. Ge-doped SiO_2 core film was formed by plasma-enhanced chemical vapor deposition (PECVD). The Δ was varied by changing the density of Ge dopant. The PECVD process was followed by photolithography and reactive ion etching (RIE) to form waveguide patterns. Then the core was embedded in a non-doped SiO_2 over-cladding layer by PECVD. The propagation loss of high-Δ waveguides at $\lambda = 1.55\,\mu$m is plotted in Fig. 4(a). The losses of a 100-cm-long waveguide and 5-cm-long waveguide on the same chip were measured and then the propagation loss was estimated as the difference between these losses. Although the propagation loss increased as Δ was larger, the loss was sufficiently low (less than 0.1 dB/cm) up to the Δ of 2.5%. The excess loss of an AWG due to the propagation loss can be estimated from this result. Figure 4(b) plots the estimated excess loss and the average path lengths of 16-channel AWGs for various Δ. The design parameters in Table 1 were also used to estimate the path lengths. Since the path is shorter for larger Δ, the excess loss due to the propagation loss is as low as ∼0.2 dB up to 2.5%-Δ, although the excess loss increases to ∼0.5 dB for 4%-Δ.

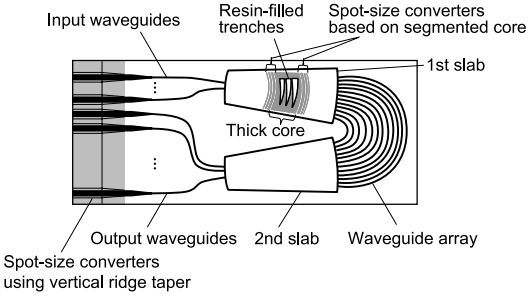


Fig. 5 Optical circuit of 2.5%-Δ athermal AWG.

2.4 Demonstration of Super-High-Δ AWG

A 16-channel athermal AWG was fabricated with 100-GHz channel spacing based on 2.5%-Δ silica waveguides [22]. The optical circuit of the athermal AWG is illustrated in Fig. 5. To obtain athermal characteristics, we introduced wedge-shaped trenches formed in the first slab and filled with silicone resin to compensate for the temperature dependence of optical path-length difference between adjacent waveguides in the waveguide array. To reduce insertion loss caused by the reduction of the spot size of a fundamental mode for super-high-Δ waveguides, we introduced spot-size converters using vertical ridge taper integrated at input and

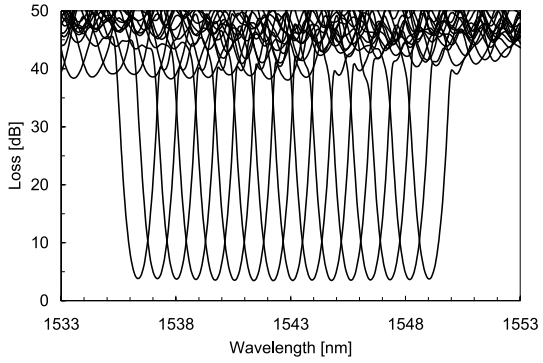


Fig. 6 Spectral responses for 16 output ports of 2.5%-Δ athermal AWG.

output waveguides to reduce the coupling loss at chip-to-fiber interface [23], and spot-size converters based on segmented core formed around the trenches in the slab [8].

The spectral responses of the proposed AWG for all 16 output ports are shown in Fig. 6. The minimum insertion loss was 3.5 dB for the central port and 3.8 dB for the marginal ports. The crosstalk was less than −34 dB, comparable to that of conventional 0.8%-Δ AWGs. The temperature-dependent wavelength shift of the module was less than 0.03 nm over 0 to 65°C, that is comparable to conventional athermal AWGs [4], [24].

3. Super-High-Δ Flat-Passband Multi/Demultiplexer Using Synchronized Routers

A combination of two synchronized routers is very attractive to obtain low-loss and flat-passband characteristics. This section describes a flat-passband multi/demultiplexer that consists of a multiple-input AWG combined with a cascaded MZI structure.

3.1 Modeling of Multiple-Input AWG

An AWG in which the interference of light from multiple input waveguides influences the passband characteristics is commonly used for demultiplexing in synchronized routers. When one needs to optimize the design of a circuit to achieve desirable performance, multiple-input AWGs often require different analytical approaches from single-input AWGs because it is necessary to treat optical amplitudes and phases from an input router. Therefore, it is essential to develop a simple and systematic design model that can treat multiple-input AWGs.

We derived the theoretical model by extending the model based on Fourier optics [25], [26] to the multiple-input AWG to systematically analyze its spectral performance [27]. The transfer function of the multiple-input AWG for the nth output waveguide located at y_n along the output-to-slab interface is derived using the Dirichlet kernel $D_N(x) = \sin(N\pi x)/\sin(\pi x)$ as

$$t(y_n; f) \cong \Delta y^2 f_b(y_n)\,[\bar{u}(-y_n) \otimes E_o(y_n; f)] \tag{4}$$

$$\bar{u}(y) = u_{in}(y) \otimes u^*_{out}(y) \tag{5}$$

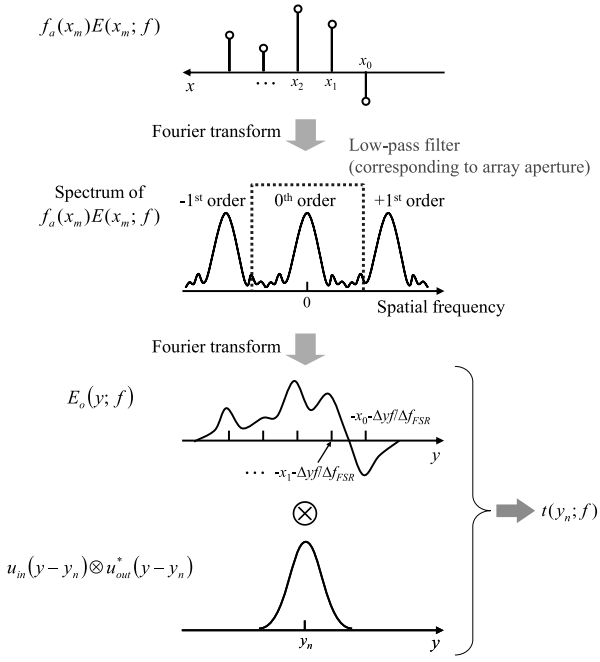


Fig. 7 Formulation of multiple-input AWG model.

$$E_o(y; f) = \sum_{m=0}^{M-1} f_a(x_m) E(x_m; f)\, D_{2I+1}\left(\frac{f}{\Delta f_{FSR}} + \frac{x_m + y}{\Delta y}\right) \tag{6}$$

where $E(x_m; f)$ is the amplitude of the light from the mth input waveguide as a function of an optical frequency f, $u_{in}(y)$ and $u_{out}(y)$ are the input and output mode field functions, M is the number of the input waveguides, $2I+1$ is the number of the waveguides in the array, Δf_{FSR} is the FSR in frequency, $f_a(x)$ and $f_b(y)$ are the images of the input-side and output-side mode field functions of a single arrayed waveguide produced on the input and output edges of the slabs, $\Delta y = \lambda_0 z/(n_s D)$ where λ_0 is the center wavelength, and $g_1(y) \otimes g_2(y)$ represents the convolution of periodical functions $g_1(y)$ and $g_2(y)$ with a period of Δy. With this formulation, we can treat discrete amplitude values of the light from the input waveguides $E(x_m; f)$ and the field distribution $u_{in}(y)$ separately, instead of treating the actual field distribution from the input waveguides to the input slab.

The formulation of the model is briefly illustrated in Fig. 7. The interpolation in $E_o(y; f)$ with the Dirichlet kernel corresponds to filtering the series of the discrete sampling values $f_a(x_m)E(x_m; f)$ with a spatial low-pass filter with the bandwidth corresponding to the array aperture. The output amplitude $t(y_n; f)$ is derived as an overlap integral between $E_o(y; f)$ and $\bar{u}(y-y_n)$. This formulation, expressed with Eqs. (4)–(6), suggests that the following two factors are important as the guidelines for flattening the passband:

- The first is smoothing the overlap integral between $E_o(y; f)$ and $\bar{u}(y-y_n)$ by sufficiently expanding the width of the mode-field function $\bar{u}(y)$.
- The second is smoothing the interpolated field function

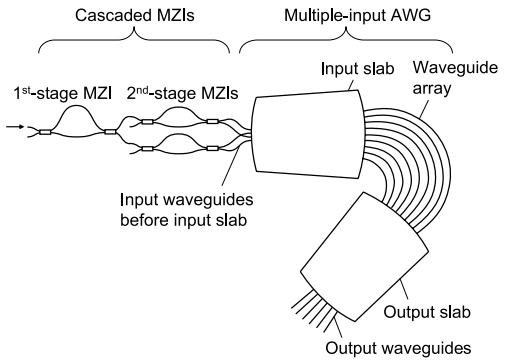


Fig. 8 Optical circuit of flat-passband multi/demultiplexer.

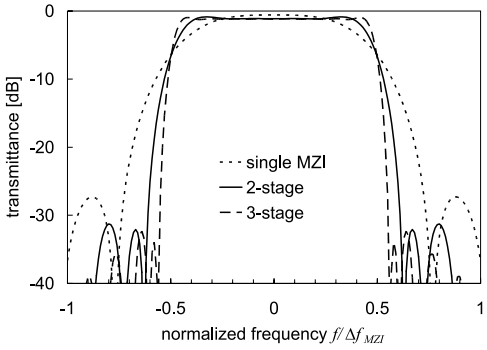


Fig. 9 Calculated spectral responses of proposed structure using 1 to 3-stage cascaded MZIs.

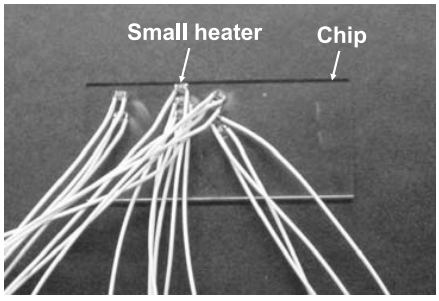


Fig. 10 Photograph of chip of flat-passband multi/demultiplexer for measurement.

$E_o(y; f)$ by sufficiently expanding the width of the main-lobe of the Dirichlet kernel $D_{2I+1}(f/\Delta f_{FSR} + (x_m + y)/\Delta y)$. This expansion is done by limiting the number of waveguides in the array, $2I+1$, and this is analogous to avoiding undersampling in reconstructing a signal from its sampling values. The interpolated function $E_o(y; f)$ is bandlimited to a spatial frequency $(2I+1)/(2\Delta y)$ from a sampling theorem for periodic functions [28], and this limitation ensures the smoothness in $E_o(y; f)$.

3.2 Flat-Passband Multi/Demultiplexer Using Multiple-Input AWG and Cascaded MZIs

The optical circuit of a proposed flat-passband multi/demultiplexer is shown in Fig. 8. The circuit consists of a multiple-input AWG and cascaded MZIs connected to the AWG input ports as an input router synchronized with the AWG. The signals from a first-stage MZI are demultiplexed with second-stage MZIs by setting the FSR of the second-stage MZIs to twice that of the first-stage MZI. The signals with four equally-spaced frequencies $f_1, \ldots, f_4$ within one FSR of the second-stage MZIs are first divided with the first-stage MZI between the two groups f_1, f_3 and f_2, f_4, and next divided with the second-stage MZIs into each signal. The lower port of the upper second-stage MZI and the upper port of the lower second-stage MZI should cross each other so that the signals $f_1, \ldots, f_4$ are spatially arranged in this order at the input slab of the AWG. To obtain an appropriate demultiplexing function, the channel spacing of the AWG was set to the FSR of the second-stage MZIs.

The transfer function for the mth output port of an L-stage cascaded MZI demultiplexer (with M=2^L output ports) is generally expressed with the discrete inverse Fourier transform form [29] as

$$E(x_m; f) = \frac{e^{j\phi_m}}{M} \sum_{k=0}^{M-1} e^{j2\pi k \frac{f+\delta f}{\Delta f_{MZI}}} e^{j2\pi \frac{mk}{M}} \quad (7)$$

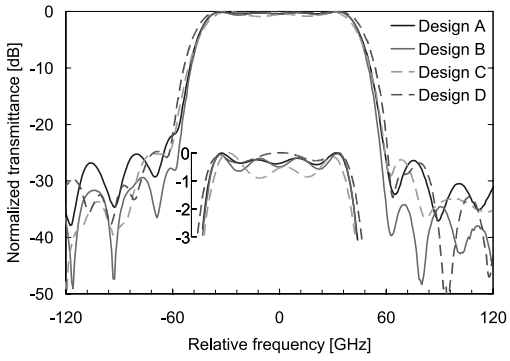
where δf and Δf_{MZI} are the frequency shift and FSR for the final-stage MZIs, and ϕ_m is the phase shift in the mth AWG input waveguide before the slab. By using Eqs. (4)–(7), the optical performance for the proposed structure can be analyzed.

Figure 9 plots the calculated spectral responses near the passband of the multi/demultiplexer using 1 to 3-stage cascaded MZIs. The passband width is increased as the number of the stages is increased. In practical circuit layout, however, the number of the stages should be limited because the circuit size directly depends on it. By optimizing design parameters, the good performance (the flatness of less than 0.5 dB and minimum transmittance of larger than −1.2 dB within the passband of +/−0.35 x (channel spacing)) is expected even if we use the two-stage MZIs.

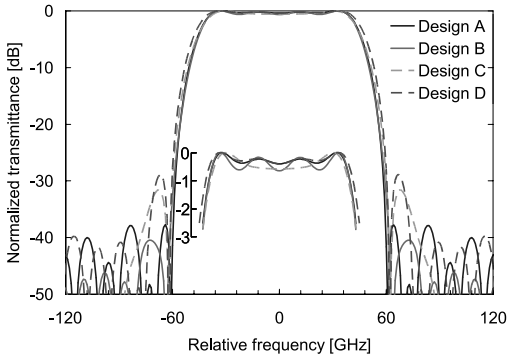
3.3 Demonstration of Flat-Passband Multi/Demultiplexer

We demonstrated a flat-passband multi/demultiplexer with 100-GHz channel spacing using a multiple-input AWG and cascaded MZIs [10], [11]. The Δ of 2.5% was used to significantly reduce the chip size from a conventional Δ of 0.8%. The typical chip size was 38.5 mm × 17 mm, which allows us to arrange seven chips on a 4-inch wafer. We fabricated chips with several different design parameters. The varied parameters were the number of arrayed waveguides, input waveguide interval, and core widths of input/output waveguides at the edges of the slabs. Figure 10 shows the photograph of the chip for measurement. Small heaters were adhered on arms of each MZI and input waveguides before the input slab. Optical phases of the MZIs and input waveguides were adjusted via the thermooptic effect by applying electrical power to the heaters during the measurement.

The spectral responses measured by TE-polarized light



(a)



(b)

Fig. 11 Spectral response for various design parameters. (a) measured response and (b) calculated response.

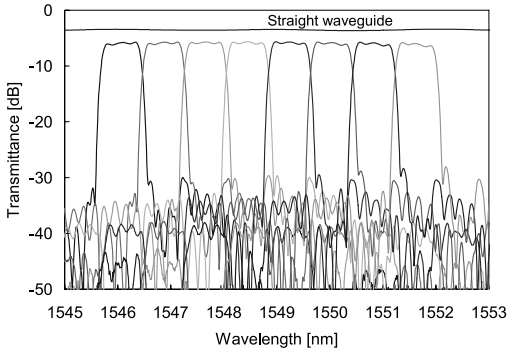


Fig. 12 Measured spectral response for central eight output ports of design D.

are plotted in Fig. 11(a) for different design parameters, and the simulation results are plotted in Fig. 11(b). The passband shape for the measured results generally agrees well with that for the calculated one in each design. The spectral responses for the central eight output ports of design D are shown in Fig. 12. We obtained very flat responses for all eight output ports. The 1-dB and 20-dB bandwidths were 0.645–0.658 nm and 0.944–0.960 nm, which correspond to figure-of-merit [18] values of 0.68–0.70. The minimum insertion loss was 5.7–5.8 dB. Comparing with the result of an input port directly connected to the AWG, the increase in insertion loss due to the passband-flattening was estimated to be as small as 0.9–1.0 dB. The total insertion loss also contains fiber-to-chip transition loss of 3.4–3.7 dB that can be reduced by applying spot-size converters to the edges of the chip.

4. Conclusion

This paper reviewed our recent progress on AWGs using super-high-Δ silica-based PLC technology and their application to integrated optical devices. Some factors affecting the chip size of AWGs and the impact of increasing Δ on the chip size were investigated, and the fabrication result of a compact athermal AWG using 2.5%-Δ silica-based waveguides was presented. Also, a flat-passband multi/demultiplexer consisting of an AWG and cascaded MZIs was presented as an application of super-high-Δ AWGs to integrated devices. Super-high-Δ AWGs will play an important role as applications to compact and low-cost passive devices for DWDM systems.

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