FOREWORD

Special Section on Low-Leakage, Low-Voltage, Low-Power and High-Speed Technologies for System LSIs in Deep-Submicron Era

Thanks to the continuous advancement in CMOS device scaling, system LSIs has achieved a great performance enhancement. The leakage current increased by CMOS device scaling is the one of the performance-limiting factors not only for mobile LSIs but also for high-speed LSIs. In addition, a low-voltage operation of these LSIs is hindered by increase of device variation. With an application of system LSIs to ubiquitous devices, low-power, high-speed technologies are in greater demand than ever before. This special section contains 1 letter and 16 regular papers.

On behalf of the editorial committee of this special section, I would like to thank all the authors for their contributions and to all the reviewers for their helpful comments for ensuring the correctness and quality of the papers. I am also grateful to Dr. Yoshiharu Aimoto, the editorial committee members and the staff of the IEICE Transactions on Electronics for their dedication to the publication of this special section.

Tadayoshi Enomoto, Guest Editor

Tadayoshi Enomoto *(Fellow)* received his M.S. and Ph.D. degrees from the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, in 1972 and 1975, respectively. In 1975, he joined NEC Microelectronics Research Laboratories where he worked on analog MOS LSI development (CCD filters, SCFs, adaptive equalizers, analog circuit scaling rules, and fabrication processes). From 1982 to 1986, he worked on a monolithic stacked IC using SOIs, participating in the Japanese national program for three-dimensional ICs. From 1984, he started work on CMOS and BiCMOS digital LSIs, including the world's first video codec processor (1987), the world's first vector processor LSI for supercomputers (1991), and a dictionary search processor. From 1986 through 1991, he directed the System ULSI Research Laboratories, researching ADCs, memories, and logic LSIs. Since 1992, he has been a professor at Chuo University, Tokyo, Japan, and his current research interests include motion-picture encoding algorithms, video encoder architectures, processors and memories for future LSIs, and high-speed and low-power CMOS LSI technologies. Dr. Enomoto has authored or co-authored five books and one handbook, published about 100 reviewed technical papers, and holds 50 patents in Japan and abroad. He has received several awards including the 1992 Best Paper Award of the IEEE Journal of Solid-State Circuits, the IEICE Outstanding Achievement Award (1995), the Best Poster Award of the Eighth System LSI Workshop of the IEICE (2004), the IEEE ASP-DAC Design Contest Special Feature Award (2006), the TELECOM System Technology Award of the Telecommunications Advancement Foundation (2006), a four-year Ohio State University Fellowship (1970–1974), three NEC R&D Awards (1982, 1985, and 1988), and six Chuo University Prominent Research Awards (1994, 1997, 1999, 2002, 2005, and 2007). He was the chairman of the IEICE Technical Group of Integrated Circuits and Devices from 1993 to 1995, the chairman of the IEICE Technical Group of Electron Devices from 1995 to 1997, and a member of the IEICE Electronics Society from 1993 to 1997. He was an associate editor (1991–1995) and an advisory member (1993–1997) of the IEICE Transactions on Electronics. He was also a special issue guest editor of the same Transactions in 1993, 1995, and 1996 and an associate editor of the IEEE Journal of Solid-State Circuits (2000–2003). He is an IEEE Fellow, a member of the Institute of Image Information and Television Engineers of Japan and an Expert Commissioner of the Supreme Court of Japan.