

Smart Front-Ends, from Vision to Design

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SUMMARY An integral multi-disciplinary chain optimization based on a high-level cascaded Shannon-based channel modeling is proposed. It is argued that the analog part of the front-end (FE) will become a bottleneck in the overall chain. This requires a FE-centric design approach, aiming for maximizing the effective data capacity, and for an optimal exploitation of this capacity for given power dissipation. At high level, this asks for a new view on the so-called client-server relations in the chain. To substantiate this vision, some examples of research projects in our group are addressed. These include FE-driven transmission schemes, duty-cycled operation with wake-up radio, programmable FEs, smart antenna-FE combinations, smart and flexible converters, and smart pre and post correction.

key words: front-end, programmable, smart, Shannon, mixed-signal, data converters

1. Introduction

Front-ends (FEs) form crucial blocks in any communication chain. This is especially true for wireless applications. Front-ends receive an antenna signal and recover the application bits from it, and vice versa. Note that in this definition of Front-end, the data converters are included. With the emergence of many new applications and standards, and the user demand to have everything done with just one single multi-purpose device, the front-end has to filter out one out of a bunch of channels, from an ever-more crowded frequency spectrum with an increasing number of interferers, and for a lot of different standards. The applications at the same time become more complex, requiring more and more data to be transmitted in the same time, and thus, higher data rates. And, to make the challenge even larger, the front-end has to be reliable, under more severe mobility conditions, its form factor has to decrease (smaller devices), and battery life time has at least not to diminish, meaning a severe reduction on power dissipation. From the transmission side we see a move upward in frequency, from the crowded lower bands to new bands around 60 GHz. That solves some capacity problems in the transmission channel, but it poses again a lot of extra challenges on the frontend, more specifically, on the analog part of the frontend, the AFE. This all causes the front-end to become the weakest link in terms of

performance versus cost (power dissipation, chip area).

From this vision, we draw four conclusions:

1. An integral, multi-disciplinary and Shannon-based view is needed, on the whole communication chain, and on the relations in the chain, which we have named client-server relations [1].
2. A FE-driven system design is required, consequently with new client-server relations [1].
3. The FE should be conversion-driven: it should primarily focus on its fundamental 'IC-channel modulation' function, which is data conversion [2].
4. Front-ends need to become smart: comprise intelligence to adapt and optimize themselves under varying application, system, user and environment conditions [2], [3].

The research in our group is driven by this vision. This invited paper substantiates this vision by addressing some of our activities. The paper is set up as follows. In Sects. 2–4 we discuss the high-level concepts, in Sects. 5–9, several sub issues of our vision will be elucidated with activities, and, finally, conclusions are given in Sect. 10.

2. Shannon-Based View and Chain Modeling

Shannon and Hartley gave the well-known formula for the capacity C of a channel, see Fig. 1.

This capacity can be increased by increasing B and/or SNR; both require power and chip area because of physical laws. However, having this capacity is not enough; we should also exploit it by using appropriate modulation and coding. Finally, part of the capacity is consumed by margins that are taken into account in the design, to cover system imperfections (imperfections and constraints in processing, modeling, PVT, coding, signal processing, etc.), and interfering signals. Uncertainties, limited knowledge, but also costs are underlying reasons.

Hence, in view of the increase in data rates, we need to:

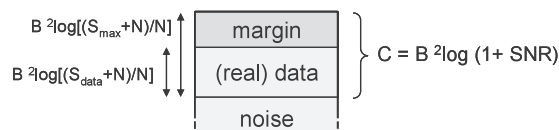


Fig. 1 Effective data capacity, as a part of the Shannon capacity.

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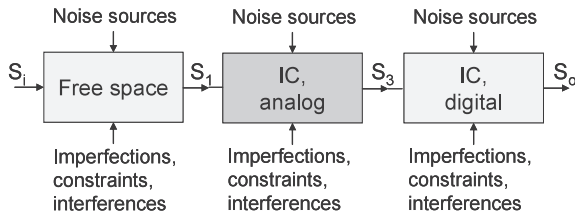


Fig. 2 A cascade Shannon model for the chain.

- 1) increase the capacity C ;
 - 2) exploit the effective capacity optimally; and
 - 3) decrease the margins;
- and all these issues cost power . . .

Expanding this model for the overall transmission chain leads to Fig. 2: a cascade of ‘transmission channel,’ analog-IC channel, and digital-IC channel. The analog-IC part will become the weakest link, in view of the trends addressed in the introduction, and of the following observations: any increase of capacity in free space is paid for by the transceiver in terms of power; with technology scaling, the capacity of the digital IC will increase whereas that of the analog IC part will decrease; and the required margins increase, especially for the analog part (more interferences, more parasitic effects at higher frequencies, more modeling uncertainty, etc.) [1]–[3].

3. FE-Centric Design Approach

With the analog-IC link being the bottleneck, we need a FE-centric design approach that primarily focuses on fighting this bottleneck. That can be done at system level, by optimizing the overall chain, by proper high-level partitioning and by defining proper ‘client-server’ relations (Sect. 4).

Following that line, we can define transmission schemes that are driven by the requirements of the FE, thus aiming for maximizing the capacity/cost of the AFE’-channel link, and on maximizing the exploitation of the capacity. Examples can range from choice of modulation type, to wake up radio, and cross-layer optimization (Sect. 5).

Complementary, we can tackle the margin problem to enhance the effective data capacity, and at the same time optimize the effective use of it. This path goes from programmable FEs, that can be adapted by the user to changing conditions (Sect. 6), to, finally, smart FEs, that can eliminate uncertainties by self-measuring, and that can autonomously adapt their operation, thus decreasing the margins, and increasing the ratio between effective data capacity and power dissipation. Examples will be given of smart antenna-FE combinations (Sect. 7), smart and flexible data converters (Sect. 8), and smart pre and post processing (Sect. 9).

4. FE-Driven System-Level Chain Design

To optimize the chain in favor of the weakest link, we first need to split the whole (hardware) chain into three parts, according to the previous split in the Shannon model of the

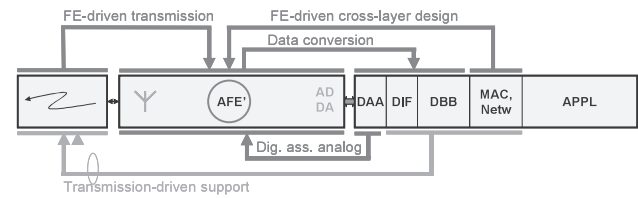


Fig. 3 Chain with client-server relations.

chain. To do so, we need to consider the usually individual blocks antenna, AFE and AD/DA, as one functional block AFE’ with its primary focus on converting analog EM-fields to bits and vice versa. Figure 3 visualizes this view on future communication chains, with successively free-space transmission, AFE’, and digital processing block. The latter digitally assists the analog block (DAA), and provides digital IF (DIF), digital baseband (DBB), MAC, network, and application processing.

Next in the optimization of the chain, the AFE’ should be seen as a client that needs to be supported maximally by the other links of the chain. That brings us to new ‘client-server’ relations [1], represented by the arrows in the figure, where the AFE’ focuses on data conversion, which in fact comprises fundamentally all functionality required to change the input signals (EM fields) to the IC-optimized signal representation (the digital one), and vice versa, so to optimize for the IC-channel. For that purpose, the AFE’ should be optimally supported by the digital DAA block and the MAC/Network layer, and a front-end efficient transmission scheme should be defined. Modulation support for the free-space transmission (‘Transmission-driven support’) is shifted from the AFE’ to the digital block as far as it is not in line with the optimal conversion function [2].

5. FE-Driven Transmission Schemes

Defining optimal transmission schemes from a FE point of view, that minimize the cost for the AFE’, helps considerably in reducing the AFE’ bottleneck. Three examples will be given here.

5.1 FE-Driven FHSS Modulation

Wireless sensor networks must often work in a very hostile indoor environment. As any other channel medium, the indoor environment is noisy. The often used Industrial, Scientific and Medical (ISM) bands, like the 2.4 GHz and the 915 MHz bands, present an interference-crowded scenario which requires the capability to discern a weak transmitted signal among several stronger unwanted signals. Finally, the presence of objects creates a multipath interference, which translates in a spatial degradation of the SNR. This degradation can be as large as 20 dB or more and is often referred to as fading. These requirements make FE design quite tough. However, though the environment parameters are dictated by the application area required to be covered and they cannot change, several other parameters can be optimized in

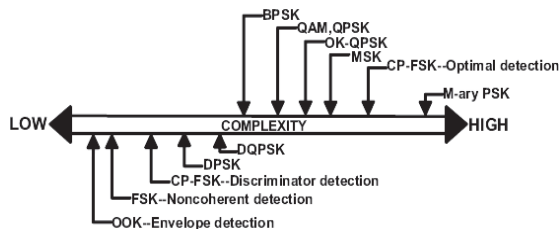


Fig. 4 Relative complexity of various modulation schemes [4].

order to minimize the impact of those non-idealities on the transceiver complexity and power consumption. Some of those parameters are the following:

- modulation format;
- system bandwidth;
- data transmission rate;
- transmitter/receiver architecture.

A FE-driven modulation format should be used to encode the information. The relative modulation complexity of various modulation schemes is shown in Fig. 4. In terms of AFE' power consumption a robust, simple and constant-envelope modulation scheme is preferred. Phase-modulation schemes are constant envelope before filtering (adjacent channel filtering), but not anymore after it. This forces the PA to back-off during transmission reducing the PA efficiency. On-off keying (OOK), though very simple, is very weak in the presence of strong interferers [4]. Therefore, an FSK modulation format is the most suitable for this scenario. Furthermore, though a coherent FSK has a 3 dB SNR advantage over a non-coherent (NC) FSK, the much lower complexity of NC-FSK allows for a larger reduction of the overall power consumption.

The choice between narrowband and wideband FSK is also FE-driven. For the receiver, in order to save power and area, a zero-IF topology is preferred. Unfortunately this suffers from some non-idealities producing a DC offset. In order to easily reject it, it is preferable that the signal has no information around DC. Therefore, a wideband FSK is an optimal choice for a zero-IF receiver.

System bandwidth (bandwidth used on the average for the data transmission) and data rate can also be FE-driven. First, we divide between narrowband and wideband systems. The so called spread-spectrum (SS) systems form a specific class of wideband systems. They allow to trade bandwidth for robustness, assuming low data-rate transmission, generally ranging between 1 kbps and 50 kbps. Moreover, as a narrowband filter can be used, the amount of noise is very low. Therefore, for a given SNR required by the modulation format, the transmitted power can be drastically reduced. Two main SS techniques are generally used: Direct Sequence SS and Frequency Hopping SS. A DSSS system is intrinsically a wideband system. Therefore, for a given processing gain (PG), the filter will have a bandwidth equal to PG times the modulated bandwidth. An FHSS system, though wideband on the average, is narrowband when a single time slot is considered. Therefore, robustness to interfer-

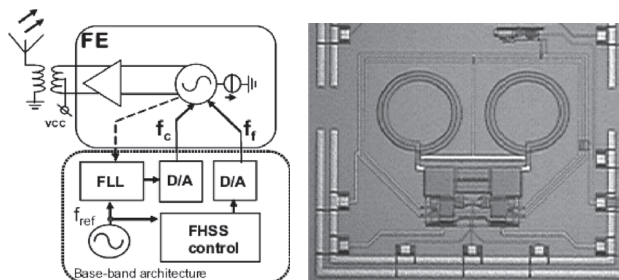


Fig. 5 Diagram and IC photograph of a direct FHSS transmitter [5].

ers and fading is guaranteed by its on-the-average wideband behavior, while selectivity and low noise is assured by its instantaneous narrow-band behavior, allowing narrowband channel filtering. Furthermore, an FHSS system can trade-off transmitted power for hopping speed, which gives another degree of freedom on reducing the overall power consumption.

The transmitter architecture is also very important in order to optimize the overall system. The chosen modulation scheme allows a very simple way to transmit the wanted data, viz. by direct modulation of a high-frequency VCO. In this way no up-conversion stage is required. Moreover if we combine the oscillator with the PA it is possible to have a system which nearly uses all its power to transmit the data and only very little power for data processing. The schematic diagram and IC photo of such a system is shown in Fig. 5. More details can be found in [5], [6].

5.2 FE-Driven Cross-Layer Design

Transmission need not always be done in a continuous way. If done duty cycled, we have the option to power down the transceiver, which helps to reduce the averaged power dissipated per bit transferred, especially for the receiver. We can use transmission schemes that allow transmission-signal-level duty cycling, like impulse radio, where a receiver can be powered down when no impulse is sent, or data-level duty cycling, where the transceiver is powered down when no data is sent. With data-level duty cycling we further can reduce power by increasing the data rate, so as to decrease the data-burst transfer time and thus the power-on time. Of course, for the receiver blocks where power dissipation is proportional to the data rate, this will not help, but for many receiver blocks it does (like e.g. PLLs), making this option very valuable from an AFE'-centric approach. A further improvement might be obtained by letting the transceiver be wakened up by a separate 'wake up radio' that is optimized for this function only, instead of leaving this to the transceiver. However, that also entangles the PHY layer design with the MAC/Network layer (Fig. 3), as the power dissipation is strongly dependent on protocol issues like preambles, and pilot tones. By using all these options, energies/bits in the order of 10 nJ/bit can be achieved. In [7] this is further elaborated. Figure 6 shows a wake-up radio in parallel to a 60 GHz (beamsteering) receiver.

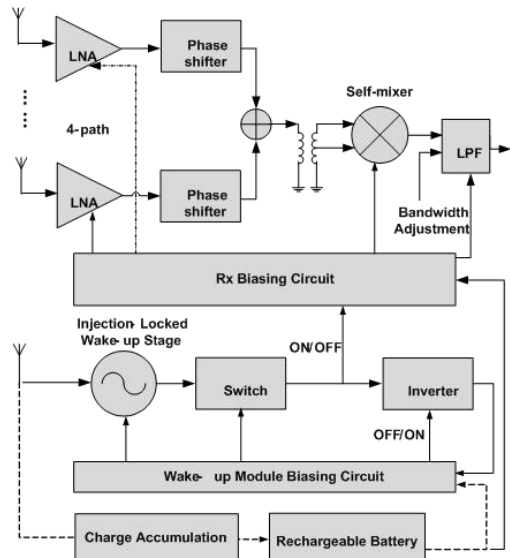


Fig. 6 60 GHz beamsteering receiver with wake-up radio.

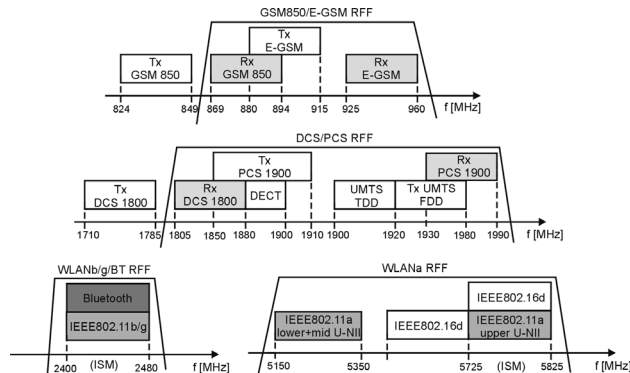


Fig. 7 Standards and frequency bands covered.

5.3 Electronic Beamsteering FE

Electronic beamsteering is another option to combat the AFE' bottleneck. Spatial selectivity, provided by the beamsteering, provides higher SNR and decreased interferer level, thus alleviating the problem for the AFE' considerably, but at the same time it requires extra hardware in the AFE': parallel paths, phase shifters, and control [24]. As this option requires an optimal antenna-FE design and a smart FE that can autonomously perform self-steering, it will be further addressed in Sect. 7.2.

6. Programmable FEs

Besides trying to optimize the capacity and to exploit this maximally, we can tackle the margin problem to enhance the effective data capacity, and at the same time optimize the effective use of it. As a first step we discuss in this section programmable FEs that can be adapted by the user to changing conditions. In further sections we will address smart FEs.

In the research addressed in this section, the channel is made programmable to make it suitable for a lot of standards. The main problem is the wide frequency band (with its associated problems like power, linearity and interference) covered in total by the various standards, see Fig. 7. A straightforward option is to convert the whole frequency band and also the full signal range covered by the standards and do all transmission functionality in the digital baseband; this leads to a lot of noise (so decreased capacity in the analog part), to non-optimal use of the capacity (non-optimal signal conditioning), and to large margins (to cover all linearity and interference problems that come along with such a wideband approach); it is thus in all aspects very inefficient in power dissipation and area. Alternatively, we can

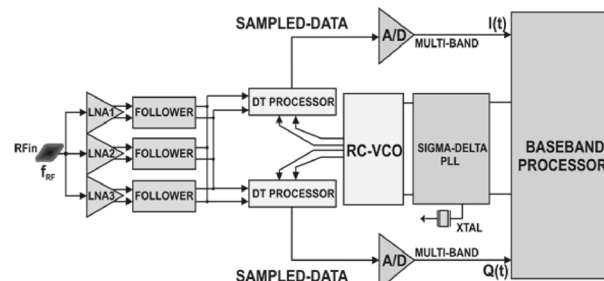


Fig. 8 A three sub-wide band channel solution.

split into parallel channels, each optimized, and switch on only the one used (or multiple channels, in case of concurrent operation). This costs a lot of area. Making the analog functions programmable, as a function of the actual situation, seems a more reasonable solution. Adjusting the analog building blocks can be done in design, performance, and parameter space [8], [9]. Especially for high speed analog circuits, this is difficult without introducing extra impairments and extra costs.

Here we have chosen to combine these options, and to do the programming gradually at the various parts of the AFE, in such a way that the channel adaptation is optimally distributed over the chain inside the AFE, see Fig. 8 [10], [11]. First, the frequency selectivity is distributed over three stages: we split the full wideband that covers all the standards to be received in sub bands, each still wide, but nevertheless narrower than the original band, see Fig. 7.

The three paths respectively treat the GSM and DCS/PCS bands; the WLAN-b/g and Bluetooth bands; and the WLAN-a bands and the IEEE 802.16 bands. The assumption made here is the presence of RF selective filters in front of the LNA for relaxing the linearity requirements of the front-end.

The LNA circuit is shown in Fig. 9; the bond inductance is used to compensate parasitics and to match the sub-wideband. As no narrow-band selectivity is chosen, we can do without the area-consuming inductors. Next, we provide some further selectivity with the discrete time signal processing block (Fig. 8) that provides a tunable bandpass filter with poly-phase filters and mixers, for multi-mode and

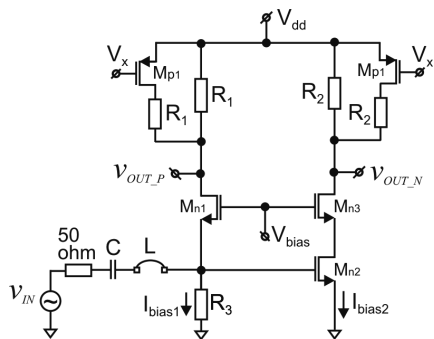


Fig. 9 LNA for ‘sub wide band’ with programmable gain.

multi-band receiver IF selectivity [11]. A PLL suppressed the noise of the RC oscillator, to fulfil the required timing selectivity requirement. The selectivity steps are meant to optimize in terms of Shannon capacity: to decrease the margins, by suppressing the interferers, and to optimize the capacity by reducing the noise. Next, we do the conversion. Final channel selectivity is left for the digital baseband processor. Besides selectivity programming, we need signal range programming. This is done in only two steps: first in the LNA, see Fig. 9; next in the digital baseband processor.

7. Smart Antenna-FE Combinations

A further optimization of the effective data capacity is achieved by making the FEs smart. Two examples of smart antenna-frontend combinations will be given in this section. One addresses smart autonomous adaptation of a FE to fluctuating antenna-FE mismatch. The other example addresses the use of smart beamforming.

7.1 Smart Antenna-FE Matching

Link quality of cellular phones suffers from antenna mismatch caused by the narrow bandwidth of miniaturized high-Q antennas and by detuning of the antenna resonance frequency [12] due to fluctuating antenna-user interaction and changes in phone form-factor. Mismatch of the antenna impedance results in reduced maximum field strength and deteriorates modulation quality [13], receiver sensitivity and power amplifier efficiency. Adaptive antenna matching techniques [14]–[18] are being explored that automatically compensate mismatch. Such smart RF front-ends are attractive because they dynamically optimize the signal conditions at the interface between transmission channel and analogue front-end [1], by minimizing reflection losses. Capacitive RF-MEMS switches [19]–[22] are used as tunable matching elements to meet the very demanding requirements on linearity, insertion loss, and tuning range.

Antenna-user interaction causes mainly a down shift in the series resonance frequency of planar inverted-F antennas (PIFA) that are often used in mobile phones. We apply a tunable series-LC network, depicted in Fig. 10, for

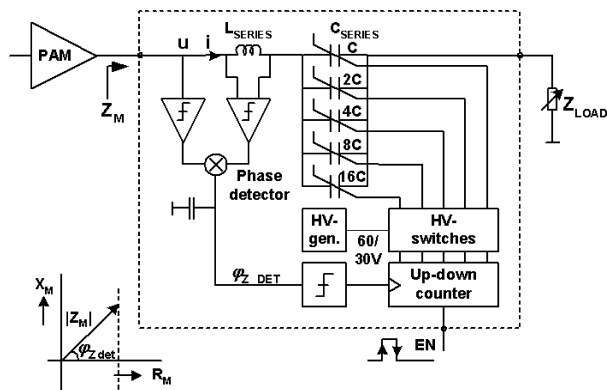


Fig. 10 Block diagram of an adaptively controlled series-LC matching network. It compensates the reactive part of the load impedance by controlling the detected phase $\varphi_{Z\text{DET}}$ of the matched impedance to zero.

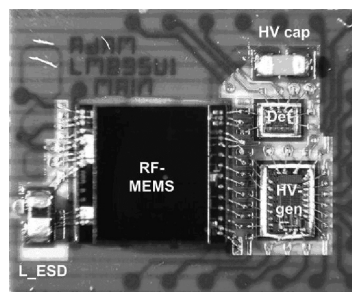


Fig. 11 Photograph of the adaptive antenna matching module showing the packaged RF-MEMS, high-voltage generator, and impedance phase detector die.

impedance correction because it is the simplest network that effectively compensates the resulting inductive antenna behavior. The adaptive tuning system comprises a tunable 5-bit switched capacitor array, high-voltage MEMS biasing switches, a high-voltage generator, a phase detector, and an up/down counter.

Mismatch information is derived from the phase of the matched impedance Z_M at the network input, which is given by the phase difference between the input signals u and i . Both signals are hard limited and applied to a mixer to obtain the phase $\varphi_{Z\text{DET}}$ [23]. Depending on the sign of the detected phase, the counter output, and hence the switched capacitor array, will either be increased or decreased in steps of 1LSB (least significant bit). Consequently, the loop controls the phase of the detected impedance $\varphi_{Z\text{DET}}$ to zero, step by step, keeping phase transients of the transmitted signal small. The photograph in Fig. 11 shows the adaptive antenna matching module that consists of a Si-capped RF-MEMS array, a detector, and a high voltage generator die mounted on laminate.

The variable capacitor is realized as a 5-bit binary weighted switched capacitor array as depicted in Fig. 12. Each bit is activated via a bias control line b_i . The resistors R provide RF-isolation and have high impedances to minimize insertion loss.

Hardware evaluation proves the module to meet all

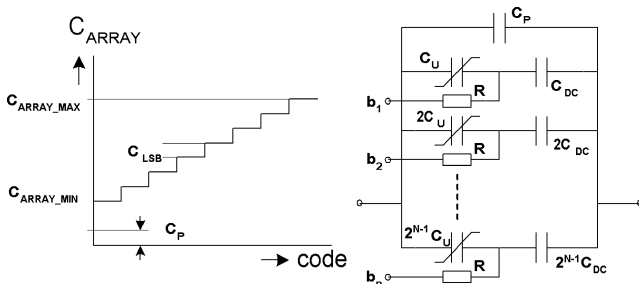


Fig. 12 Binary weighted RF-MEMS switched capacitor array, including DC-block capacitors and bias resistors, and its corresponding control curve.

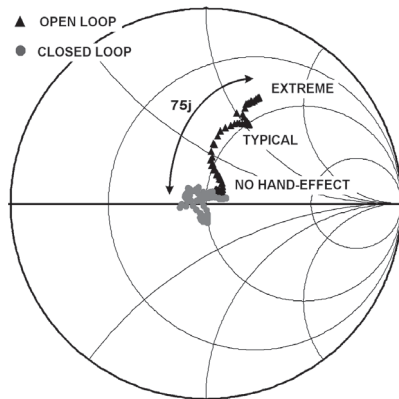


Fig. 13 Measured input impedance of the module when connected to a PIFA that is influenced by hand-effects, for open loop and closed loop conditions. $f = 900$ MHz.

GSM/EDGE/WCDMA linearity requirements. Adaptive control of the complete module, connected to a planar inverted-F antenna (PIFA), has been verified. When a hand is moved towards the PIFA, the module input impedance remains close to the center of the Smith chart in closed loop condition, whereas the impedance shifts away in open loop condition, as depicted in Fig. 13. For extreme hand-effects the maximum correction is $-75j\Omega$. Hence, the module corrects antenna impedance disturbances as expected.

7.2 Smart Beamforming

As discussed already shortly in Sect. 5, beamsteering is a very effective way to provide extra selectivity (in the spatial domain, thus providing antenna gain) and decrease of interferers (so high signal gain and selectivity). If the zeros in the antenna radiation pattern are put in the direction of the interferers, a high suppression of them can be achieved. However, this requires both electrically programmable beams and a smart control. Here, we will limit us to our research on electrically-controlled beamforming with the use of a phased antenna array, in the context of transmission at high frequencies (60 GHz), where the antenna dimensions, and the distances between the antennas in the array, can be kept small. Figure 6 already showed a beamsteering receiver (in conjunction with the wake up radio that was discussed), and in [24] several phase shift architecture options, and a series-

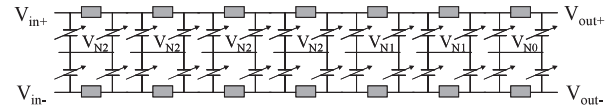


Fig. 14 Circuit diagram of 4-bit phase shifter.

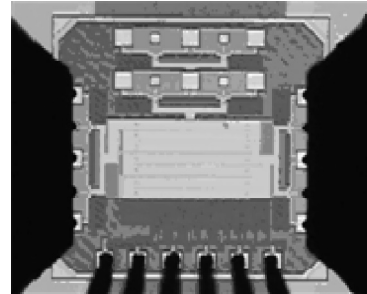


Fig. 15 Microphotograph of 4-bit phase shifter.

tuned phase shifter are discussed. In [25] a 4-bit controlled varactor-loaded differential transmission-line phase shifter is described, implemented in 65 nm CMOS, to achieve a phase resolution of 22.5° .

Figure 14 shows the circuit diagram. Each varactor is controlled by just one bit, placing the varactor at one of the two insensitive ends of its voltage range. The differential operation of the varactor keeps the well at virtual earth, making it quite insensitive to parasitics. The 7-bits thermometer-code control for the seven stages is decoded from the 3 LSB PCM bits. The MSB PCM bit controls a swap, thus providing a corresponding 180° phase shift. The whole phase shifter, see Fig. 15, occupies only 0.2 mm^2 .

8. Smart and Flexible Data Converters

For the data converters, too, it holds that smartness can decrease the margins and increase the ratio between effective data capacity and power dissipation (Fig. 1). In [2], [3] it is described how smartness can be applied in various ways, both to combat various problems like interferences and technology spread and dependence, and to optimally adapt to and cooperate with the rest of the chain, system, user and environment. The margin can also be reduced by adapting the conversion (and the whole system) to the application, which requires flexibility. In this section we will first address examples of smart and flexible DA converters, and next give an example of a flexible AD converter.

8.1 Smart and Flexible DA Converters

A first approach to smartness, to improve the performance in a DAC, is to calibrate the individual current sources, on-chip, and autonomously. The conventional way, and also our first step, is to do that for the unary currents in a segmented converter [26], leaving the binary currents uncalibrated, and hence leaving the converter partly dependent on architecture (choice of segmentation) and technology. A better approach is to include the binary currents in the calibration.

A methodology for calibrating binary currents is proposed in [28]. The basic idea is that two (or more) sets of binary currents are available, by just copying the binary set, or by splitting each individual binary current source in two.

In [28]–[30] both the algorithm and a fully integrated DAC, with self-calibrating unary and binary current sources, are presented (Fig. 16). Four individual DACs are preceded on-chip by a programmable digital preprocessing block that provides smartness and flexibility: depending on a chosen mode of operation (op-mode) it redistributes the input digital word $w(nT)$ among the sub-conversion branches. The four DACs on the chip together can e.g. be seen as one DAC with an unconventional segmentation (four main segments, each of them unary/binary segmented), which provides flexibility and redundancy in current-source combinations. This has been exploited to achieve both unary and binary calibration, making the (static) performance of the DAC completely independent of architecture and technology.

The flexibility and redundancy in this DAC architecture can also be exploited by finding, via on-chip measurement facilities, from all redundant combinations the best sets of combinations (‘optimal mapping of codes to current sources’), such as to minimize e.g. the INL (static performance) or SFDR (dynamic performance), see [30]. In earlier work [31] we introduced a mapping technique that, applied to a set of thermometer current sources, showed an improvement in SFDR of about 30 dB for a linear distribution of errors, and 20–25 dB for a random one. Again another option is to randomize the combinations (‘shuffling’), thus randomizing the errors, which minimizes the distortion components.

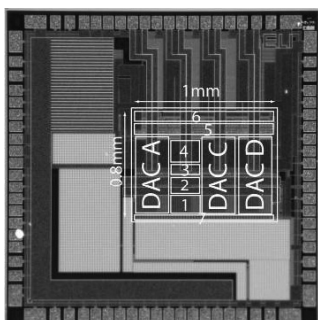


Fig. 16 Smart and flexible DAC.

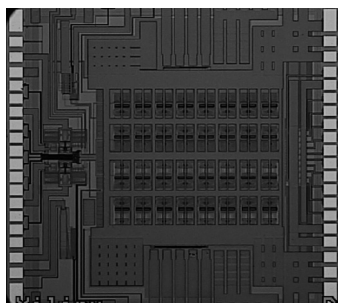


Fig. 17 Flexible AD architecture.

Finally, the flexibility can be exploited to achieve flexibility at application level (like user programmable choice of the number of DA conversion functions, the resolution, and the power dissipation), which facilitates the use of this DAC on programmable chips, like multistandard/multimode chips or even FPGAs.

8.2 Smart and Flexible AD Converters

An example of a flexible AD converter is given in [32]–[34]. This converter is built up in an ‘FPGA-like’ way, see the chip photomicrograph in Fig. 17, with basic modules (residue stages) that can be combined in various ways, so as to provide the structure of choice, like pipeline, time-interleaved or cyclic structure; to parallelize units to optimize the signal to noise ratio; or to minimize the power dissipation for a given speed. Also, several independent ADs can be configured in parallel. This makes this approach such flexible that it can be used as a component in programmable chips, like the general purpose FPGAs.

9. Smart Pre and Post Correction

Margin reduction, and thus improvement of effective data capacity (Fig. 1), can also be achieved by compensation of distortion errors by means of pre and post processing.

9.1 Smart Digitally-Assisted Analog Pre-Correction

In [35], [36] a method for the on-chip measurement and analog correction of gain errors, offsets and non-linearities of the T&H circuit of an ADC was presented. The T/H was made programmable in the analog domain and digitally assisted, to correct for (matching) errors in e.g. an interleaved AD converter, see Fig. 18. The method does not require an accurate reference source nor an accurate measurement device.

9.2 Smart Digital Post Correction

Digital post correction at baseband, e.g. for AD converters is well known and widely used. An example of post correction of the aforementioned T&H in the digital domain is given in [37]. A further integration of post correction with the chain, especially with the IF or RF part of it, is less straightforward.

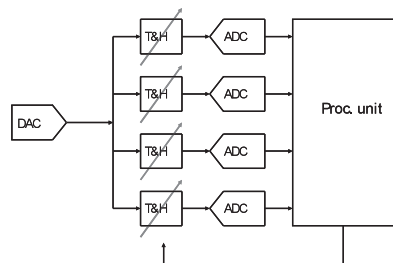


Fig. 18 Digitally-assisted programmable T/H's.

A prerequisite then is a proper estimation and a modeling of the impairments at RF/IF level to their influence at baseband where it is to be corrected. In [38] this baseband modeling is done for I/Q imbalance, DC offsets and non-linearities in the IF part between mixer and AD converter. Conventional distortion metrics, like 1 dB-compression point and IP3, are not suited for this purpose. Instead, a bounded Taylor series is used to describe the signal, and all potential distortion products (limited by the bound on the Taylor series), with assumed independent phases, are taken into account and translated to a parameter matrix in a baseband model description. The parameters, describing the amplitudes of the individual distortion components, can be estimated during pilot tones that are sent out in preambles, and used to correct the linearity of the system by means of an inverse non-linear characteristic in a post-processing block. The final parameter values can also be mapped back, finally, to the conventional parameters, to ease their interpretation.

10. Conclusions

Future transmission chains require an integral multi-disciplinary chain optimization, both over the hardware chain and across various OSI layers. A high-level Shannon view in combination with trends reveals that the analog front-end will become a severe bottleneck, and that this asks for a new FE-centric view on the partitioning and on the client-server relations in the overall chain. Antenna, analog FE and converters should be seen as one function: optimal translation of the incoming signals into relevant bits, and vice versa. A smart-FE approach is required to fight the increase in margins and thus to increase the effective data capacity of the channel, and to optimize the utilization of this data capacity. Several examples have been shown to concretize it.

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