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Evolutional Trend of Mixed Analog and Digital RF Circuits

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SUMMARY This paper describes recent technology trend of mixed analog digital RF circuits. With the progress of CMOS technology, large-scale digital signal process and control function can be integrated in an RF integrated circuit and some analog signal process blocks can be translated to digital signal processing units. At the same time, the design of remaining analog functional blocks becomes very hard. In this paper, those integration techniques for receiver and transmitter in these 20 years are reviewed. As a typical example of digital assisted systems, synthesizer based transmitters are discussed in detail.

key words: *RF, analog, digital, transmitter, receiver*

1. Introduction

With the progress of finer CMOS technology, transceiver ICs and tuner ICs are being integrated both of which conventionally existed as independent ICs and this trend is remarkable particularly in recent years. In Table 1, the trend of integration is shown taking a mobile phone as an example. In the GSM (Global System for Mobile Communications) mobile phone whose current number of shipment is the largest, not only the integration [1] of the RF transceiver and the base-band MODEM, but also the so-called "1-chip solution" by the integration [2], [3] of various kinds of interfaces including audio interface or other analog interfaces is being promoted.

While on the other hand, in the high-end field including HSPA (High Speed Packet Access) and the like, not only the improved basic characteristics such as lower power consumption, support for scaled-up RF circuits such as support for diversity, loading of receiving circuits and the like is being progressed. With these, the main stream is now combining with BBMODEM interposing digital interface [4]. In any product groups, with the progress of integration, the number of the cases has been increasing in which a large number of digital circuits is utilized and the digital circuits are strongly applied even to RF circuits that were conventionally made up only of analog circuits. Digital clock oscillator (DCO) technology [1] and calibration technology [5], [6] can be exemplified as its examples. In this paper, the process of digitalization of the RF circuits is interpreted as 1) CMOS of the RF circuits as the previous stage and 2) the fusion of the RF circuits on the fine CMOS circuits and the signal processing technology, followed by reviewing the overall trend, thereafter reviewing the recent technical trend particularly taking synthesizer based transmitter as an example.

Table 1 Resent integration trend of mobile phone applications.

Current Volume Zone Productions: 1Chip Radio (RF & MODEM) — Current Emerging Production: RF LSI with digital Interface+ MODEM

Standard	GPRS	EDGE	W-CDMA	HSPA	3.9G	4.0G
Data Rate(bps)	~115k	~384k	~2M	~14M	~1G	>1G
Modulation	GMSK	8-PSK	QPSK	16QAM	OFDM /SC-FDMA	OFDM /SC-FDMA
BBMODEM Process*	90n	65n	····· 65nm, 45nm, 32nm ·····▸			
BBMODEM Vdd (V)	1.2V	1.0V	····· 1.0 V or Bellow 1 V ····▸			

2. Trend of Integrated RF Circuits [27]

In Table 2, the progress for the technologies supporting RF products since 1990s is shown. In the global arena, many of the RF technologies in 1990s have been led by mobile phones represented by GSM. While in Japan, the circumstances have been a little different in that many circuit technologies have been developed by PHS that played a leading role. In the former 1990s, before CMOS, the main challenging issue used to be making transceiver function into 1-chip, the circuits themselves were on the developing stage, and in the circuit mode, rather than the one suitable for integration of channel filters including direct conversion mode in later years, the one to which external filters are applied including super heterodyne mode and the like were made into practical use. However, ahead of these circumstances, trial for realizing the direct conversion receiving circuit [9] by CMOS were made, which should be noted. In addition, regarding CMOS at that time, with a view to improving RF gain at first, consideration for integrating spiral inductors [10] was started. Also, the suggestions were made for improving Q of VCO inductors such as utilization for bonding wires [11].

In the later 1990s, although the situations of the application were not changed, with the refinement of the processes, the performance of the element circuit was enhanced, which enabled the integration of LNA [12].

In the meantime, synthesizers independent so far were to be integrated to transceivers. In addition, with the popularization of GSM, off-set PLL [13], [14] became popular specializing in GMSK modulation that is one kind of FM modulations employed in the GSM.

With the advent of 2000s, applications have expanded the horizons to Bluetooth, W-LAN, UWB without restricted to the mobile phones. Direct conversion receiving circuits

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Table 2 Evolution of RF circuits.

	Receiver	Transmitter	RF Building Block	Application
-1995	Super Heterodyne	2-step transmitter	Synthesizer Spiral Inductor VCO	GSM CDMA PHS,PDC
		Transceiver IC		
1996-2000		Offset PLL	On chip LNA On chip synthesizer	
2001-2005	Direct Conversion Low-IF Receiver	Direct Conversion ΔΣ Polar-Loop	On chip VCO Mixer	GSM WCDMA W-LAN Bluetooth UWB Digital TV
2006-2010	Sampling Receiver	ADPLL LINC etc.	From VCO to DCO Low Voltage Operation Digital Assisted Calibration Inductor Less LNA	
	Digital Inter face			
	Complete 1 chip Transceiver LSI (Including BBMODEM and Power management etc.)			
2010-	Software Defined Radio、Cognitive Radio RF System as ASIC Library			LTE 4G

[15]–[17] and low IF receiving circuits [18] have been made into practical use and into wider use. In particular, many of the low IF-receiving circuits have been used as a mode for avoiding the influence of 1/f noise of the CMOS. Regarding transmitting systems, many modes have come to be used practically and other than direct conversion transmitting circuits, polar-loop transmitting circuits [19]–[22], in which AM modulation including negative feedback function to the earlier mentioned off-set PLL, the mode for directly modulating power amplifier [53], and the like have been made into practical use.

Among them, ΔΣ transmitting circuits [23] utilizing fractional synthesizers and modulating division ratio of a divider via ΔΣ modulation have also been practically used. Although the principled reviews for these new circuit modes were already made in 1980s to 1990s, the practical uses thereof have not been made until the realization of higher integration and high-speed motion by the refinement of the processes. These modes were to be further evolved into DCO circuits.

In the later 2000s, performance degradation caused by the temperature of the analog characteristics and the varied processes that these modes have was to be calibrated by the digital control, and the characteristics have come to be realized which had not in the past due to the element sensitivity. Toward 2010s, the technologies for supporting 3.9 G and 4 G mobile phones with improved data transmitting speed are becoming important and so are the cognitive technologies utilizing high-integration digital circuits and supporting many communications infrastructures. In addition, the development of the technologies for realizing highly performing analog circuits (mixers [24], VCOs, filters, and the like) under the restricted supply voltage of not greater than 1 V with progressed refinement such as 45nCMOS and the like remains to be a big challenging issue.

3. Integration of Receiving Circuits

In discussing CMOS and the digitalization of receiving circuits, the integration of mixer circuits [25] as one of the main configuration circuits is extremely important. A Gilbert-type mixer applying CMOS shown in Fig. 1 can realize gain and linearity at the same time. However, when applied to a direct conversion-type receiving circuits [27] applied as many receiving circuits for cellular communication, 1/f noise overlaps with the base-band signal, thereby causing the problem of S/N degradation. For reducing the influence of the 1/f noise, 4FET mixers shown in Fig. 2 are widely applied. These operate FET in a linear operation region and a drain and a source are set unpotentially. By setting unpotentially, in principle, no 1/f noise is generated since direct current is not carried to FET. In Gilbert-type mixers, when LO signals are set with current set above a certain level, conversion gain is saturated and becomes less sensitive to LO signal level, while in 4FET mixers, saturation is hard to LO signal level, and so care should be required in setting LO levels. Recent study [26], [27] has shown that noise characteristics greatly change with the existence of overlapped regions of on-state and off-state of the LO signals and local signals as shown in Fig. 3 have come to be used.

Thus, in parallel to the development of mixer element circuits, as circuit modes as countermeasure for reducing 1/f

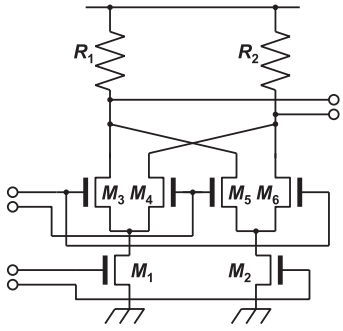


Fig. 1 CMOS Gilbert mixer.

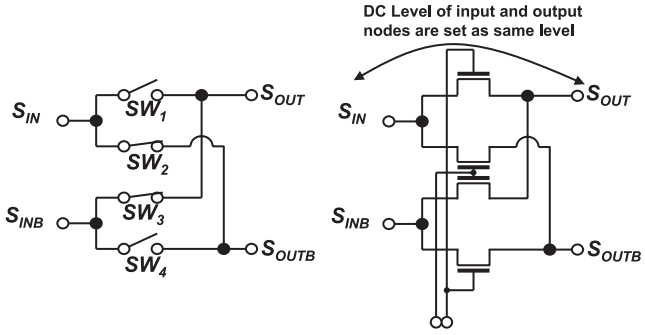
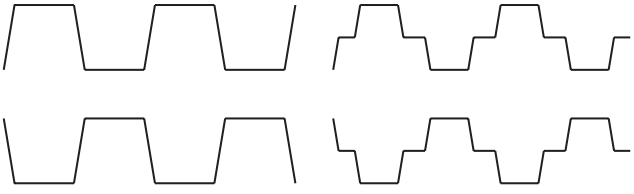


Fig. 2 Circuit diagram of 4FET switching mixer.



(a) Conventional Clock (b) Non-overlap Clock

Fig. 3 Local clock waveform evolution.

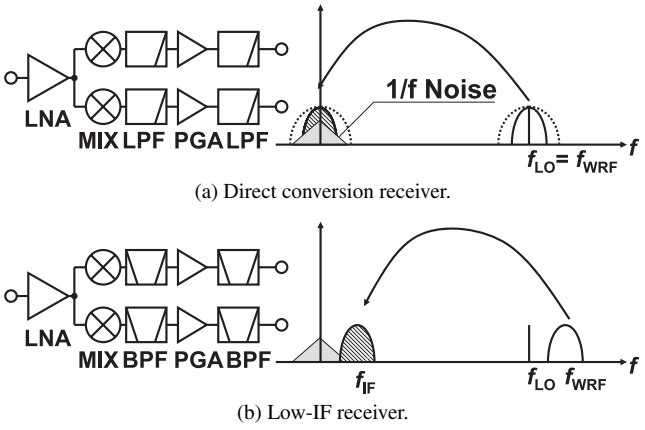
noise, low-IF modes [18] are being considered.

When signal bands are wide, as shown in Fig. 4(a), S/N degradation caused by 1/f noise does not become obvious and therefore, application thereof is available, however, in many cases, Low-IF architectures are widely applied in applications with narrow band such as GSM.

As shown in Fig. 4(b), since low-IF receiving circuits set IF frequency at sufficiently low values, channel filters can be set up in integrated circuits. Therefore, the structure of the circuit blocks become the same as direct conversion receiving circuits, which makes image removal at the digital signal processing part of the subsequent stages and frequency conversion from IF frequency to base bands realize at the same time. Since 1/f noise can be eliminated out-of-band in low-IF receiving circuits, robust receiving circuits against 1/f noise can be set up.

The biggest problem of applying low-IF receiving circuits is the influence of the image signals converted to the same IF frequency. Figure 5(a) shows the intensity of interfering wave of the neighboring channels defined by GSM standard. In the neighboring channel (+/− 200 kHz detuning), receipt of the signals by the maximum of 9 dB greater than the receiving signals is assumed and in the channel next to the neighboring channel (+/− 400 kHz detuning), receipt of greater signals by 41 dB is assumed. In this case, interfering wave greater by 41 dB would exist as an image signal in the same IF frequency as that of receiving signals when, for example, 200 kHz IF frequency is set as shown in Fig. 5(b).

In this case, at least 50 dB of image suppression is required. As earlier mentioned, in carrying out the image removal by digital signal processing, errors can be lessened by the process of the image removal itself. However, when there are some phase errors in I, Q RF mixers or when there are some gains or phase errors in two signal paths of I and Q, it means there are some errors in signals before image removal, which makes it difficult to secure image suppression in large amount. For securing the image suppression amount, many digital assist technologies have been proposed [5], [6], [28]. Figure 6 shows one of them [5]. As already mentioned, phase errors or amplitude errors in IQ signals are generated not only by errors in mixers but also by amplitude or phase relative errors of LPF in each IQ. In order to calibrate this, IQ linear transformation circuits with



(a) Direct conversion receiver.

(b) Low-IF receiver.

Fig. 4 Brock diagram and frequency plan of direct conversion and low-IF receivers.

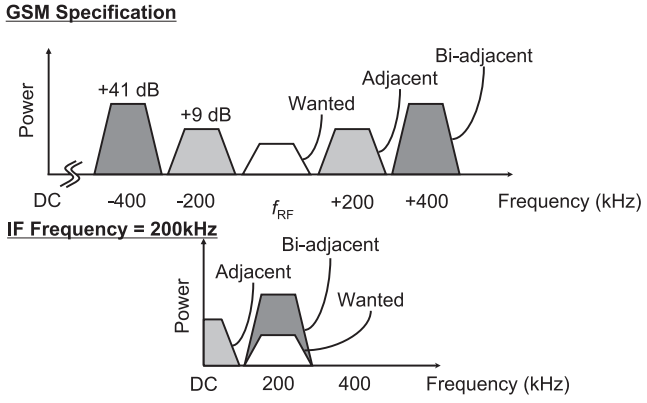


Fig. 5 A wanted signal and reference interferences.

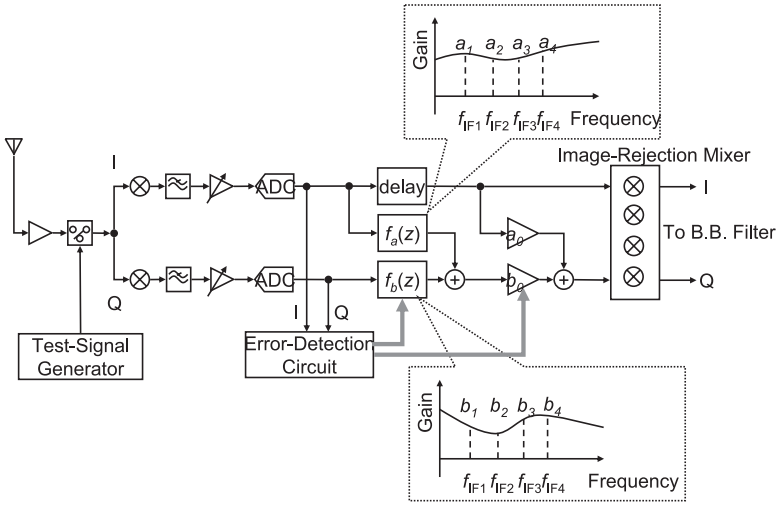


Fig. 6 Digital IQ calibration system.

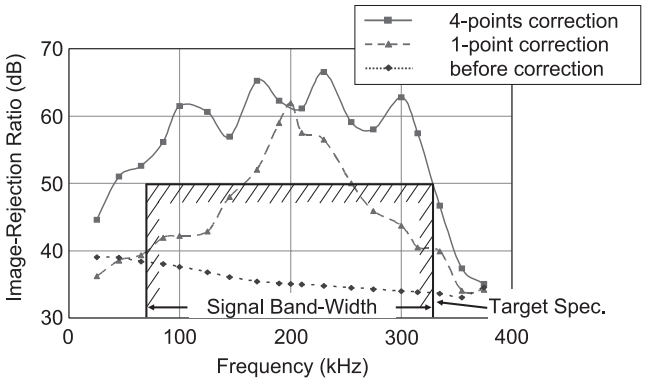


Fig. 7 Measured image-rejection ratios.

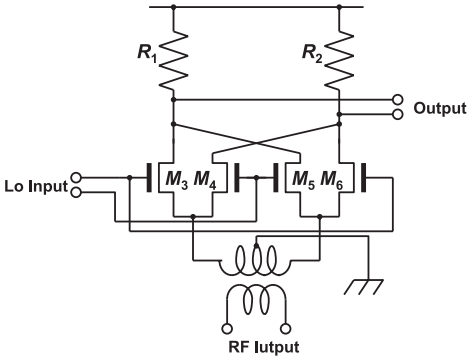


Fig. 8 Mixer with transformer input.

frequency characteristics are loaded on a digital signal processing part. This system is a so-called Off-line calibration mode that requires calibration exclusive period, detecting phase errors at four frequency points with TEST timing, calculating correction coefficient, thereby realizing calibration. Figure 7 shows one example of evaluation results. While the image suppression amount including the errors of mixers and IQ filters is 30 to 40 dB, not less than 50 dB image suppression amount is realized by calibration.

Low-voltage operation is also another important issue for integrating CMOS digital LSI. As a countermeasure for element circuits, a mixer shown in Fig. 8 can be exemplified. When supply voltage is lowered to the vicinity of 1 V, structure of double-stage circuits becomes difficult. Therefore, in the Gilbert-type mixers in Fig. 1, difference input stage composed of active transistors M1 and M2 was realized by transformer thereby making mixers with single-stage. The low voltage can be hereby coped with by composing the circuits with single DC connection utilizing inductance and transformer.

A sampling receiving circuit [29] shown in Fig. 9 is considered as a circuit mode in order to fundamentally cope with the low voltage operation. With lowering supply voltage, the structure of basic analog circuits such as OP amplifiers becomes difficult. Therefore, channel filters are prepared with analog discrete filters (FIR, IIR) made up of capacity and switches, thereby making the receiving circuits as

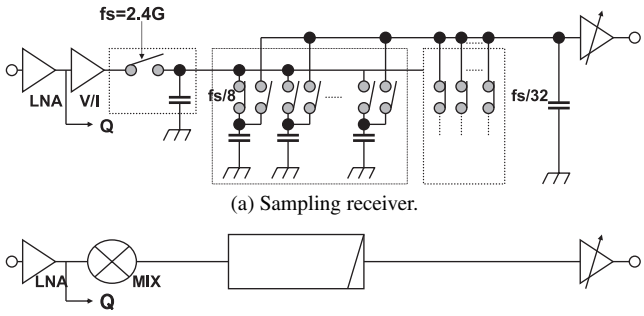


Fig. 9 Sampling receiver.

a whole by structure components that are easily composed with low voltage.

As heretofore mentioned, with interactions of element circuit technologies, digital signal processing technologies, and new receiving circuit technologies, countermeasures for the affect of 1/f noise that is the issue for CMOS receiving circuits and the realization of the low voltage operations is achieved.

4. Integration of Transmitting Circuits

As important technologies in discussing digitalization for CMOS of transmitting circuits, mixer circuit modes, VCO circuit modes, and synthesizer circuit modes can be exemplified. Since relating to mixer technologies overlaps with the technologies already introduced in the receiving circuits, in this chapter, mixer technologies is shortly mentioned first, followed by mentioning VCO circuits and synthesizers in more detail.

4.1 Mixer Circuit Technologies in Transmitting Circuits

As a representative example of transmitting circuits, direct conversion transmitting circuit shown in Fig. 10 can be exemplified. Regarding CMOS, it is exemplified that the problem to be solved in transmitting circuits is to reduce the generation of unwanted signal caused by interelement variabilities, while the problem to be solved in receiving circuits is to reduce 1/f noise. In direct conversion transmitting circuits, an orthogonal modulator using two mixers is operated by transmit frequency, and when DC off-set exists in mixers, carrier leakage is generated, and when there is phase difference in two local signals, image signals are generated [25]. By setting exclusive period for calibration and creating cos wave and sin wave as I, Q signals, carrier leakage and image signals corresponding to these errors are generated to output. When detected by a detector circuit, this shows that the carrier leakage ingredient is generated in the IQ signal frequency and the image signals are generated in twice as much frequency. By making AD conversion, monitoring signal intensity, adding DC off-set to IQ signals and by adjusting phases, both carrier leakage and image signal can be reduced [7], [30].

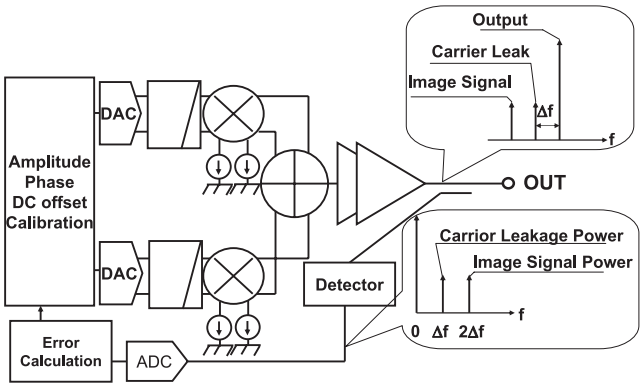
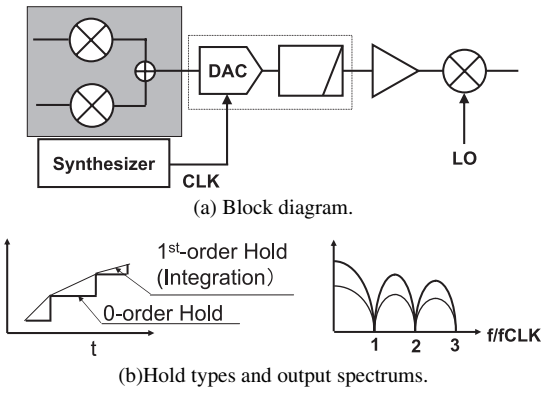


Fig. 10 Direct conversion transmitter with calibration.



(a) Block diagram.

(b)Hold types and output spectrums.

Fig. 12 Digital IF transmitter.

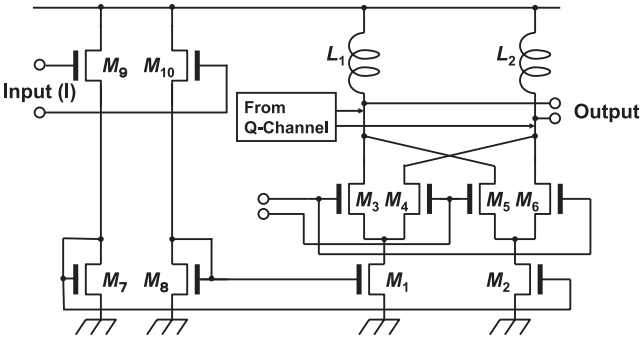


Fig. 11 CMOS Gilbert mixer for quad modulator.

In many cases of transmitting circuits, it is difficult to carry out the calibration by sending out signals and so, adjustment methods corresponding to systems are selected such as measuring DC off-set of mixers [31], adjusting DC off-set to be added to I, Q signals.

Regarding low voltage, since the signals of the input side of the mixer is I, Q signals and transformer cannot be used as in the case of the mixer for receiving circuit, the low voltage is coped with by making input with folded cascode connection as shown in Fig. 11. Although the composition is double-stage as ever, by enlarging M1 and M2, such countermeasures are intended as gaining margin and the like. Besides, in recent years, some examples [32] appear in which improved performance is intended by a clock construction carrying out low voltage operation by combining FET that performs switching operation as well as prohibiting overlap like receiving mixers and the Gilbert-type mixers that have long been applied are now under revision.

Facilitation of the system structure is also considered by digitizing the circuits that generate errors when composed of analog circuits such as orthogonal modulator and by eliminating the above mentioned calibration [33]. An example of digitalized orthogonal modulator is shown in Fig. 12(a). The digitized modulator is output as an IF signal from a DA modulator with a two-step transmitting circuit having IF frequency. In this case, the output spurious suppression of the DA modulator becomes the new challenge. As shown in Fig. 12(b), by defining the output of the DA modulator as differential signal of the output signal and by integrating the output with capacity, the output is converged from 0-order Hold to 1st-order Hold thereby suppressing the spurious. This mode requires SAW filter for suppressing the image because of the existence of the IF signal and is not applied for terminal-oriented SOC, however, it is employed in base stations. It is considered to be the technology field with increased significance depending on the development of RF elements.

4.2 Integration of VCO Circuits

In discussing CMOS and the digitalization of transceivers, the integration of VCOs as one of the main configuration circuits is extremely important. The most important VCO characteristics is C/N characteristics and the C/N affects the performance including interfering wave durability of the receiving circuits, EVM of the demodulating wave, noise characteristics of the transmitting circuits, EVM of the transmitting wave, and the like. Therefore, high C/N ratio is required for the VCOs used for cellular communicating systems. In order to realize this, improvement for Q of resonance circuits, improvement of S/N, and the like are essential.

The full-fledged review for the CMOS integration of VCOs for high performance was started in the mid 1990s as mentioned before [11], and at the onset, Q of the resonance circuit was improved by utilizing bonding wires. Concurrently, the review for highly performing spiral inductors on the integrated circuit was progressed.

Other than series parasitic resistance of a wiring layer, the analysis [10] on the influence such as loss by eddy current on Si substrate has been progressed and many suggestions have been made including configurations and the like. One key for realizing higher performance is to reduce the eddy current on the Si substrate and reduction by patterning [34] the diffuse layers has been reviewed. Presently, however, such methods seem to be widely employed that would physically keep the distance from the Si substrate using wiring layers with high layers. Further, although two load inductors were independently formed that connect to a negative resistance circuit of differential form in the initial

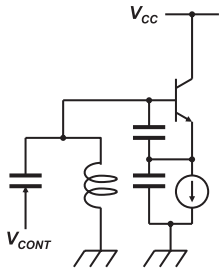


Fig. 13 Circuit diagram of conventional colpitts oscillator.

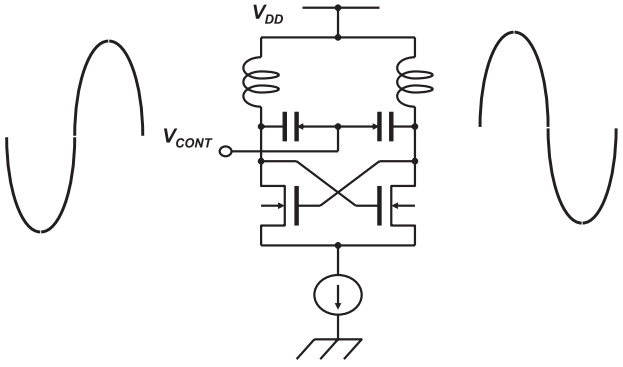


Fig. 14 Integrated differential oscillator.

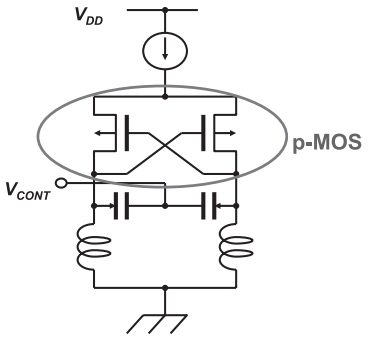


Fig. 15 Integrated differential oscillator with pMOS croses coupled pair.

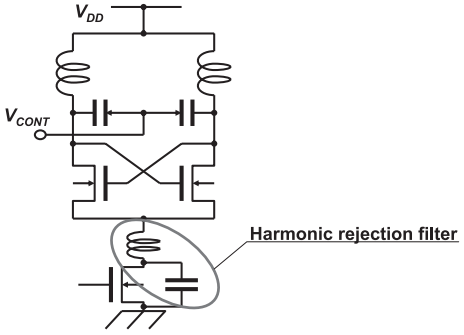


Fig. 16 Integrated differential oscillator with harmonic rejection filter.

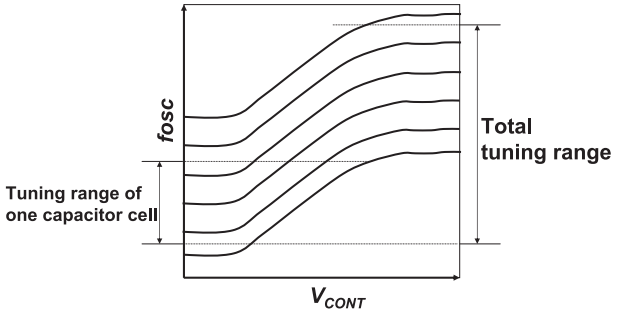


Fig. 17 Tuning range of integrated VCO.

stage of the study, in recent years, in many cases, load of a transforming mode that would utilize mutual inductance as well have been used.

As shown in Fig. 1(a), VCOs by CMOS, unlike the Colpitts oscillation circuit by a loan transistor as shown in Fig. 13 that was conventional so far, is composed by connecting a negative resistance circuit that cross-couple connects two nMOS transistors to a parallel resonance circuit by a varactor and an inductor as shown in Fig. 14. As an advantage for composing by FET, non-existence of saturation action that comes to be the problem when using bipolar transistor even though the drain amplitude is enlarged is exemplified. Therefore, signal amplitude can be sufficiently kept. Although the keystone for VCO design is to enlarge C/N ratio, together with differential operation, by enlarging "C" realizing the signal amplitude of not less than that of supplying voltage, the design allows Q of a resonator that is restricted on the integrated circuit.

The noise of FET was also reviewed and the method [35] of using pMOS with little 1/f noise shown in Fig. 15 and the method [36] of depressing the noise from the bias circuit shown in Fig. 16 have been suggested. The mechanism is that by suppressing double harmonic components of the vibration signals, the neighborhood noise of the double harmonic component is down-converted thereby preventing from being added to the carrier neighborhood noise. By these technologies, some prospects can be in sight for applying integrated VCOs to mobile phones requiring high C/N.

When applying the CMOS process, variable range of capacity values of MOS used as variable capacity is narrower compared with that of a unit varactor element that applies exclusive process. The problem further arises that the sufficient variable range cannot be secured due to further reduction in the variable range with the large signal amplitude and averaged MOS capacity value for achieving high C/N characteristics with low Q value.

In order to solve this problem, the mode of switch-overing the fixed bias MOS capacity and adding frequency offset has been suggested [37] as shown in Fig. 17. In addition, the mode of switch-overing the VCO alley [38], the mode of switch-overing the inductor [39], and the like have been suggested. Moreover, systematic reviewing on phase noise [40], [41] has been made and the integrated VCO is widely applied for cellular communication systems.

4.3 Synthesizer Based Transmitter Circuit

Talking now of the synthesizer system as a whole, integer

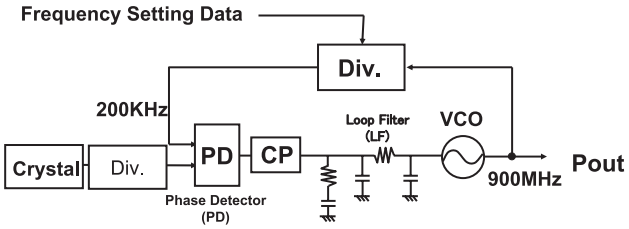


Fig. 18 Integer synthesizer.

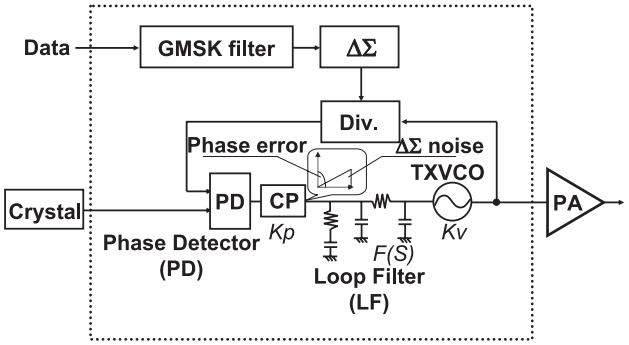


Fig. 19 Fractional synthesizer.

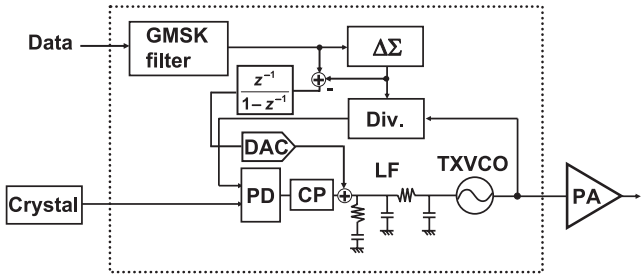


Fig. 20 ΔΣ transmitter with noise cancellation.

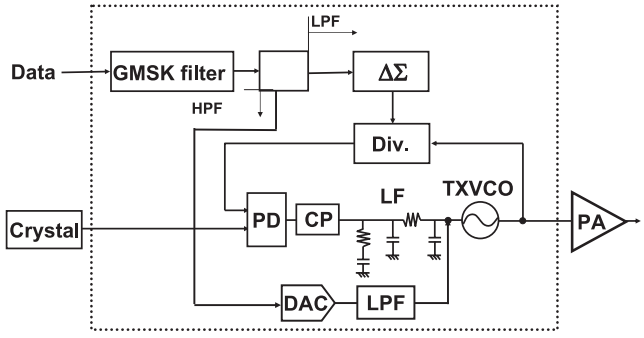


Fig. 21 2-point modulation type ΔΣ transmitter.

synthesizers as shown in Fig. 18 have been widely used in 1990s that applies phase comparison frequency that equals to channel interval of the application. However, in recent years, fractional-type synthesizers are more widely applied that can enhance the phase comparison frequency since it is ideal to enhance the phase comparison frequency to improve the phase noise performance. Talking of the fractional synthesizer itself, it starts from the mode [42] of thinning out the power output of the divider, followed by reviewing the modes [43]–[45] of switching-overing the dividing ratio of the divider by ΔΣ modulation, thereby arriving at the circuit form easily applied for cellular communication and applicable to the transmitting circuits as well as shown in Fig. 19.

When using ΔΣ modulation, near-carrier quantized noise is shifted to the region with distant frequency, and so, eliminating the noise by the design of the loop filters is required. Therefore, care should be taken since the sensitivity to the varied element values of the loop filter become high. Particularly, when the transmitting circuits modulating VCO are composed by adding the modulation information to frequency dividing ratio, widening of the loop band frequency is essential and the technology for eliminating the trade-off with the noise suppression is required. As a countermeasure, as shown in Fig. 20, the mode of cancelling the noise by actively adding the reverse phase signal of the noise generated by the ΔΣ modulation via DAC has been suggested [46]–[48]. By calculating the difference of the output between the original signals and ΔΣ modulator and by detecting the noise component, and by adding the reverse signal of the noise from DAC connected in parallel to the charge-pump output, the noise is reduced. By reducing the noise, the required accuracy of the frequency characteristics of the loop filter can be alleviated. Adding the circuit that adds the signal in action, however, lead to the noise degradation to some extent, and therefore, the detailed noise design is required. As another example, 2-point modulation method [49] can be exemplified as shown in Fig. 21. This utilizes the property of synthesizers showing the characteristics of Low pass filter to the signal change added to frequency dividing ratio, while showing the characteristics of High pass filter to the signal change added to VCO control voltage terminal. The modulated signal is added to ΔΣ modulator as well as adding the signal that directly controls VCO via DAC at the same time. The noise of the ΔΣ modulator is suppressed by the loop filter and the high pass component of the decaying modulated signal due to band limitation is compensated by the signal pass that directly modulates VCO. By the above mentioned operation, the influence that the modulated signal has caused by the limitation of loop filter bandwidth can be avoided. However, even with this mode, there lies a risk of noise deterioration since the added DAC adds the noise.

As a countermeasure of not adding circuits to the synthesizers, such a method that adds pre-enhancer circuits [23] (See Fig. 22) is suggested. This includes connecting the pre-emphasis circuits that cancels the LPF characteristics to the signal changes that the response of the synthesizer adds to the frequency dividing ratio before the ΔΣ modulator, thereby cancelling the effect of the band limitation of the loop filter. This method has no additional circuits in the synthesizer part and the noise deterioration can be kept to the lowest, however, it has the maximum risk of characteristic deviation caused by the variation of the element values of the loop characteristics.

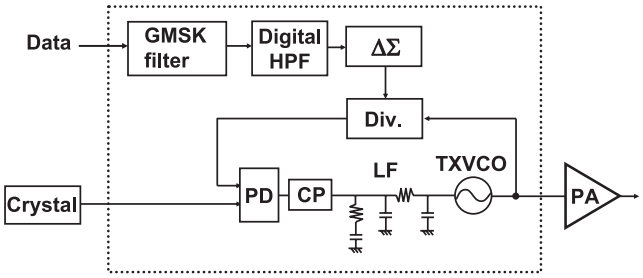


Fig. 22 Pre-enhancer type ΔΣ transmitter.

4.4 Digital Assist Loop Characteristics Calibration Technology

As a case study for a digital assist technology, such a system that comprises detecting the change of this loop characteristic is hereby introduced [50]. The outline of the calibration system is shown in Fig. 23. By utilizing the loaded ΔΣ modulator and by setting the divider to microscopic fluctuation, the so-called step signal of the frequency value is put in, and by observing the double integration of the step response of the synthesizer closed loop characteristics, the loop gain is detected. Based on this detected result, the loop gain is adjusted by changing the charge pump current, thereby enhancing the accuracy of the loop characteristics. In this method, for explaining the operation of this mode which requires to have some periods exclusive for calibration to observe the step response, first of all, the second-order PLL system is considered as shown in Fig. 24. Here, θ_{REF} represents phase comparator input signal phase, θ_{PLLOUT} represents VCO output phase, f_{out} represents output frequency of VCO, N represents frequency dividing ratio, θ_o represents feedback phase, $\Delta\theta_o$ represents error phase, K_p represents the phase error of the charge pump circuit-current coefficient, I_{CPO} represents charge pump output current, $F(S)$ represents loop filter transfer function, C_1 represents loop filter capacity, R_1 represents loop filter resistance, Vc represents VCO control voltage, and vI_{CPO} represents VCO voltage-frequency coefficient.

Usually and in many cases, the loop filter selects the third-order filter and applies the fifth-order PLL system, however, here, for analytical review, the loop filter is simplified to the first-order. Here, the overall open loop transfer function is represented by the following formula:

$$T_O(S) = \omega_n^2 \frac{\frac{2\xi}{\omega_n}S + 1}{S^2}, \quad \omega_n = \sqrt{\frac{K_p K_v}{NC_1}},$$

$$\xi = \frac{R_1}{2}\sqrt{\frac{K_p K_v C_1}{N}}$$

Here, ω_n represents oscillating coefficient and ξ represents attenuation coefficient. Here, the open loop gain is represented as follows.

$$\omega_n^2 = \frac{K_p K_v}{NC_1}$$

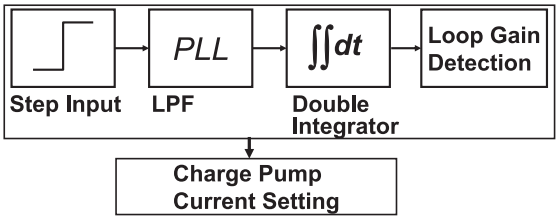


Fig. 23 Concept of calibration system.

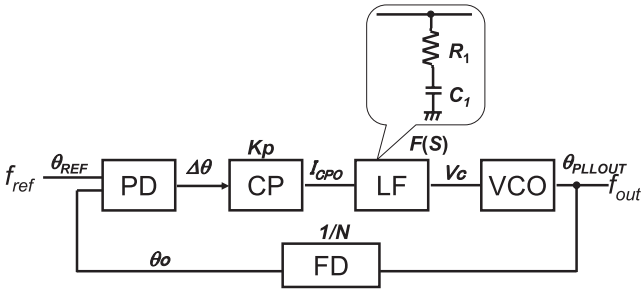


Fig. 24 Simplified 2nd -order PLL system.

Table 3 PLL transient response.

$\xi < 1$	$C(t) = 1 - e^{-\xi\omega_n t}\left\{\cos\omega_n\sqrt{1-\xi^2}\,t - \frac{\xi}{\sqrt{1-\xi^2}}\sin\omega_n\sqrt{1-\xi^2}\,t\right\}$
$\xi = 1$	$C(t) = 1 - e^{-\xi\omega_n t}\{1 - \omega_n t\}$
$\xi > 1$	$C(t) = 1 - e^{-\xi\omega_n t}\left\{\cosh\omega_n\sqrt{\xi^2-1}t - \frac{\xi}{\sqrt{\xi^2-1}}\sinh\omega_n\sqrt{\xi^2-1}t\right\}$

Despite any variability of K_p, K_v, N, and C_1, they are in dependent relation and they are the same in the sense of the change in open loop gain. Thus, for example, when K_p the charge pump circuit-current coefficient is adjusted, the variability of the open loop gain caused by the other parameters can be adjusted.

The step response of PLL can easily be gained analytically and the solution is shown in Table 3. As well known to many, the solution is divided into three cases, depending on the value of attenuation coefficient ξ. The result of double integration of these is shown in Table 4. Strictly speaking, providing step response to the targeted frequency switching the frequency-dividing number means to provide lump input to the phase, and the result of the integration of this phase response is shown in Table 4.

Assuming the system to be linear, this becomes identical to the result of double integration of the step response when frequency is set to be variable. As an example for these analytical formulae, $K_p = 50/2\pi$ (μA/rad), $K_v = 15$ (MHz/V), $C_1 = 100$ pF, $R_1 = 45$ kohm, $N = 35$, Open

Table 4 Double integration result.

$\xi < 1$	$\iint_0^{t_1} C(t)dt = \frac{t_1^2}{2} + \frac{1}{\omega_n^2} e^{-\xi\omega_n t_1} \cos\left(\sqrt{1-\xi^2}\,\omega_n t_1\right) + \frac{1}{\omega_n^2}\frac{\xi}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t_1} \sin\left(\sqrt{1-\xi^2}\,\omega_n t_1\right) - \frac{1}{\omega_n^2}$
$\xi = 1$	$\iint_0^{t_1} C(t)dt = \frac{t_1^2}{2} + \left\{\left(\frac{1}{\xi\omega_n}\right)^2\left(\frac{2}{\xi}-1\right) + \frac{t_1}{\xi^2\omega_n}\right\} e^{-\xi\omega_n t_1} - \left(\frac{1}{\xi\omega_n}\right)^2\left(\frac{2}{\xi}-1\right)$
$\xi > 1$	$\iint_0^{t_1} C(t)dt = \frac{t_1^2}{2} + \frac{1}{2\sqrt{\xi^2-1}\left(\xi-\sqrt{\xi^2-1}\right)\omega_n^2} e^{-\left(\xi-\sqrt{\xi^2-1}\right)\omega_n t_1} - \frac{1}{2\sqrt{\xi^2-1}\left(\xi+\sqrt{\xi^2-1}\right)\omega_n^2} e^{-\left(\xi+\sqrt{\xi^2-1}\right)\omega_n t_1} - \frac{1}{2\sqrt{\xi^2-1}\left(\xi-\sqrt{\xi^2-1}\right)\omega_n^2} + \frac{1}{2\sqrt{\xi^2-1}\left(\xi+\sqrt{\xi^2-1}\right)\omega_n^2}$

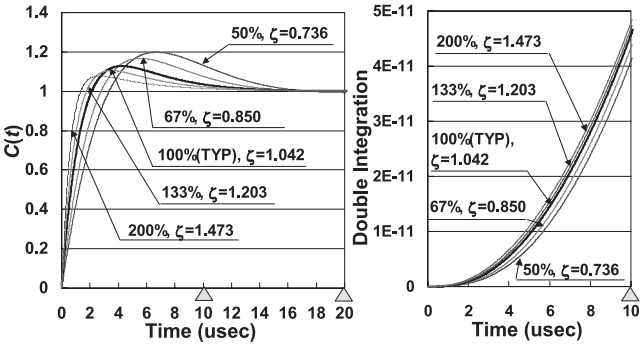
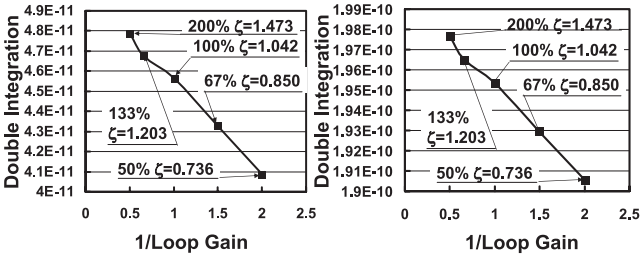


Fig. 25 Time domain waveform and double integrated result from analytical solution.



(a) $t_p = 10\,\mu$sec. (b) $t_p = 20\,\mu$sec.

Fig. 26 Relation between loop gain and double integration result at typical timing periods.

Loop Unity Gain Frequency = 157 kHz is shown and the step response and its double integration result calculating each response is shown in Fig. 25. As a variation example of loop characteristics, K_p was changed from 50% to 200% and the response difference was shown. The relationship of the reciprocal number of the loop gain normalized at the timing of 10 μsec and 20 μsec by this response and the result of the double integration is shown in Fig. 26. In either timing, the linear correlation was acknowledged and it is found that the result of the double integration is the parameter suitable for identifying the loop gain.

When applied to the ΔΣ synthesizer, to be specific, the result is as shown in Fig. 27.

By putting in the frequency step signal to the ΔΣ modulator and by accumulating the result of counted response by the indentifying counter, the double integration is realized. The operational process is shown in Fig. 28. First, by changing the frequency divisional ratio, the step signal of the frequency is generated. In this case, when the response of the synthesizer is observed by the output wave of the VCO, the response is corresponding to the loop gain. For example, when the loop gain is high, the response is quick, while when the loop gain is low, the response is slow. This process is counted with the counter and is accumulated. And since the VCO output that oscillates at 1 GHz and 2 GHz is directly used, even without the step response process, large counted result and large accumulated result are observed as off-set. In order to find off-set (ACC1), the period for counting and accumulating is provided before the step response and by subtracting the off-set value from the observed result of the step response (ACC2), the double integration result is obtained. In detecting with a counter, it is important to synchronize and as shown in Fig. 29, it is necessary to synchronize synchronous counter and accumulator and it is necessary for counter period, reference signal that is accumulation starting timing signal, and the reset signal of the accumulator to be synchronized with the VCO signal. Figure 30 shows the detected result of the loop gain in the ΔΣ transmitting circuit for GSM produced experimentally. The reciprocal of the normalized loop gain and the result of the double integration shows highly linear relationship and 2% accuracy is attained. Figure 31 shows the relationship of the charge pump current with the loop gain calibrated based on said detected result and the phase difference of the GMSK

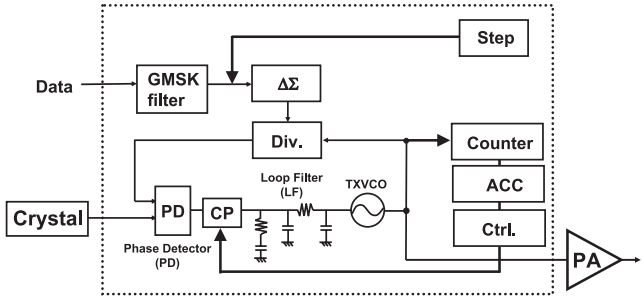


Fig. 27 Loop gain calibration system with double counter.

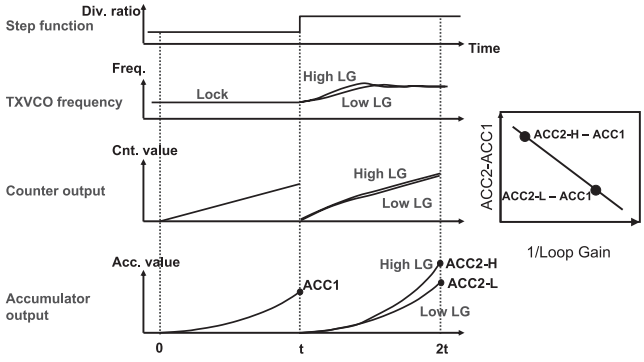


Fig. 28 Operation summary of double counting system.

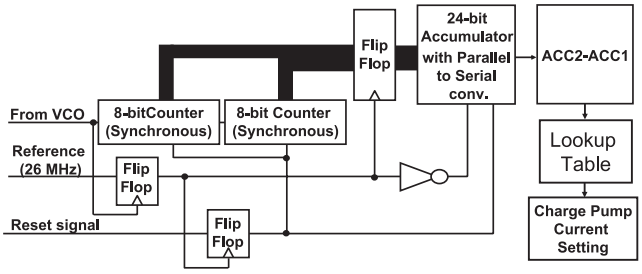


Fig. 29 Synchronization scheme of cal. system.

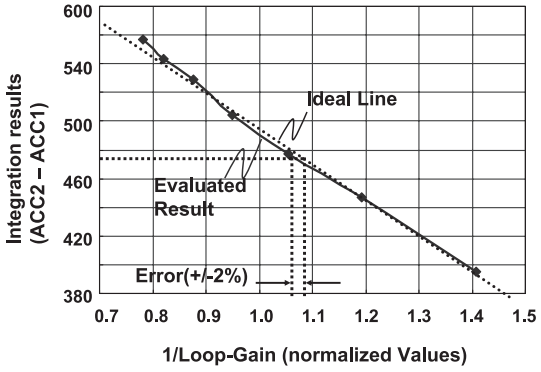


Fig. 30 Evaluated accumulator output.

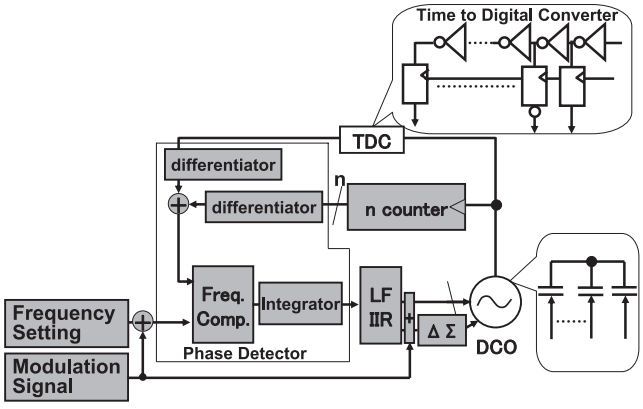


Fig. 31 All digital PLL transmitter.

modulation signal.

By calibration, the optimum charge pump current is selected thereby capable of optimizing the phase difference.

This method realizes the same detection by observing the difference signal of the phase comparator by ADC instead of using a counter [51]. Thus, by using digital signal processing, analog characteristics can be calibrated with high accuracy and therefore, robust system can be realized against variation of the element value.

4.5 ADPLL Circuit

As the refinement of CMOS advances, the supply voltage is lowered, and together with the restricted device characteristics, the variable range of the capacity is narrowed. To cope with this problem, the earlier mentioned capacity switchovering technology should be applied, and the ultimate one in which the frequency setting is realized by the switch-over of capacity alley is shown in Fig. 5, that is, DCO and all digital PLL (ADPLL) [52]. Naturally, to obtain the accuracy of frequency, static state obtained by the switch-over of the capacity value is not enough. In order to lock to the targeted frequency, it is essential to improve the accuracy by the oversampling technology such as $\Delta\Sigma$ modulation. The action of the DCO of switching the capacity can be considered as a DA converter with some kinds of oversampling functions. Thus, the image signal determined by the sampling frequency (the noise with the same frequency as that of aliasing at AD conversion), the noises by $\Delta\Sigma$ modulation, and the quantization noise are generated to DCO output. Since the oscillator takes the role of the integrator as well, these noises increase their suppression amount as they are distant from the oscillating frequency by the primary integrator. Thus, care must be taken in designing so as not to generate spurious that affects the applications such as clock frequency and the like. In the general synthesizers, regarding the output of the divider (counter), phase difference is detected by a reference clock and a phase comparator, followed by converting to the current pulse in proportion to the phase difference by a charge pump circuit, smoothing with a loop filter, thereby generating the control voltage of the VCO. Although the divider itself is a digital circuit, what is transmitted is the timing of the rising edge and the trailing edge of the divider output and the analog value. In order to control the DCO, the loop filter output should be a digital code and it is required to digitize a series of functions of divider-phase comparator-charge pump-loop filter. The function of the divider is replaced by the counter and TDC (Time to Digital Converter). Unlike the analog divider, the output of the counter is not the changes in the top of the n-bit counter but the counted values in all bits are output. TDC is composed of a delay circuit by inverter sequence and it is the circuit of detecting the number of actions that the inverter makes starting from a timing within a predetermined period, detecting the phase difference with higher accuracy than that of the counter, and to be specific, it detects the information of the action not greater than 1 cycle by VCO. Since it is difficult to set the phase when using the phase comparator, the output is differentiated and is replaced by the frequency information, followed by detecting the difference from the value showing the targeted frequency, integrating the detected result to re-create the phase information, inputting the phase information to the loop filter, thereby generating the numerical values that determine the state of DCO. Thus, it is found that basically, it has the same action principle as that of the analog synthesizer. ADPLL does not require analog charge pumps that are hard to be used at a low voltage action in accordance with the refinement and there is no concern for varied elements of the loop filter nor is there any varied K_v characteristics of VCO, thereby solving many problems that analog synthesizer used to have. However, cares must be taken for highly-accurate

analog characteristics since TDC requires the one [3].

5. Conclusion

The trend of CMOS and of the digitalized technologies of the transmitting circuits and the receiving circuits was heretofore reviewed taking the synthesizer based transmitter as one example. With the process refinement, while enhancement of the calibration function can be realized by employing digital signal process and control, due to the lowered supply voltage and the like, the challenge level of the remaining analog part tends to increase. Therefore, both the utilization of the digital function and the development of challenging analog circuit are and will be important.

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References

[1] R.B. Staszewski, J.L. Wallberg, S. Rezeq, C.-M. Hung, O.E. Eliezer, S.K. Vemulapalli, C. Fernando, K. Maggio, R. Stazewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phone," IEEE J. Solid-State Circuits, vol.40, no.12, pp.2469–2482, May 2005.

[2] P.H. Bonnaud, M. Hammes, A. Hanke, J. Kissing, R. Koch, E. Labarre, and C. Schwoerer, "A fully integrated SoC for GSM/GPRS in 0.13 μm CMOS," IEEE, ISSCC2006, Dig. Tech. Paper, pp.482–483, Feb. 2006.

[3] R.B. Staszewski, D. Leipold, O. Eliezer, M. Entezari, K. Muhammad, I. Bashir, C.M. Hung, J.J. Wallberg, R. Staszewski, P. Cruise, S. Rezeq, S. Vemulapalli, K. Waheed, N. Barton, M.-C. Lee, C. Fernando, K. Maggio, T. Jung, I. Elahi, S. Larson, T. Murphy, G. Feygin, I. Deng, T. Mayhugh, Y.-C. Ho, K.-M. Low, C. Lin, J. Jaehnig, J. Kerr, J. Mehta, S. Glock, T. Almholt, and S. Bhatara, "A 24 mm^2 quad-band single-chip GSM radio with transmitter calibration in 90 nm digital CMOS," IEEE ISSCC2008, Dig. Tech. Paper, pp.208–209, Feb. 2008.

[4] T. Sowlati, B. Agarwal, J. Cho, T. Obkircher, M.E. Said, J. Vasa, B. Ramachandran, M. Kahrizi, E. Dagher, W.H. Chen, M. Vadkerti, G. Taskov, U. Seckin, H. Firouzkouhi, B. Saeidi, H. Akyol, Y. Choi, A. Mahjoob, S. D'Souza, C.-Y. Hsieh, D. Guss, D. Shum, D. Badillo, I. Ron, D. Ching, F. Shi, Y. He, J. Komaili, A. Loke, R. Pullela, E. Pehivanoglu, H. Zarei, S. Tadipour, D. Agahi, D. Rozenblit, W. Comino, G. Williams, N. Damavandi, S. Wloczysiak, S. Rajendra, A. Paft, and T. Valencia, "Single-chip multiband WCDMA/HSDPA/HSUPA/EGPRS transceiver with diversity receiver and 3 G digRF interface without SAW filters in transmitter/3 G receiver paths," IEEE ISSCC2009, Dig. Tech. Paper, pp.116–117, Feb. 2009.

[5] K. Maeda, W. Hioe, Y. Kimura, and S. Tanaka, "Wideband image-rejection circuit for low-IF receivers," IEEE ISSCC2006 Dig. Tech. Paper, pp.476–477, Feb. 2006.

[6] K. Maeda, T. Yamawaki, Y. Kimura, and S. Tanaka, "Mixed analog digital IQ calibration techniques," IEICE Technical Report, 2008 Microwave Workshop Digest, WS13-3, pp.325–330, Nov. 2008.

[7] S. Tanaka, "Circuit techniques for mobile communication transceivers," IEICE Trans. Electron. (Japanese Edition), vol.J89-C, no.10, pp.622–640, Oct. 2006.

[8] S. Tanaka, "Technical trend of mixed analog and digital RF circuits," IEICE Technical Report, 2008 Microwave Workshop Digest, WS13-1, pp.315–320, Nov. 2008.

[9] J. Sevenhans, "An integrated Si bipolar RF transceiver for a zero IF 900 MHz GSM digital mobile radio frontend of a hand portable phone," IEEE Proc. CICC1991, pp.7.7.1–7.7.4, May 1991.

[10] J. Lee, A. Kral, A.A. Abidi, and N.G. Alexopoulos, "Design of spiral inductors on silicon substrates with a fast simulator," Proc. 1998 ESSCIRC, pp.328–331, Sept. 1998.

[11] J. Craninckx and M. Steyaert, "A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler," IEEE J. Solid-State Circuits, vol.30, no.12, pp.1474–1482, Dec. 1995.

[12] K. Takikawa, T. Yamawaki, S. Tanaka, M. Kokubo, T. Wakuda, K. Irie, K. Hori, Y. Okabe, T. Hashimoto, M. Kasahara, and B. Henshaw, "RF circuits technique of dual-band transceiver IC for GSM and DCS1800 applications," Proc. 25th ESSCIRC, pp.278–281, Sept. 1999.

[13] T. Yamawaki, M. Kokubo, K. Irie, H. Matsui, K. Hori, T. Endou, H. Hagisawa, T. Furuya, Y. Shimizu, M. Katagishi, and J.R. Hildersley, "A 2.7 V GSM RF transceiver IC," IEEE J. Solid-State Circuits, vol.32, no.12, pp.2089–2096, Dec. 1997.

[14] S. Tanaka, "A PLL based transmitter architecture for GSM system," MWE2000 Digest, pp.361–365, Dec. 2000.

[15] S. Atkinson and A. Kontos, "Fractional frequency multiplier for use in GSM direct conversion receivers," IEICE Technical Report, 2001 Microwave Workshop Digest, pp.253–257, Dec. 2001.

[16] S. Tanaka, T. Yamawaki, K. Takikawa, N. Hayashi, I. Ohno, T. Wakuta, and B. Henshaw, "GSM/DCS1800 dual band direct-conversion transceiver IC with a DC offset calibration system," Proc. 27th ESSCIRC, pp.492–495, Sept. 2001.

[17] S. Tanaka, T. Yamawaki, N. Hayashi, M. Kasahara, and B. Henshaw, "Circuit techniques for GSM/DCS1800 direct conversion receiver," IEICE Technical Report, 2001 Microwave Workshop Digest, pp.269–274, Dec. 2001.

[18] A.A. Abidi, "RF CMOS come of age," IEEE Microw. Mag., vol.4, no.4, pp.47–60, Dec. 2003.

[19] T. Sowlati, D. Rozenblit, R. Pullela, M. Damgaard, E. McCarthy, K. Dongsoo, D. Ripley, F. Balteanu, and I. Gheorghe, "Quad-band GSM/GPRS/EDGE polar-loop transmitter," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2179–2189, Dec. 2004.

[20] Y. Akamine, S. Tanaka, M. Kawabe, T. Okazaki, Y. Shima, M. Yamamoto, R. Takano, and Y. Kimura, "A polar loop transmitter with digital interface including a loop-bandwidth calibration system," IEEE ISSCC2007 Dig. Tech. Paper, pp.348–349, Feb. 2007.

[21] T. Yamawaki, Y. Akamine, T. Norimatsu, and Y. Kimura, "Polar-transmitter technique for GSM/EDGE mobile-phone applications," IEICE Technical Report, 2007 Microwave Workshop Digest, WS10-2, pp.289–294, Nov. 2007.

[22] R. Pullela, S. Tadjpour, D. Rozenblit, W. Domino, T. Obkircher, M.E. Said, B. Ramachandran, T. Sowlati, D. Agahi, W. Chen, D.A. Badillo, M. Kahrizi, J. Komaili, S. Wloczysiak, U. Seckin, Y.-Y. Choi, H. Akyol, M. Vadkerti, A. Mahjoob, H. Firouzkouhi, D. Shum, R. Suhanthan, N. Vakilian, T. Valencia, C. Dantec, A. Paff, and M. Ahooie, "An integrated closed-loop polar trasmitter with saturation prevention and low-IF receiver for quad-band GPRS/EDGE," IEEE ISSCC2009, Dig. Tech. Paper, pp.112–113, Feb. 2009.

[23] E. Gotz, H. Krobel, G. Marzinger, B. Memmler, C. Munker, B. Neurauter, D. Romer, J. Rubach, W. Schelmbauer, M. Scholz, M. Simon, U. Steinacker, and C. Stoger, "A quad-band low power single chip direct conversion CMOS transceiverwith DS- modulation loop for GSM," ESSCIRC 2003 Dig., pp.217–220, Sept. 2003.

[24] H. Majima and M. Hamada, "A 90 nm CMOS CT BPF for Bluetooth transceivers with DT 1b-switched-resistor cut-off frequency control," IEEE ISSCC2009, Dig. Tech. Paper, pp.334–335, Feb. 2009.

[25] S. Tanaka, "Circuit technique for integrated mixer," IEICE Technical Report, 2001 Microwave Workshop Digest, pp.413–422, Dec. 2001.

[26] V. Krizhanovskii, N.T. Kien, and J.-C. Choi, "A direct conversion CMOS front-end for 2.4 GHz band of IEEE 802.15.4 standard," IEEE ASSCC2005, pp.449–452, Oct. 2005.
[27] M. Camus, B. Butaye, L. Garcia, M. Sie, B. Pellat, and T. Parra, "A 5.4 mW/0.07 mm^2 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4 WPAN standard, "IEEE J. Solid-State Circuits, vol.43, no.6, pp.1372–1383, June 2008.
[28] I. Elahi and K. Muhammad, "I/Q mismatch compensation using adaptive decorrelation in a low-IF receiver in 90-nm CMOS process," IEEE J. Solid State Circuits, vol.41, no.2, pp.395–404, Feb. 2006.
[29] K. Muhammad, D. Leipold, B. Staszewski, Y.-C. Ho, C.M. Hung, K. Maggio, C. Fernando, T. Jung, J. Wallberg, J.-S. Koh, S. John, I. Deng, O. Moreira, R. Staszewski, R. Katz, and O. Friedman, "A discrete-time Bluetooth receiver in a 0.13 μm digital CMOS process," IEEE ISSCC2004 Dig., pp.322–323, Feb. 2004.
[30] C.P. Lee, A. Behzad, D. Ojo, M. Kappes, S. Au, M.-A. Pan, K. Carter, and S. Tian, "A highly linear direct-conversion transmit mixer transcondactance stage with local oscillation feedthrough and I/Q imbalance cancellation scheme," IEEE ISSCC2006 Dig. Tech. Paper, pp.368–369, Feb. 2006.
[31] D. Miyashita, H. Ishikuro, T. Shimada, T. Tanzawa, S. Kuusai, H. Kobayashi, H. Majima, K. Agawa, M. Hamada, and F. Hatori, "A low-IF CMOS single-chip Bluetooth EDR transmitter with digital I/Q mismatch trimming circuit," IEEE 2005 VLSI Symposium on VLSI Circuit Dig., pp.298–301, June 2005.
[32] X. He and J. Sinderen, "A 45 nm low-power SAW-less WCDMA transmit modulator using direct quadrature voltage modulation," IEEE ISSCC2008 Dig. Tech. Paper, pp.120–121, Feb. 2009.
[33] V.W Leung, E.L. Larson, and S.P. Gudem, "Digital-IF WCDMA handset transmitter IC in 0.25 μm SiGe BiCMOS," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2215–2225, Dec. 2004.
[34] C.P. Yue and S.S. Wong, "On-chip spiral inductors with patterned ground shields for si-based RF IC," IEEE Dig. of 1997 VLSI Circuit Symposium, pp.85–86, June 1997.
[35] C.-M. Hung and K.K. O, "A 1.24-GHz monolithic CMOS VCO with phase noise of −137 dBc/Hz at a 3-MHz offset," IEEE Microw. Guid. Wave Lett., vol.9, no.3, pp.111–113, March 1999.
[36] E. Hegazi, H. Sjoland, and A.A. Abidi, "A filtering technique to lower LC oscillator phase noise," IEEE J. Solid-State Circuits, vol.36, no.12, pp.1921–1930, Dec. 2001.
[37] A. Yamaguchi, T. Tsukahara, M. Harada, and J. Kodate, "A low-voltage 6-GHz-band CMOS monolithic LC-tank VCO using a tuning-range switching technique," IEEE 2001 IMS, pp.735–738, June 2001.
[38] A. Kral, F. Behbahani, and A.A. Abidi, "RF-CMOS oscillators with switching tuning," IEEE 1998 CICC, pp.555–558, 1998.
[39] S.-M. Yim and K.K. O, "Demonstration of switched resonator concept in a dual-band monolithic CMOS LC-tuned VCO," IEEE 2001 CICC, pp.205–208, Oct. 2001.
[40] A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillators," IEEE J. Solide-State Circuits, vol.33, no.2, pp.179–194, Feb. 1998.
[41] A. Hajimiri and T.H. Lee, "Design issues in CMOS differential LC oscillators," IEEE J. Solide-State Circuits, vol.34, no.5, pp.717–724, May 1999.
[42] J. Gibbs and R. Temple, "Frequency domain yield its data to phase-locked synthesizer," Electronics, pp.107–113, April 1978.
[43] B. Miller and R.J. Conley, "A multiple modulator fractional devider," IEEE Trans. Instrum. Meas., vol.40, no.3, pp.578–583, June 1991.
[44] T.A.D. Riley, M.A. Copeland, and T.A. Kwasniewsky, "Sigma-delta modulation in fractional-N frequency synthesis," IEEE J. Solid-State Circuits, vol.28, no.5, pp.553–559, May 1993.
[45] W.T. Bax, T.A.D. Riley, C. Plett, and M.A. Copeland, "A D-S frequency discriminator based synthesizer," IEEE 1995 ISCAS, June 1995.
[46] S. Pamarti and I. Galton, "Phase-noise cancellation design tradeoffs in delta-sigma fractional-N PLLs," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol.50, no.11, pp.829–838, Nov. 2003.
[47] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation," IEEE J. Solid-State Circuits, vol.39, no.1, pp.49–62, Jan. 2004.
[48] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700 kHz bandwidth SD fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," IEEE J. Solid-State Circuits, vol.39, no.9, pp.1446–1454, Sept. 2004.
[49] B. Neurauter, G. Marzinger, A. Schwarz, and R. Vuketich, "GSM900/DCS1800 fractional-N modulator with two-point-modulation," IEEE MTT-S IMS Dig., pp.425–428, June 2002.
[50] Y. Akamine, M. Kawabe, K. Hori, T. Okazaki, M. Kasahara, and S. Tanaka, "DS PLL transmitter with a loop-bandwidth calibration system," IEEE J. Solid-State Circuits, vol.43, no.2, pp.497–506, Feb. 2008.
[51] H. Shanan, G. Retz, K. Mulvaney, and P. Quinlan, "A 2.4 GHz 2 Mb/s versatile PLL-based transmitter using digital pre-emphasis and auto calibration in 0.18 μm CMOS for WPAN," IEEE ISSCC2009 Dig., pp.420–421, Feb. 2009.
[52] R.B. Staszewski, J.L. Wallberg, S. Rezeq, C.-M. Hung, O.E. Eliezer, S.K. Vemulapalli, C. Fernando, K. Maggio, R. Stazewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phone," IEEE J. Solid-State Circuits, vol.40, no.12, pp.2469–2482, May 2005.
[53] B. Wilkins, "Polaris total radioTM, a highly integrated RF solution for GSM/GPRS and EDGE," IEEE RFIC Symp. Dig., pp.383–386, June 2003.

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