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# A Single Element Phase Change Memory

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**SUMMARY** We report a fast single element nonvolatile memory that employs amorphous to crystalline phase change. Temperature change is induced within a single electronic element in confined geometry transistors to cause the phase change. This novel phase change memory (PCM) operates without the need for charge transport through insulator films for charge storage in a floating gate. GeSbTe (GST) was employed to the phase change material undergoing transition below 200°C. The phase change, causing conductivity and permittivity change of the film, results in the threshold voltage shift observed in transistors and capacitors.

***key words:*** *memory, phase change memory, PCM, nonvolatile, GST*

## 1. Introduction

For nanoscale nonvolatile memories, the commercial efforts have followed two paths in the last decade. Charge injection and trapping is the primary commercial approach in use for achieving a memory state while phase change in a series resistance connection has been a major area of research and development for the future. The first approach — charge trapping/detrapping within an insulator stack — is integrated into a field effect transistor [1] leading to compact designs such as the NAND architecture. In ultra-small devices, the injection phenomena and the energetic interactions affect the reliability, endurance, and operating characteristics. Stochastic and small-scale effects continue to become increasingly dominant. The second approach uses conductivity change arising from phase change between amorphous and crystalline phases [2]. This structure employs an access element (a diode, fet, or a bipolar transistor) in series. The first approach leads to a single element device, but encounters degradation of dielectric due to carriers' energy being lost in creating increased number of defects during use. The second approach employs phase change created thermally and requires current flow and power dissipation. The amorphization and crystallization processes typically happen or are initiated in the vicinity of a metal electrode. This approach encounters problems related to power, timing, scaling issues due to surface effects, and the need of area for two elements. Our device is a new form of memory based on phase change in a single element. The new approach takes advantage of the fact that information can be stored by changing other characteristics of the material — such as those of permittivity or conductivity without resorting to charge storage. An interest in a universal memory having DRAM and Flash's merits has driven the invention of many structures of novel memory devices and various combinations/mixtures of materials [3]. This phase change memory may be capable of serving this area.

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## 2. Novel Memory Structure

Figure 1 shows the structure of PCM with the features of DRAM and conventional FLASH memories.

A phase change material is placed in the transistor structure similar to the floating gate of Flash memories. The phase change in the material takes place through heating of the device as a result of current flow. The dissipated thermal energy is employed to write the data, and erase the data with use of temperature-time profiles that come about from the passage of current with applied waveforms of bias voltages. If the transferred thermal energy is high enough to switch the phase of phase change material, the transistor proper-

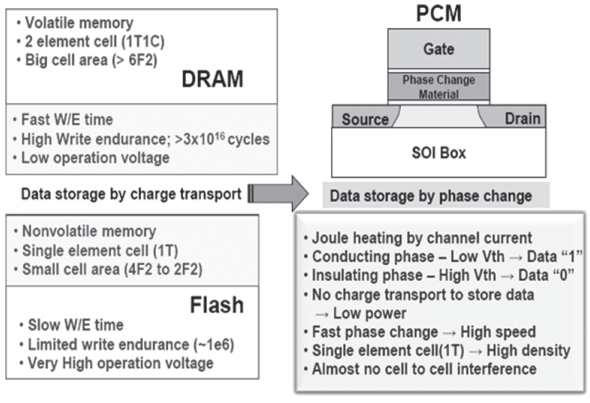


**Fig. 1** Features of DRAM and Flash memories and the schematic of phase change memory device.

**Table 1** Various phase change materials with critical temperatures and transition factors.

| | T1 | T2 (ΔT) | ρ1 | ρ2 (Ratio) | ε | Eg | Transition Factors |
|---|---|---|---|---|---|---|---|
| | [°C] | | [Ω°cm] | | | [eV] | |
| GST | - | 150 @ACT 270 @CCT | 25 | 0.025 (1000) | 16.5 @Amorph 32 ~ 40 @FCC 38 @HCP | 0.7 → 0.5 | Heat |
| Doped IGT | - | 280 ~ 300 | 1000 ~ 1e4 | 1 (Nor.) | | | Heat |
| TMO (NiO) | - | > 300 | 100 ~ 1000 | 1 (Nor.) | | | E-field Heat |
| CrO2 | - | -60 | | | | | Heat H-field |
| Nb2O5 | 350 | 530 | | | | | Heat H-field |

ties can be changed due to the variation of equivalent oxide thickness (EOT). Here, PC material plays a role as a memory node by changing of the dielectric constant and conductivity induced by phase change. Table 1 shows several phase change materials showing critical temperatures and transition factors. GST is the most prevalent material used: in PRAMs, CDs and DVDs. Its phase can be reversibly switched from the amorphous to the poly-crystalline by Joule heating. GST has two crystalline phases. One is the metastable FCC phase, the other is the stable HCP phase [4], [5]. So, phase change happens twice. At around 150°C, the phase changes from amorphous to FCC crystalline, and at around 270°C, it changes from FCC to HCP crystalline.

## 3. Model & Simulation Results

Figure 2 shows the simple model for PCM. For this model, we assume that there is no oxide charge, and $V_{fb}$, $\Psi_s$ and $Q_s$ are the same in both phases. That is, only the dielectric constant and conductivity of the PC material is assumed to be different between two phases and that in the metallic state, the conductivity and permittivity are infinite. From this assumption, we can get the threshold voltage difference between two phases.

$$\Delta V_{th} = |Q_S| \times t_{ox} \times \varepsilon_{ox} \times \left(\frac{\alpha}{\gamma}\right) \tag{1}$$

According to Eq. (1), $\Delta V_{th}$ is determined by the thickness and dielectric constant of a PC material. In detail, $\Delta V_{th}$ is proportional to the thickness and reversely proportional to the dielectric constant in the insulating phase. Phase change time ($t_{tr}$) is a very critical factor on data writing process. So, to estimate how fast the phase change happens, we estimate it using the following equation.

$$\alpha I_{dsat}^2 R_{ch} t_{tr} = m_{ox} C_{ox} \Delta T + L_{GST} V_{GST} \tag{2}$$

Left term is a formula of joule heating energy generated by channel current and the first term on the right represents the oxide-heating energy and the second is latent heat of GST. The heat efficiency $\alpha$ was derived from the ratio of

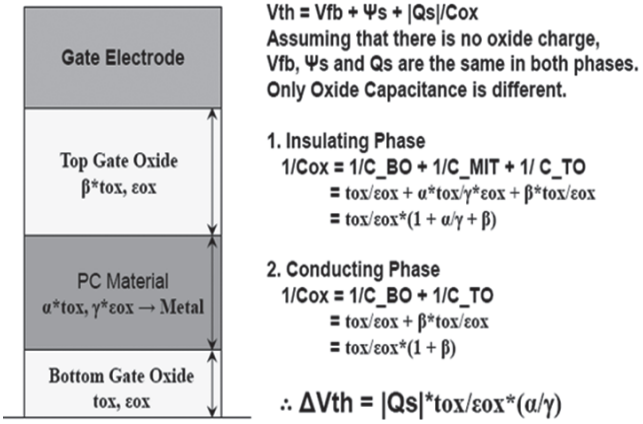


**Fig. 2** A model for phase change memory.

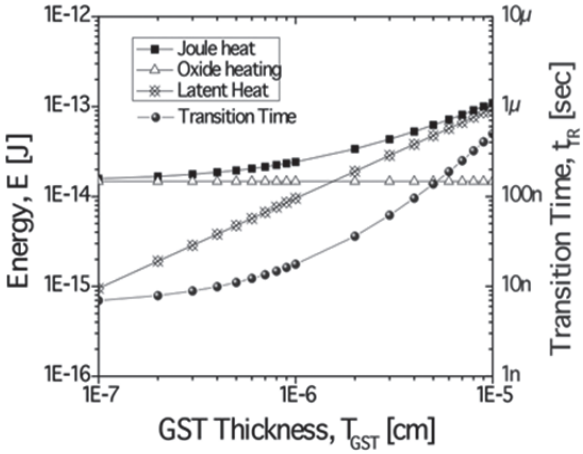


**Fig. 3** Trend of energy & transition time with varying thickness of GST.

heat conduction as follows.

$$\alpha = H_{\text{up}}/(H_{\text{up}} + H_{\text{down}}) = R_{\text{down}}/(R_{\text{up}} + R_{\text{down}}) \tag{3}$$

Here, $H_{\text{up}}$ and $H_{\text{down}}$ are heat conductions delivered from the channel upwardly and downwardly, respectively. $R_{\text{up}}$ and $R_{\text{down}}$ are heat resistances of corresponding heat conductions. The heat efficiency is around a few percent for a device with bulk Si substrate and around ~50 percent for a bridge type structure having air dielectric beneath of Si channel. As shown in Fig. 3, a transition time to reach phase change temperature (130°C) has been calculated in nanoscale devices. It has 100 nm/100 nm of gate width and length with 5 nm of bottom gate oxide thickness, 10 nm of GST thickness and 10 nm of top gate oxide layer.

When 3 V is applied to $V_{GS}$ and $V_{DS}$, the transition time is around 18 ns, which is comparable to the writing time of a DRAM cell. For the large memory window, two factors, the thickness and dielectric constant of a PC material, should be increased, which can deteriorate the speed of phase change. The optimization of these factors might be a challenge for memory applications.

## 4. Results and Discussion

GeSbTe (GST) films with the thicknesses of 100 nm were deposited by RF sputtering. Figure 4 shows the resistance change of GST after external heating and cooling. First, we measured the resistance change in hall bar test pattern which doesn't have transistor process, meaning that the GST film keeps initial status as it was sputtered. The initial resistance is about 500 kΩ, which is close to the value of GST in the amorphous phase [6]. In contrast, when all transistor-making processes are adapted, the initial resistance is around 7 kΩ, which is close to the value of GST in the metastable fcc crystalline phase. So, the fabrication processes can make an effect on the initial phase of GST. To prevent GST from changing its phase from amorphous to FCC crystalline during fabrication processes, it is necessary to control all the processes under 150°C of the phase change temperature. After $H_2$ anneal at 350°C in flowing 5% $H_2$ for 1 hr, the resistance decreased to about 300 Ω being close to the value of GST in the HCP crystalline phase. Once the phase of GST became HCP crystalline, thermal hysteresis behavior disappeared and GST acted like a metal. In this phase, when the temperature increased, the resistance also increased due to the increase of phonon scattering.

As shown in Fig. 5, after $H_2$ anneal, the threshold voltage decreased and gate capacitance increased by 0.5 V and 8 pF, respectively. As we expected, phase change effects on the change of GST dielectric constant. Additionally, we investigated the possibility of gate field induced phase change using modified hall bar test patterns. If we control the phase of a PC material by the gate field, we can enlarge the memory window. Figure 6 shows the resistance variation according to the gate field. The main reason for this little change is that the heat generated in the channel can dissipate through the substrate more easily than be delivered to a PC material through the gate oxide because the thermal conductivity of silicon is about 150 times higher than that of silicon dioxide.

Therefore the temperature of the channel and the heat delivery efficiency must be lower than expected. The heating efficiency can be improved by use of Silicon-on-insulator (SOI), wire and other forms where heat transport through the substrate is suppressed. In the amorphous phase, the resistance variation is larger than that of the FCC crystalline. This is the very first discovery implying that the gate field can affect the phase change mechanism of GST.

## 5. Conclusion

We have demonstrated a new single element memory device using phase change. It does not need charge transport to its memory node for data storage. Additionally, its phase change time is estimated to be fast — in the range necessary for universal memories. The cell consists of only one transistor making it a highly dense memory. In this novel form of memory using GST phase change material, the threshold voltage has been changed with the variance

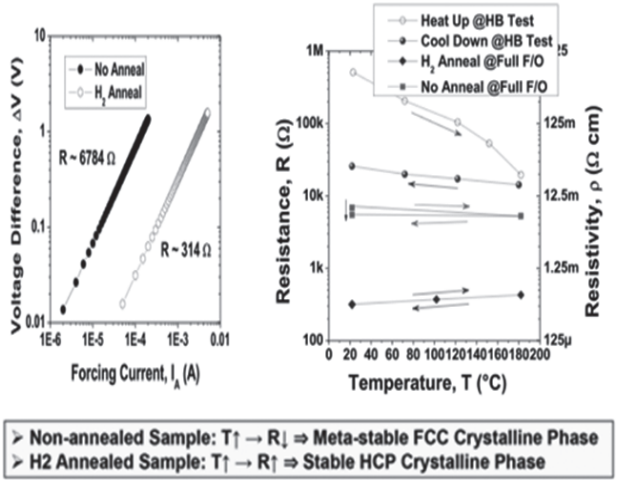


**Fig. 4** The comparison of GST resistance.

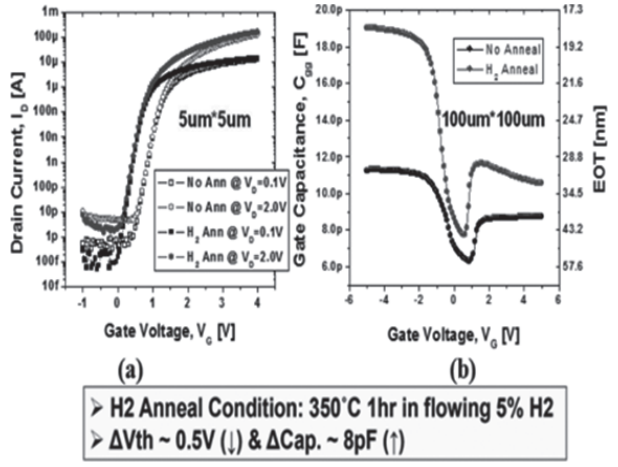


**Fig. 5** Threshold voltage shift/capacitance change in PCM.

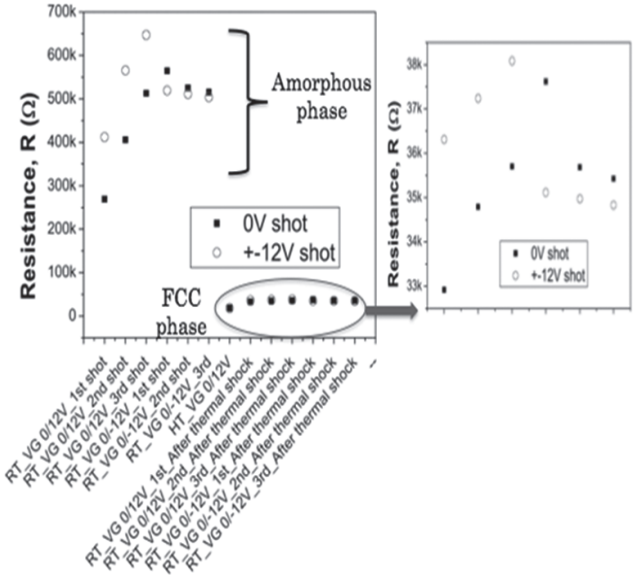


**Fig. 6** Resistance variation according to the gate field.

of the material phase change caused by heating induced by flowing current under bias. Although the change resulting from the Joule heating is currently small and irreproducible in the bulk substrates, we expect that the new high thermal impedance structures (SOI or wire etc.) will overcome these shortcomings. If successful, and if good reliability is achievable, this embodiment may be an appealing medium power and medium speed nonvolatile memory alternative suitable for embedded and stand-alone applications.

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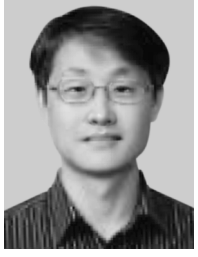

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