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Dual-Gate ZnO Thin-Film Transistors with SiNx as Dielectric Layer

Young Su KIM[†], Min Ho KANG[†], Kang Suk JEONG[††], Jae Sub OH[†], Yu Mi KIM[††], Dong Eun YOO[†], Hi Deok LEE[††], *and* Ga Won LEE[††a)], *Nonmembers*

SUMMARY We report on the fabrication of coplanar dual-gate ZnO thin-film transistors with 200-nm thickness SiN_x for both top and bottom dielectrics. The ZnO film was deposited by RF magnetron sputtering on SiO_2/Si substrates at 100°C. And the thickness of ZnO film is compared with 100-nm and 40-nm. This TFT has a channel width of 100-μm and channel length of 5-μm. The fabricated coplanar dual-gate ZnO TFTs of 40-nm-thickness exhibits a field effect mobility of about 0.29 cm^2/V s, a subthreshold swing 420 mV/decade, an on-off ratio 2.7×10^7, and a threshold voltage 0.9 V, which are greatly improved characteristics, compared with conventional bottom-gate ZnO TFTs.

key words: *ZnO, TFT, dual gate, sputter*

1. Introduction

ZnO-based thin film transistors (TFTs) have attracted a lot of attention because of wide band gap, transparency, and high field effect mobility, compared to that of the conventional a-Si TFTs [1]–[3]. Recent advances in ZnO-based TFTs and their application have been devoted to achieving driver or peripheral circuit components of next generation display [4]–[6]. ZnO is a material that has higher n-type conductivity unintentionally. The n-type characteristics of un-doped ZnO channel layers result from zinc interstitials or oxygen vacancies [7], [8]. Normally, there are more mobile carriers at top-side of ZnO film than bottom-side because of the increase of ZnO crystallization as-grown [9]. As for TFT structures, bottom-gate ZnO TFTs are preferred to top-gate type because higher quality of gate insulator can be made regardless of the temperature limitation by active channel formation. And turn-on voltage and hump characteristics of bottom-gate ZnO TFTs are largely dependent on oxygen concentration during ZnO sputtering in fabrication process. As ZnO TFT is deposited in low oxygen concentration relatively, large negative turn-on voltage and hump are generated by donorlike trap [10]. As we compare staggered type with coplanar type on condition of the same gate type and same oxygen concentration, coplanar type shows the depleted characteristics due to the low contact resistance. But coplanar type source/drain also presents higher on-current because of lower contact resistance than staggered type. In this study, we examined the characteristic depending on the structural change on condition that the structures of coplanar bottom gate, coplanar top gate and coplanar dual-gate in the same wafer are split in the same oxygen concentration during ZnO sputtering. Dual-gate structure on ZnO TFTs was reported by Park et al. [11]. They were made by using Al_2O_3 as gate insulator and by using top contact of channel while our dual-gate device is manufactured using SiNx as gate insulator and using bottom contact structure. We also analyze the structural and electrical characteristics comparing bottom-gate and top-gate with dual-gate ZnO TFTs according to the channel thickness.

2. Experiment

Figure 1 is the schematic cross section and Fig. 2 is the process flow of the coplanar dual-gate ZnO TFTs with 200-nm-thick SiNx for both top and bottom dielectrics. Bottom gate insulator was deposited at high temperature but top gate insulator was deposited at low temperature after ZnO deposition. The fabrication process was as follows, a 100-nm-thick Ti was deposited as a bottom gate by RF magnetron sputtering and patterned by lithography and dry etch process. Then, a 200-nm-thick SiNx was deposited as the gate insulator by conventional PE-CVD at 400°C and 100-nm-thick Ti was deposited as a channel pad by RF magnetron sputtering and patterned by lithography and dry etch process. The ZnO channel layers with 40-nm-thick and 100-nm-thick were deposited on the gate insulator and channel pad by using a RF magnetron sputtering in Ar/O_2 (60%/40%) at 100°C. A 50-nm-thick. SiNx film was deposited on the ZnO by PE-CVD at 150°C in order to protect the body of ZnO TFTs since the ZnO film was easily damaged by developer which were used in a photolithography process [12]. The SiNx and ZnO films were patterned by the dry etching. The dry etching gases of ZnO channel were HBr and Ar [13]. After definition of the active channel, a 150-nm-thick SiNx for the top gate insulator was deposited by PE-CVD at 150°C. Contact holes for source and drain electrodes were opened by the dry etching. And then a 100-nm-thick Ti for source/drain electrodes and a top gate was deposited by RF magnetron sputtering at room temperature and was patterned by the dry etching. The channel length and width are 5-μm and 100-μm, respectively. For the comparison of electrical characteristics, we also fabricated the conventional bottom-gate and top-gate ZnO TFTs on the same wafer. The ZnO and SiNx

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[†]The authors are with National Nanofab Center, Daejeon 305-806, Korea.
[††]The authors are with Dept. of Electronic Engineering, Chungnam National University, Daejeon 305-764, Korea.
a) E-mail: gawon@cnu.ac.kr

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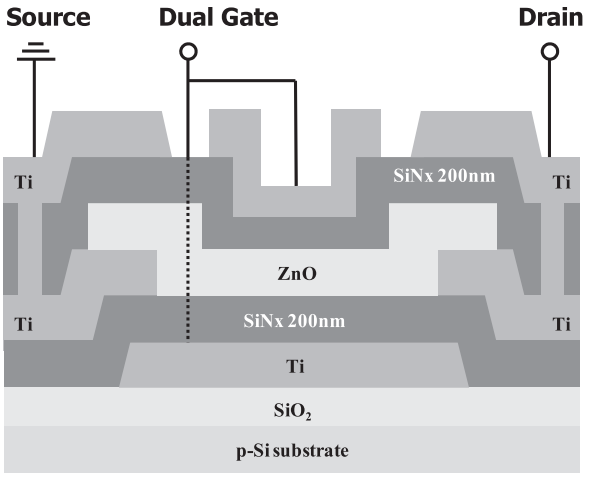

Fig. 1 Schematic cross-section of the dual-gate ZnO TFTs. A 200-nm-thick SiNx layer as a gate insulator is used at the both sides of ZnO channel.

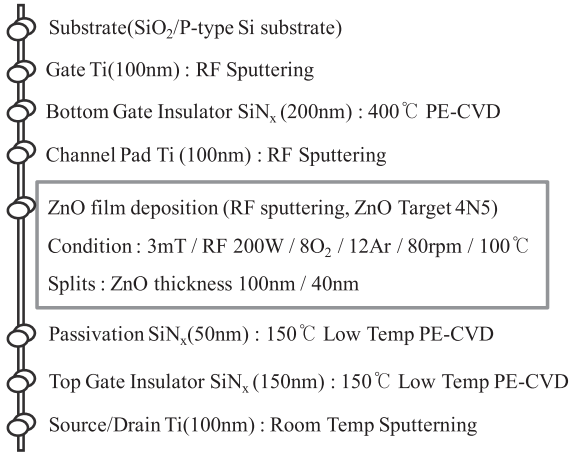

Fig. 2 Conditions of film deposition for coplanar dual gate ZnO TFTs.

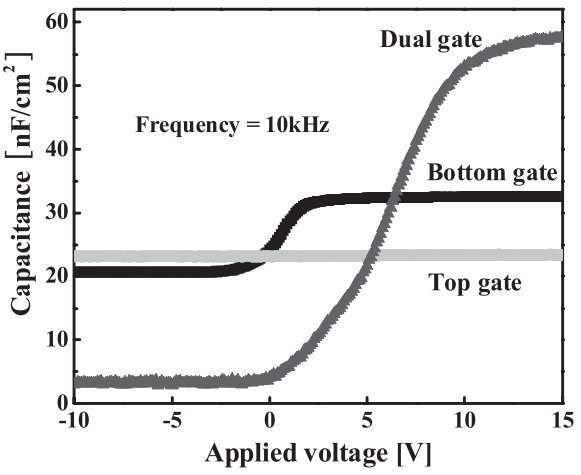

Fig. 3 Capacitance-voltage (C-V) characteristics of ZnO TFTs with various gate types measured at 10 kHz.

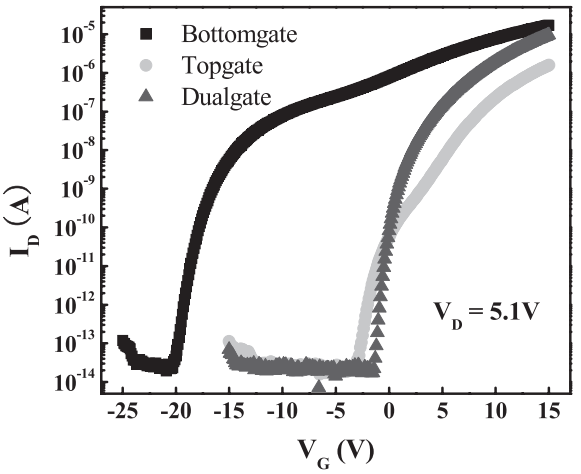

Fig. 4 The transfer curves ($\log_{10}(I_D)$-V_G curves) obtained from the bottom- gate, top-gate and dual-gate for 100-nm-thick ZnO TFTs.

film thickness were measured using a spectroscopic ellipsometer and cross-sectional SEM. The structural characteristics are analyzed by XRD and the devices are electrically characterized in the air, at room temperature, and in the dark using Keithley 4200 semiconductor parameter analyzer with common bottom- gate and top-gate.

3. Results and Discussion

Figure 3 shows the capacitance-voltage (C-V) characteristics of W/L = 100-μm/100-μm. These C-V characteristics show n-channel behavior operating in accumulation mode on a positive gate bias. C_{itop}, gate capacitance of top-gate is 2.34×10^{-8} F/cm^2, C_{ibot} of bottom-gate value is 3.26×10^{-8} F/cm^2 and C_{idual} of dual-gate value is 5.87×10^{-8} F/cm^2. C_{idual} is equal to the summation of C_{ibot} and C_{itop}. The low capacitance and poor voltage dependence of C_{itop} are due to depleted characteristic of top-gate insulator deposited at low temperature and high density of the intrinsic defects at top-side of ZnO [14]. And the capacitance at the depletion region for dual-gate structure is so small compared to that of bottom and top-gate structures. At C-V measurement, the ground plate positions of top and bottom-gate are contacted in the surface of ZnO while the position of dual-gate is contacted in the interface of ZnO due to structural restriction. The position difference causes to lowering the capacitance at the depletion region. Figure 4 and Fig. 5 show the transfer curves ($\log_{10}(I_D)$-V_G curves) obtained from the bottom-gate, the top-gate and the dual-gate on 100-nm-thick ZnO TFTs and 40-nm-thick ZnO TFTs, respectively. The 100-nm-thick ZnO TFTs show that the turn-on voltage, V_{ON} is appeared in −20.2 V at the bottom-gate and −3.3 V at the top-gate, respectively while V_{ON} is about −1.5 V at the dual-gate. In the case of 40-nm-thick ZnO TFTs, V_{ON} is appeared in −11.3 V at the bottom-gate and −4.6 V at the top-gate, respectively while V_{ON} is about −1.4 V at the dual-gate. Here, the turn-on voltage is defined as the gate voltage corresponding to the onset of the initial sharp increase of current in a $\log_{10}(I_D)$-V_{GS} curves [15]. To analyze the large difference of V_{ON} of bottom gate TFTs according to the channel thick-

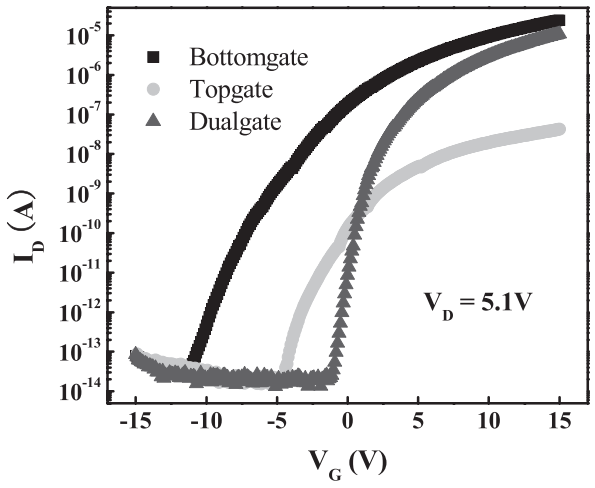

Fig. 5 The transfer curves ($\log_{10}(I_D)$-V_G curves) obtained from the bottom- gate, top-gate and dua- gate for 40-nm-thick ZnO TFTs.

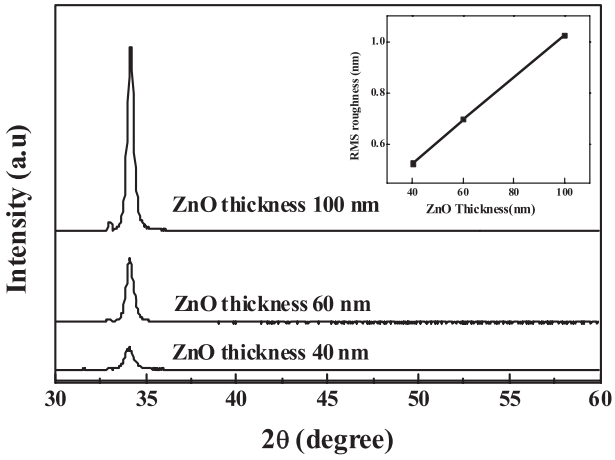

Fig. 6 XRD spectra and AFM RMS roughness (inset) of the ZnO films deposited at 100°C as a function of the film thickness.

ness, the crystallinity is analyzed by XRD and AFM. Figure 6 shows the XRD spectra and inset in Fig. 6 represents AFM RMS roughness of the ZnO films for various thicknesses. All the films exhibited only one peak corresponding to the ZnO (0 0 2) orientations in the range of 30–60°, indicating that the films have the c-axis preferred orientation with poly crystalline structure [16]. The peak intensity of XRD and RMS surface roughness (from 0.5 nm to 1.0 nm) increased as film thickness increase from 40-nm to 100-nm. It means that the grain size gets bigger because of crystallization by thermal diffusion as long as deposition time and that the crystallinity of the thick films is enhanced. Therefore, the great differences of V_{ON} can be explained by considering the possible current paths in ZnO TFTs. Figure 7 shows the schematic of a conventional bottom-gate TFT with two parallel current paths [17]. One ($I_{D,Bottom}$) is the current path through the accumulation layer induced by the gate voltage and the other ($I_{D,Top}$) is by mobile carriers pre-existing at the opposite region of gate (top side of the

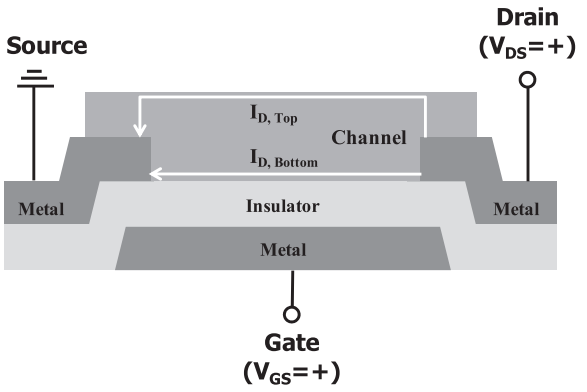

Fig. 7 Schematic of a bottom-gate TFT with two parallel current paths. Here, $I_{D,Bottom}$, is due to carriers induced by gate bias. $I_{D,Top}$ is due to mobile carriers pre existing at the top of channel [17].

Table 1 Device parameters of various gate types for 100-nm-thick and 40-nm-thick ZnO TFTs. Here, the field effect mobility is estimated at linear region.

	100nm-thick ZnO			40nm-thick ZnO		
Gate types	Bottom	Top	Dual	Bottom	Top	Dual
Threshold voltage [V]	-17	2.3	0.6	-5.9	1.5	0.9
Turn-on voltage [V]	-20.2	-3.3	-1.5	-11.3	-4.6	-1.4
Saturation current [μA]	0.038	0.043	0.22	0.089	0.008	0.46
On/off ratio	1.5×10^6	1.9×10^6	8.8×10^6	2.2×10^6	4.2×10^5	2.7×10^7
Subthreshold swing [V/dec]	0.65	0.56	0.32	0.95	0.74	0.42
Mobility, μ_{FEin}[cm^2/Vs]	0.012	0.013	0.25	0.003	0.002	0.29

channel).

When the free carrier concentration especially at the top side becomes large enough to be normally-on, the bottom-gate TFTs can turn on in negative gate bias range causing hump. That's why the thicker ZnO TFT is, the larger grain size is and grain boundaries as electron scattering centres could be small in the thick film. This phenomenon will be apparent as the crystallinity of the top side of the channel improves and so 100-nm-thick ZnO TFT shows more negative V_{ON}.

This top current path by the mobile carriers can be controlled in the top-gate structure and so V_{ON} can be made to shift to more positive range as shown in Fig. 4 and Fig. 5. When the gate bias is applied at both side of channel as in the dual-gate type, the early V_{ON} disappears due to fully depletion of channel. This removal of parasitic current path in the dual-gate greatly contributes to the improvement of subthreshold swing (SS) as shown in Table 1 where SS in the dual-gate of 40-nm-thick ZnO is dramatically improved as 0.42 V/decade, compared with bottom-gate of 0.95 V/decade and top-gate 0.74 V/decade. The linear mobility of each gate type is also compared in Table 1 which is extracted at $V_G - V_{th}$ = 10 V and V_{DS} = 0.1 V. The mobility is worst in top-gate structure. This is thought to be related with the depleted characteristic of top-gate insulator

deposited at low temperature as the temperature limitation by active channel formation. The threshold voltage, V_{th} and On/Off current ratio, $I_{ON/OFF}$. V_{th} is calculated at 10 nA × L/W as constant current mode and I_{ON} is estimated at V_{DS} = 5.1 V and $V_G - V_{th}$ = 5 V.

I_{Off} is the leakage current when the gate voltage is just below V_{ON}. It can be seen that $I_{ON/OFF}$ is improved 10 times better than bottom gate of 2.2×10^6, as $I_{ON/OFF}$ is 2.7×10^7 in the dual-gate of 40-nm-thick ZnO, which is also due to the superior SS characteristics and dual current path of the dual-gate structure.

4. Conclusions

In summary, the device performance of coplanar dual-gate ZnO TFTs is dramatically improved without additional process and post treatment, compared with the bottom-gate and top-gate ZnO TFTs. This is mainly due to the improved subthreshold slop characteristics by controlling the mobile carriers at the top side which can cause hump making the parasitic current path. The mobile carriers inducing current path have the process-dependent properties which are difficult to control. Therefore, the dual-gate structure is desirable in view of fabricating ZnO TFTs with high performance and uniform characteristics.

Acknowledgments

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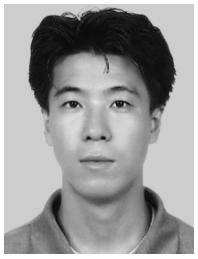
Young Su Kim received the B.S. degree in Mechanical Engineering from Busan National University, Busan, Korea (1998), and the M.S. degree in the Department of Electronics Engineering from the Chungnam National University, Daejeon, Korea (2010). He is currently working toward the Ph.D. degree in the Department of Electronics Engineering, Chungnam National University, Daejeon, Korea. In 1994, he joined LG Semiconductor Inc. Cheongju, Korea (currently Hynix Semiconductor Inc.) and participated in the process engineering department for DRAMs. He is currently working in National Nanofab Center (NNFC) in Daejeon, Korea. His main research fields are oxide TFT, MEMS and Bosch Process etching.



Min Ho Kang received the B.S. degree in material science and engineering from Korea University, Seoul, Korea (2000), and the M.S. degree in the Department of Electronics Engineering from the Chungnam National University, Daejeon, Korea (2009). He is currently working toward the Ph.D. degree in the Department of Electronics Engineering, Chungnam National University, Daejeon, Korea. From 2000 to 2005, he joined Hynix Semiconductor Ltd. as thin film process engineer, where he was involved in the 200 mm and 300 mm thin film process development of DRAM technologies. Since 2006, he is currently working in National NanoFab Center (NNFC) in Daejeon, Korea. His main research fields include multilevel interconnect technology, germanide technology, Schottky barrier MOSFETs and high performance nano-scale Ge MOSFETs.

Kang Suk Jeong received the B.S. degree in electronics engineering from Chungnam National University, Daejeon, Korea, in 2007. From 2009, he has in depth been studying semiconductor devices through the electrical and optical characteristics analysis of TFTs such as LTPS TFT, Organic TFT and Oxide-based TFT in electronics engineering from Chungnam National University graduate school, Daejeon, Korea.

Jae Sub Oh received the B.S. degrees in Metallurgical Engineering from Jeonbuk National University, Jeonju, Korea in 1997. He is pursuing a M.S. and Ph.D. degrees at the Department of Electronics Engineering, Chungnam National University, Daejeon, Korea. From 1997 to 2004, he was with Hynix Semiconductor Inc. (originally LG Semiconductor Inc.) Ichon, Korea, where he was involved in the development of 0.18-, 0.13- and 0.115-μm CMOS process technologies. Since 2004, he has been with National Nanofab Center, Daejeon, Korea, as a Senior Technical Staff. His main research fields are nano-scale CMOS including nonvolatile-memory and flexible display technology.

Yu Mi Kim received the B.S. degree in Electronics Engineering from Uiduk University, Gyeongju, Korea, in 2005. From 2005 to 2008, she joined ULTECH Co., Ltd., Daegu, Korea and participated in Research & Development department for semiconductor manufacturing systems. She is currently working toward the M.S. degree in Chungnam National University, Daejeon, Korea. Her main research fields are the electrical and optical characteristics analysis of the oxide-based TFTs.

Dong Eun Yoo received the B.S. degree in Electrical Engineering from Chungnam National University, Daejeon, Korea in 2004. From 2004 to 2007, he served as a Equipment Engineering in Magnachip Semiconductor Ltd., Chungju, Korea (originally Hynix Semiconductor Inc.). Since 2007, he has been with National NanoFab Center, Daejeon, Korea, where he currently serves as a Technical Staff in the development area of Nano Fabrication Technology.

Hi Deok Lee received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1990, 1992, and 1996, respectively. In 1996, he was with the LG Semicon Company, Ltd., where he has been involved in the development of 0.35- to 0.13-μm CMOS technologies. Since 2001, he has been with Chungnam National University, Daejeon, Korea, as an Associate Professor with the Department of Electronics Engineering. From 2006 to 2008, he was with the University of Texas, Austin, and SEMATECH, Austin, as a Visiting, Scholar. His research interests are in the areas of nanoscale CMOS technology including RF CMOS devices.

Ga Won Lee received the B.S., M.S., and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1994, 1996, and 1999, respectively. In 1999, she joined Hynix Semiconductor Ltd. as senior research engineer, where she was involved in the development of 0.115-μm, 0.09-μm DDRII DRAM technologies. Since 2005, she has been in Chungnam National University, Daejeon, Korea, as an Associate Professor with the Department of Electronics Engineering. Her main research fields are flash memory, flexible display technology including fabrication, electrical analysis and modeling.