PAPER

Low Pass Filter-Less Pulse Width Controlled PLL Using Time to Soft Thermometer Code Converter

Toru NAKURA[†a)] ***and*** **Kunihiro ASADA**[†], ***Members***

SUMMARY This paper demonstrates a pulse width controlled PLL without using an LPF. A pulse width controlled oscillator accepts the PFD output where its pulse width controls the oscillation frequency. In the pulse width controlled oscillator, the input pulse width is converted into soft thermometer code through a time to soft thermometer code converter and the code controls the ring oscillator frequency. By using this scheme, our PLL realizes LPF-less as well as quantization noise free operation. The prototype chip achieves 60 μm × 20 μm layout area using 65 nm CMOS technology along with 1.73 ps rms jitter while consuming 2.81 mW under a 1.2 V supply with 3.125 GHz output frequency.

key words: *PLL, PWCO, pulse width control, soft thermometer code, LPF-less, quantization noise free*

1. Introduction

As the process technology advances, power supply voltage scales down while transistor switching speed increases. For analog circuit design, the reduced supply voltage means degraded voltage-domain resolution while the high-speed transistors provide improved time-domain resolution. We are facing a new paradigm that time-domain resolution of a digital signal edge transition is superior to voltage-domain resolution of analog signals [1].

A PLL is one of the most fundamental building blocks of LSIs. Particularly, small layout area and low jitter operation are strongly required for the PLL design. Conventional analog PLLs shown in Figs. 1(a) and (b) control the oscillation frequency of the VCO (Voltage Controlled Oscillator). The PFD compares the VCO output with the reference CLK input and the charge in proportion to the phase difference is injected into the LPF, and the LPF output voltage controls the VCO frequency so as to match with the reference CLK. The PLLs in Figs. 1(a) and (b) are called Type-I and Type-II PLL, respectively. The Type-I PLL uses large capacitor C_m to convert the PFD output into control voltage for the VCO. The Type-II PLL also uses large capacitor C_m to stabilze the feedback loop. Thus, conventional analog PLLs consume large layout area as well as their analog control of degraded voltage-domain resolution in reduced supply voltage, resulting in large jitter.

Recently, the all digital PLL structure shown in Fig. 1(c) is becoming mainstream in the advanced CMOS process. The all digital PLL converts the PFD output pulse width into digital bits by the TDC (Time to Digital Converter), and the following DF (Digital Filter) outputs the digital bits to control the DCO (Digitally Controlled Oscillator) frequency. The digital PLL is free from the area-consuming capacitor C_m as well as free from the subtle analog voltage control, so that it overcomes the drawbacks of the analog PLL. However, the digital PLL inherently suffers from quantization noise, resulting in large jitter. One of the causes of the quantization noise is the communication between the DF and the DCO. The number of bits from the DF output is larger than the number of bits to the oscillator input in DCO, thus the DF output is dithered using a DSM (ΔΣ Modulator). The other cause of the quantization noise is the TDC whose conversion resolution is limited by a single inverter gate delay, and most of efforts in the digital PLL design are made to realize a finer time resolution of the TDC. These additional circuits for the quantization noise reduction in the digital PLL tend to increase the number of transistors used, which makes it difficult to reduce the chip area as well as its power consumption.

This paper proposes PWCO (Pulse Width Controlled Oscillator) whose oscillation frequency is controlled by the input pulse width, and demonstrates LPF-less pulse width controlled PLL (PWPLL) using the PWCO. The PWPLL

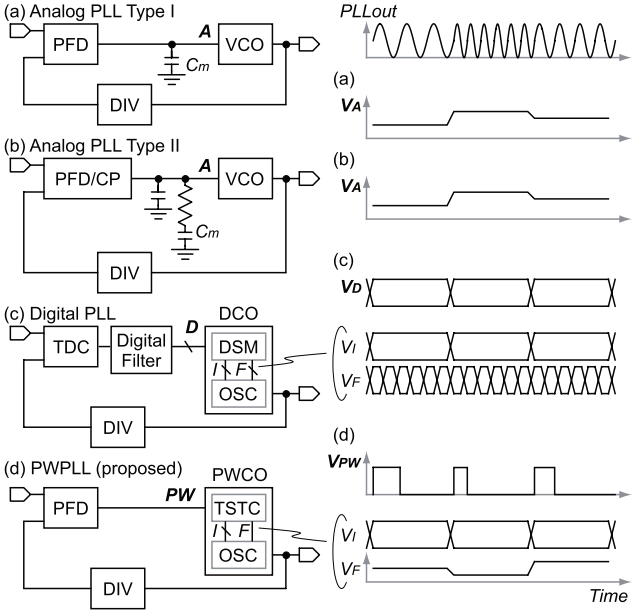

Fig. 1 Typical PLL architectures and their oscillator control signals.

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not only relaxes the voltage-domain subtle analog control but also realizes the LPF-less area efficiency.

2. Circuit Design

2.1 PWCO and Soft Thermometer Code

The feedback principle of the PWPLL is similar to the Type-I analog PLL shown in Fig. 1(a). The PFD outputs the pulse whose width is the same as the phase difference between the two inputs, reference clock and the divided feedback clock. In the Type-I analog PLL, the PFD output pulse is low pass filtered into an analog control voltage by the capacitor C_m and controls the VCO frequency, thus the ripple on the control voltage induced at every rising edge of the reference clock causes jitter.

On the other hand in our PWPLL, the PWCO converts the PFD pulse width into N bit code as shown in Figs. 2(a) and (b), where the code has many ZEROs with wider pulse width ($N = 8$ in this figure). We call the code a soft thermometer code. The key point of the soft thermometer code is that the ONE/ZERO boundary has an analog voltage so as not to generate the quantization noise which the normal thermometer code inevitably has. Inside of the PWCO, the soft thermometer code is fed to the multiple terminal ring oscillator to adjust the oscillation frequency. The overall PLL block diagram is shown in Fig. 1(d), and the PLL feedback loop locks when the PFD output pulse width, which is the same as the phase difference of the PFD inputs, corresponds to the appropriate soft thermometer code that generates the target frequency at the ring oscillator where the divided clock has the same frequency as the input reference clock.

The relation between the PFD output pulse width PW and the oscillator control voltage are shown in Figs. 2(d) and (e) for the analog PLL, and the PWPLL, respectively, yet both of them have the similar pulse width vs. frequency relation as shown in Fig. 2(f). Since only one (or two) node has an analog voltage and the others have V_{DD} or G_{ND} level at the soft thermometer code, the analog voltage fluctuation causes less jitter compared with the fluctuation of V_A in the analog PLL. In addition, the soft thermometer code does not require the large capacitor C_m since the PFD output pulse width is not directly low pass filtered.

As shown in Fig. 2(e), the slope region of V_{STi} and V_{STi+1} should overlap otherwise there exists a dead zone where the pulse width change is insensitive to the soft thermometer code change.

There is a scheme to use a digital control to select a "bank" in addition to the analog control voltage in order to increase the oscillation frequency range, as shown in Fig. 2(g), such as to switch ON/OFF the additional load on the ring oscillator together with the analog voltage control of the varactor. In this scheme, the nodes with the digital voltage and the nodes with the analog voltage are fixed and it requires sophisticated digital signal control. In contrast, our PWCO converts a PFD pulse into digital signals with the minimum use of an analog voltage where the node with the analog voltage changes in accordance with the incoming pulse width.

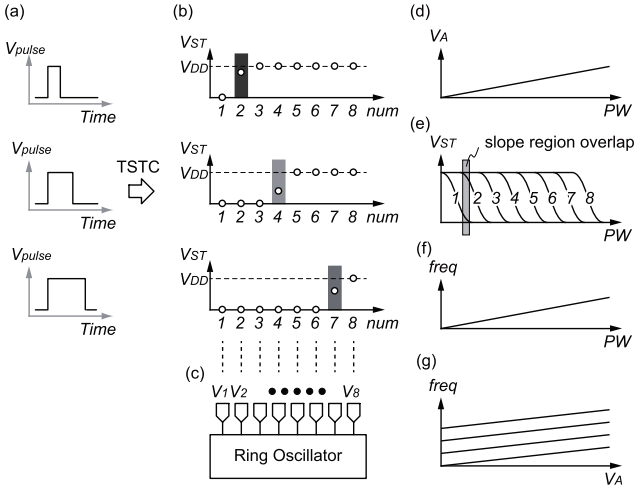


Fig. 2 Pulse width to soft thermometer code conversion.

2.2 Schematics

The schematics of the PWCO including TSTC (Time to Soft Thermometer code Converter) and a ring oscillator are shown in Fig. 3, and Fig. 4 shows their timing diagram. The input pulse from the PFD is delayed by DLY before entering the N stage buffer. Since each stage has a delay, the first k stage input is ONE and the last $N - k$ stage input is ZERO

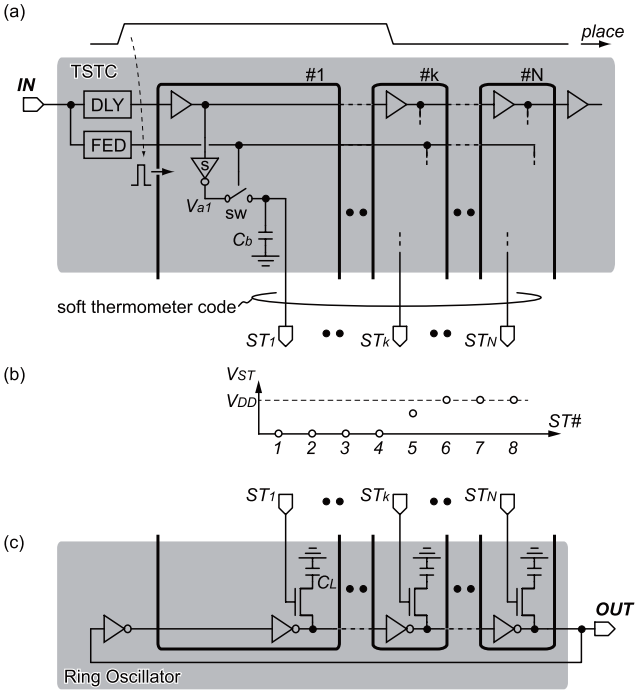


Fig. 3 Schematics of the time to soft thermometer code converter and the soft thermometer code controlled oscillator.

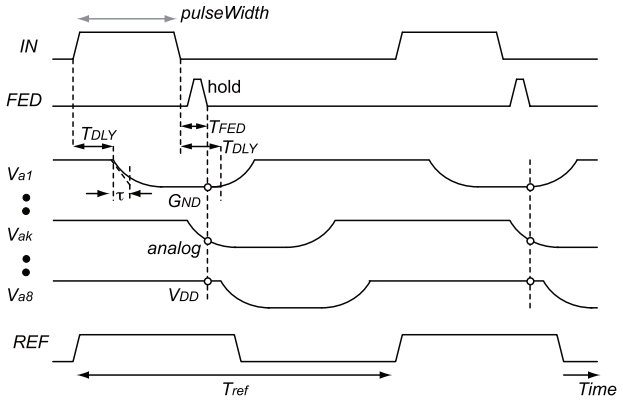


Fig. 4 Timing diagram.

at the falling edge of the input pulse, where k depends on the input pulse width. $N = 8$ and $k = 5$ in the example of Fig. 3(b). The input of each stage is inverted by the slow inverter denoted "s" in the inverter symbol in Fig. 3(a) in order to derive a slow fall time, and the inverter output voltage V_a is sampled and held to the output by the FED (Falling Edge Detector) pulse that is generated at the falling edge of the input pulse from the PFD, as shown in Fig. 4. In this way, the soft thermometer code output becomes that the first $k-1$ stage output is ZERO, the output after the $k+1$ stage is ONE and the boundary k-th stage has an analog voltage.

The converted soft thermometer code is fed to the ring oscillator whose load capacitor of each stage is controlled by the soft thermometer code input, as shown in Fig. 3. The wider pulse width from the PFD generates more ZEROs in the soft thermometer code and makes the higher oscillation frequency.

2.3 Timing Constraints

The fall time of the slow inverter is controlled by the drivability of the inverter and the load capacitor as shown in Fig. 3(a). The time constant τ plays an important role for generating the analog voltage for the ONE/ZERO boundary of the soft thermometer code as shown in Fig. 4.

Here, the slope region overlap between V_{STi} and V_{STi+1} shown in Fig. 2(e) is realized when τ is larger than the 1 stage delay, T_{stage}, and the slope region overlap gets wider as τ becomes larger. Then V_{STi}, V_{STi+1} and V_{STi+2} would have slope region overlap if τ is larger than $2T_{stage}$, but in such case, the three nodes would have analog voltage at the same time which is not desired situation for the noise tolerance. So,

$$T_{stage} < \tau < 2T_{stage} \tag{1}$$

is recommended for realizing the smooth pulse width to soft thermometer code conversion by having an appropriate slope region overlap of i-th and $i+1$-th curve shown in Fig. 2(e).

The delay of DLY (T_{DLY}) is set to be larger than the delay of FED (T_{FED}) to insure that V_a of the first stage is sampled and held to be ZERO before going up as shown in Fig. 4. It guarantees the monotonicity of the relation between the pulse width and the soft thermometer code even when the incoming pulse width is short.

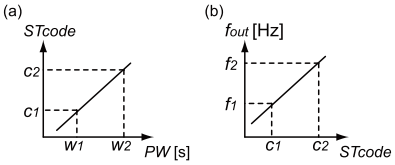


Fig. 5 Relations between (a) Pulse width vs. Soft thermometer code of TSTC, (b) Soft thermometer code and oscillation frequency of the ring oscillator.

The other timing constraints is that the input pulse width should be larger than the delay of DLY and to be smaller than the N stage delay ($N \cdot T_{stage}$). Also the N stage delay should be smaller than the reference clock period (Per_{ref}), to complete the soft thermometer code conversion before the next input pulse comes at the rising edge of the reference clock. These constraints are expressed as

$$T_{FED} < T_{DLY} < PW < N \cdot T_{stage} < Per_{ref}. \tag{2}$$

2.4 PLL Loop Dynamics

The gain of the pulse width to soft thermometer code converter K_{TSTC}[1/rad] and the gain of the soft thermometer code to the oscillator angular frequency K_{RO}[rad/s] are expressed as

$$K_{TSTC} = \frac{c_2 - c_1}{2\pi f_0 (w_2 - w_1)} \tag{3}$$

$$K_{RO} = \frac{2\pi(f_2 - f_1)}{c_2 - c_1} \tag{4}$$

where $w_1, w_2, c_1, c_2, f_1, f_2$ are shown in Fig. 5, and f_0 is the target frequency. Note that the unit of w and $2\pi f_0 w$ are [s] and [rad], respectively.

The transfer function of each block is as follows,

$$H_{PFD} = 1 \tag{5}$$

$$H_{TSTC} = K_{TSTC} \tag{6}$$

$$H_{RO} = K_{RO}/s \tag{7}$$

$$H_{d1} = e^{-t_1 s} \tag{8}$$

$$H_{d2} = e^{-t_2 s} \tag{9}$$

$$H_{DIV} = 1/M_{DIV} \tag{10}$$

$$H_{closed} = \frac{H_{PFD}H_{TSTC}H_{RO}H_{d1}}{1 + H_{PFD}H_{TSTC}H_{RO}H_{d1}H_{DIV}H_{d2}} = \frac{K_{TSTC}K_{RO}e^{-t_1 s}}{s + \frac{K_{TSTC}K_{RO}e^{-(t_1+t_2)s}}{M}} \tag{11}$$

where t_1 is the delay from PFD to the frequency change of the oscillator, and t_2 is the delay of the $1/M$ divider circuit. The closed loop transfer function of the PWPLL is expressed as H_{closed} of Eq. (11). When we neglect the delay t_1 and t_2, the transfer function of our PWPLL becomes first

order system whose time constant is $M/(K_{TSTC} \cdot K_{RO})$.

In order to compare the transfer function with Type-I PLL, where

$$K_{PD} = \frac{V_{out}}{\Delta\phi} = \frac{V_{out}}{2\pi f_0 w} \tag{12}$$

$$K_{VCO} = 2\pi f / V_{out} \tag{13}$$

thus

$$K_{PD} \cdot K_{VCO} = \frac{f}{f_0 w} \tag{14}$$

From Eqs. (3) and (4),

$$K_{TSTC} \cdot K_{RO} = \frac{f}{f_0 w} \tag{15}$$

which is identical to Eq. (14), and both of them show the replations of PFD pulse width to output frequency conversion. Therefore, our PWPLL transfer function is the same as the one of a Type-I PLL with very high frequency pole LPF (equivalent with no LPF case) by replacing $K_{PD} \cdot K_{VCO}$ with $K_{TSTC} \cdot K_{RO}$.

2.5 Pulse Width vs. Frequency

When the input pulse enters the TSTC, the larger stage delay reduces the number of stages to propagate within the same pulse width period, and hence the number of ZEROs in the soft thermometer code is reduced, as shown in Fig. 3(a). Therefore the larger stage delay in TSTC makes K_{TSTC} smaller. In this case, the N stage delay can be larger as long as $N \cdot T_{stage} < Per_{ref}$ as shown in Eq. (2).

Here, the time constant τ in Fig. 4 is not included in the transfer function. The τ is used to make the slope region overlap in Fig. 2(e). However, the τ may result in local nonlinearity of pulse width vs. oscillation frequency relations of PWCO as shown in Fig. 7(a), and the global nonlinearity occurs if each stage has different delay. These nonlinearity may affect the PLL loop dynamics. Here, Fig. 7(a) shows post-layout simulation results of PWCO.

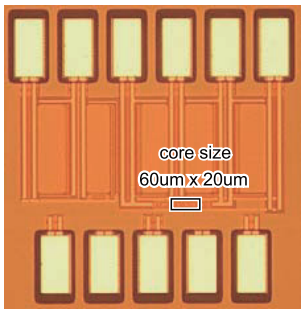
The larger C_L at the ring oscillator makes larger frequency change from the same soft thermometer code change, thus the larger K_{RO}.

The maximum frequency occurs when the PWCO pulse width is the same as the N stage delays and the soft thermometer code becomes all ZERO. The minimum frequency occurs when the pulse width is as small as T_{DLY} and the soft thermometer code becomes all ONE except V_{ST1} has an analog value. With this soft thermometer code, its oscillation frequency and locking range are decided by the ring oscillator with C_L.

3. Chip Design and Measurement

3.1 Chip Design

A prototype chip was designed and fabricated using 65 nm standard CMOS technology. The target frequency is 3.125 GHz with the division ratio of $M = 8$ thus the reference frequency is 390.625 MHz.



	L / W	# of Tr.
PMOS	65nm / 1.1um	255
NMOS	65nm / 0.5um	303
PMOS	250nm / 1.1um	8
NMOS	250nm / 0.5um	8

No resistor / inductor / MIMcap

Fig. 6 Chip photograph and the transistor count.

The number of stages N in Fig. 3 is 8 in our design. All the circuits except the slow inverters in Fig. 3(a) are designed with L=65 nm, W_p/W_n=1.1 μm/0.5 μm transistors including C_b and C_L in Figs. 3(a) and (b) consisting of 4 and 1 parallel NMOS gate capacitors, respectively. The slow inverters are designed to be L=250 nm with the same transistor width. The total transistor count is 574 (NMOS 311 and PMOS 263). No resistor/inductor/MIM cap is used. The core size is as small as 1200 μm^2 (60 μm $\times$ 20 μm) as shown in Fig. 6.

Note that C_b in TSTC is small enough to be realized by only 4 parallel MOS gate capacitors since the time constant τ is not so low as the time constant of the LPF in an analog PLL. It is also shown that C_b is not included in the transfer function in Eqs. (1)–(11). The role of C_m that converts the input pulse width into the oscillator control code, which is an analog voltage for VCO on an analog PLL, is realized in the time to soft thermometer code conversion of TSTC using only tiny capacitors.

Figure 7 shows (a) the input pulse width vs. frequency ($K_{TSTC} \cdot K_{RO}$) of PWCO, (b) PWPLL transfer function expressed in Eq. (11) with t_1=1 ns and t_2=0.3 ns, (c) the transient response of the output frequency. Figures 7(a) and (c) are the HSPICE post layout simulation results, and the parameters used in Fig. 7(b) are also extracted from the HSPICE post layout simulation. The bandwidth f_{BW} is around 5 MHz from Fig. 7(b), and the locking time could be $1/(2\pi f_{BW})$=32 ns, which is not so far from the transient response of Fig. 7(c).

3.2 Measurement

The measurement was conducted using on-chip direct probing, as shown in Fig. 8. We used Agilent Technology Signal Generator N5181A to generate 390.625 MHz clock which is divided into two paths by a power splitter, one of which is used for the reference clock of the PLL and the other is used for the trigger of the sampling oscilloscope HP54750A in order to measure the 3.125 GHz (390.625 MHz $\times$ 8) PLL output. The rms jitter from the PLL was measured to be 1.73 ps as shown in Fig. 8(b), under a 1.2 V supply with 2.81 mW power consumption. The locking range is from 2.880 GHz

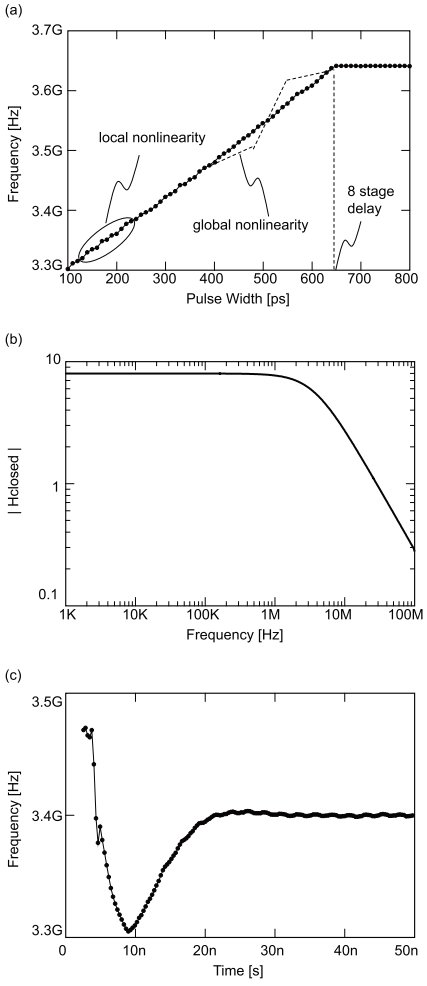


Fig. 7 Post-layout simulation results of (a) Input pulse width vs. frequency of PWCO, (b) Transfer function of PWPLL and (c) Transient response of the output frequency.

to 3.184 GHz under a 1.2 V supply and the rms jitter is almost constant along the locking range.

4. Discussion

4.1 Jitter Value

The measured PLL jitter was 1.73 ps, however, the signal generator and the oscilloscope themselves have internal jitter thus the intrinsic PLL jitter should be smaller than 1.73 ps. The signal generator is specified to have σ_{SG} ~0.5 ps rms jitter and the oscilloscope is specified to have 2 ps rms jitter at maximum. We measured the jitter from the signal generator with the oscilloscope by splitting the signal generator output, one of which is connected to the oscilloscope signal input while the other is connected to the oscilloscope trigger, and it measured $\sigma_{SG+OSC} = 1.46$ ps as shown in Fig. 9(a). Thus the oscilloscope internal jitter is calculated to be $\sigma_{OSC} = 1.37$ ps from $\sigma_{SG}^2 + \sigma_{OSC}^2 = \sigma_{SG+OSC}^2$. From the measurement results of the PLL output jitter $\sigma_{PLL+OSC} = 1.73$ ps, the PLL jitter is calculated to be

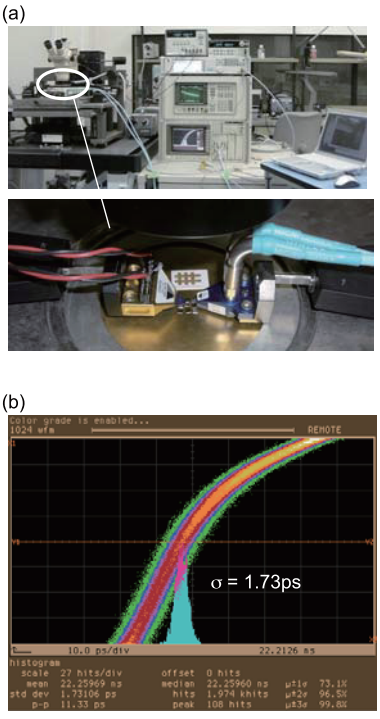


Fig. 8 (a) Measurement setup, (b) Measured PLL jitter.

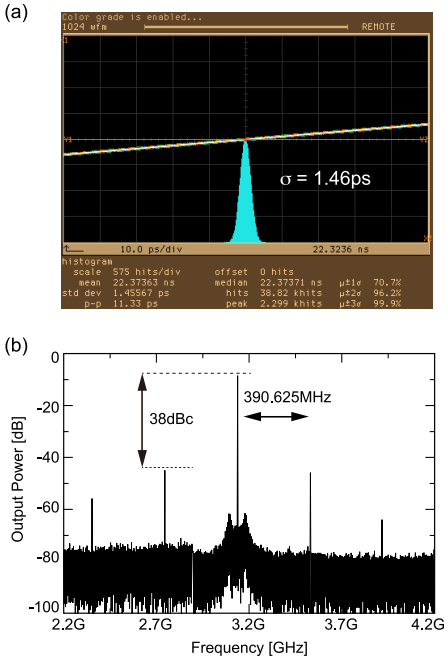


Fig. 9 (a) Measured jitter of the signal generator and the oscilloscope, (b) Measured PLL output spectrum.

$\sigma_{PLL} = 1.06$ ps from $\sigma_{PLL}^2 + \sigma_{OSC}^2 = \sigma_{PLL+OSC}^2$. In addition, since the PLL jitter includes jitter transfer from the reference clock, the intrinsic PLL jitter, which could be measured using a clean reference clock with a precise oscilloscope, is estimated to be ~1 ps.

Table 1 Comparison table.

	[2]	[3]	[4]	[5]	*This work*
Archtecture	Analog	Analog	Digital	Digital	**PW**
Frequency	2.5GHz	2GHz	5GHz	2.21GHz	**3.125GHz**
RMS Jitter	1.68ps	5.8ps	0.48ps	--	**1.73ps**
Power	6.19mW	1.2mW	5.4mW	3.8mW	**2.81mW**
Process	90nm	90nm	45nm	180nm	**65nm**
Area	0.027 mm^2	0.020 mm^2	0.0035 mm^2	0.20 mm^2	**0.0012 mm^2**
Norm. Area	3.4	2.5	1.7	6.2	**0.29**

4.2 Reference Spurious

The measured PLL output spectrum is shown in Fig. 9(b). It shows that the reference spurious noise is 38 dBc smaller than the peak power. The PFD works at every reference CLK and the SW in Fig. 3(a) switches ON and OFF, thus the ring oscillator frequency is fluctuated by the injected charge from the SW at every reference CLK. It is the cause of the reference spurious.

4.3 Comparison

The performance summary and comparison with small area and low jitter PLLs are listed in Table 1. Here the normalized area means the area divided by the square of the gate length and by 10^6: $0.0012\,\mathrm{mm}^2/(65\,\mathrm{nm})^2/10^6 = 0.29$ in our case. It shows that our pulse width controlled PLL achieves small area as well as low jitter.

5. Conclusions

We have demonstrated a PWPLL without using an LPF. A PWCO accepts the PFD output where its pulse width controls the oscillation frequency. In the PWCO, the input pulse width is converted into soft thermometer code through a TSTC and the code controls the ring oscillator frequency. By using this scheme, our PWPLL realizes LPF-less as well as quantization noise free operation. The prototype chip achieves $60\,\mu\mathrm{m} \times 20\,\mu\mathrm{m}$ layout area using 65 nm CMOS technology along with 1.73 ps rms jitter while consuming 2.81 mW under a 1.2 V supply with 3.125 GHz output frequency.

Acknowledgement

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Kunihiro Asada was born in Fukui, Japan, on June 16, 1952. He received the B.S., M.S., and Ph.D. in electronic engineering from the University of Tokyo in 1975, 1977, and 1980, respectively. In 1980 he joined the Faculty of Engineering, the University of Tokyo, and became a lecturer, an associate professor and a professor in 1981, 1985 and 1995, respectively. From 1985 to 1986 he stayed in Edinburgh the University as a visiting scholar supported by the British Council. From 1990 to 1992 he served as the first Editor of English version of IEICE (Institute of Electronics, Information and Communication Engineers of Japan) Transactions on Electronics. In 1996, he established VDEC (VLSI Design and Education Center) with his colleagues in the University of Tokyo. It is a center supported by the Government to promote education and research of VLSI design in all the universities and colleges in Japan. He is currently in charge of the head of VDEC. His research interests are design and evaluation of integrated systems and component devices. He has published more than 400 technical papers in journals and conference proceedings. He has received Best Paper Awards from IEEJ (Institute of Electrical Engineers of Japan), and ICMTS1998/IEEE and so on. He is a member of the Institute of Electrical and Electronics Engineers (IEEE), and the Institute of Electrical Engineers of Japan (IEEJ).