INVITED PAPER *Special Section on Josephson Junctions — Past 50 years and Future —*

Recent Developments of High-T_c Electronic Devices with Multilayer Structures and Ramp-Edge Josephson Junctions*

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SUMMARY Recent developments of electronic devices containing Josephson junctions (JJ) with high-T_c superconductors (HTS) are reported. In particular, the fabrication process and the properties of superconducting quantum interference devices (SQUIDs) with a multilayer structure and ramp-edge-type JJs are described. The JJs were fabricated by recrystallization of an artificially deposited Cu-poor precursory layer. The formation mechanism of the junction barrier is discussed. We have fabricated various types of gradiometers and magnetometers. They have been actually utilized for several application systems, such as a non-destructive evaluation (NDE) system for deep-lying defects in a metallic plate and a reel-to-reel testing system for striated HTS-coated conductors.

key words: *high-T_c superconductor, Josephson junction, ramp-edge, SQUID*

1. Introduction

Josephson effect is a unique characteristic of superconductivity [1]. Soon after the discovery of high-T_c superconductors (HTSs) in 1986 [2], one had expected realization of electronic devices utilizing the effect at high temperatures above a few tens of Kelvin or more. That was one of the great impacts of the discovery. Simultaneously, it was pointed out that superconducting connection was quite weak at the grain boundaries of polycrystalline HTS samples [3]. It was also revealed that HTSs intrinsically had a large anisotropy [4], [5]. These facts mean that HTSs with highly-controlled crystal orientation are needed to fabricate electronic devices. Preparation technique of superconducting thin films with high quality is a key for reproducible fabrication of JJs applicable to actual devices. Enormous efforts have been paid to establish the technique. For example, the relationship between oxygen partial pressure and temperature for successful deposition of high-quality superconducting films was clarified [6], [7]. Presently, HTS films suitable to device fabrication are prepared by various deposition techniques, such as pulsed laser deposition (PLD), sputtering, reactive coevaporation or molecular beam epitaxy (MBE), chemical vapor deposition (CVD) and so on. Various types of JJs were developed with the aim of application to electronic devices in 1990s. Successful preparation of JJs led to fabrication of superconducting quantum interference devices (SQUIDs). Since then, the fabrication technology of HTS-SQUIDs has been gradually improved. Presently we can find commercial SQUID magnetometers and gradiometers in actual market places [8]. Single flux quantum (SFQ) devices containing many JJs were designed and fabrication of HTS-SFQ digital circuits was also tried [9].

In the recent decade, our research group has investigated fabrication of HTS-SFQ circuits and HTS-SQUIDs. For the first several years, we had concentrated on constructing a stable fabrication process of JJs [10] and demonstrating proper logic operation of the HTS-SFQ circuits [11]. Then recent years, we have been developing various systems using HTS-SQUIDs utilizing the JJ-preparation technology improved in the former HTS-SFQ studies [12]. We developed the technology including superconducting wiring with multilayer structures and ramp-edge type JJs. In this paper, we mainly describe our JJ-preparation technology and recent activities on HTS-SQUID systems. Our results on HTS-SFQ are also described only briefly. Prior to the reports on our research activities, a general introduction on a variety of HTS-JJ types is briefly given.

2. Types of HTS Josephson Junctions

Observation of Josephson effect is one of indispensable conditions for establishment of superconductivity in a particular material. Following the discovery of HTSs, fabrication of JJs in forms of break junction [13] and point contact [14], as illustrated in Fig. 1, has been tried and physical properties of HTSs such as Josephson coupling and energy gaps were investigated. In these techniques, the surface plays an important role. The unknown altered layer at the surface has chances to form moderate junction barriers, when it is sandwiched by two superconductors. They are good techniques to try observing the particular phenomena.

Various types of JJs using superconducting thin films are illustrated in Fig. 2. Bi-crystal junctions [15], [16] (Fig. 2(a)) have been widely used, because of the easy fabrication process and moderately good reproducibility. However, the long grain boundary in a substrate gives restric-

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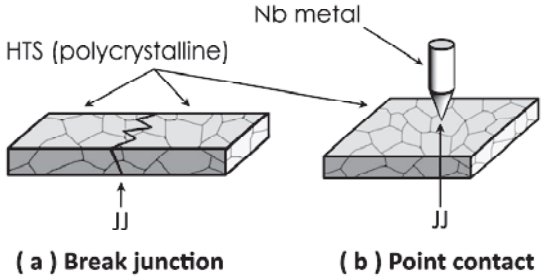

Fig. 1 Josephson junctions using polycrystalline HTS samples. (a) Break junction and (b) point contact.

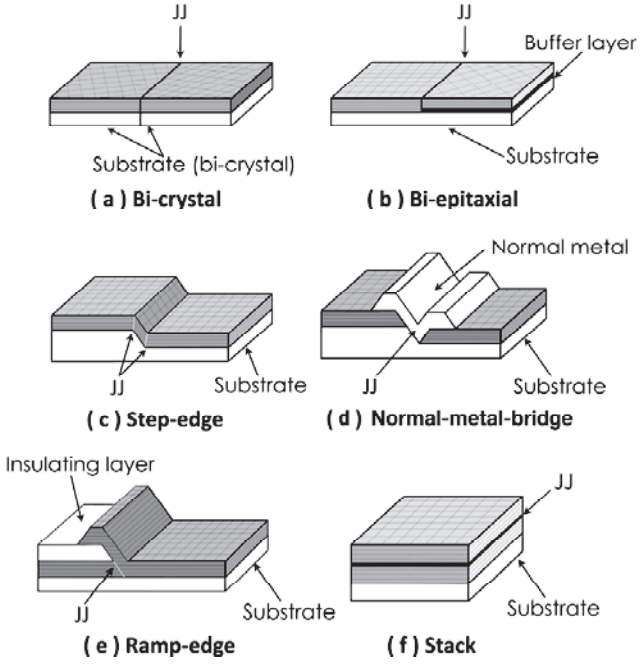

Fig. 2 Josephson junctions using HTS thin films. Superconducting films are *c*-axis oriented, i.e. the CuO_2 planes are parallel to the substrate surface.

tions to superconducting wiring design in a chip. The other types illustrated in Figs. 2(b)–2(f) do not have such disadvantage. One can prepare JJs at desired positions in a chip. Char et al. [17] developed a bi-epitaxial technique in which partially modified *in-plane* orientation by inserting a buffer layer is effectively utilized, as illustrated in Fig. 2(b). Steps artificially formed on a substrate surface are also effectively utilized to make JJs. Daly et al. [18] succeeded in demonstrating proper JJ operation at $YBa_2Cu_3O_y$ (YBCO) grain boundaries at steps artificially formed on a substrate (Fig. 2(c)). This type of JJ is also widely used in actual devices as well as bi-crystal JJs. Another type of JJ using a step on a substrate was developed by DiIorio et al. [19] and Ono et al. [20] Separated superconducting portions at a step are mediated by normal metal, as drawn in Fig. 2(d). This type of JJ is called as normal-metal-bridge JJ.

Two types of JJs having oxide multilayer structures were fabricated, as illustrated in Figs. 2(e) and 2(f). These are really attractive for realization of chips with complicated layout designs containing superconducting cross-over wiring. A well-improved fabrication process is required to realize them. One is a so-called ramp-edge type JJ (Fig. 2(e)) [21]–[24], the other is a stack type JJ (Fig. 2(f)) [25]–[27]. Barrier layers in both the types are artificially prepared by interface engineering techniques such as surface modification of the lower superconducting layer, namely base electrode (BE) [24], or by deposition of some non-superconducting materials [21]–[23]. In the ramp-edge JJs (Fig. 2(e)), ramp surface at which edges of CuO_2 planes appear is exposed and then the upper superconducting layer, namely counter electrode (CE), is deposited after proper interface engineering of the ramp. Usually, *c*-axis oriented films are used for superconducting electrodes. Josephson current in the direction being parallel to the CuO_2 plane passes through a barrier. The ramp-edge JJ has an overhang structure of CE. In the structure, the JJ barrier is covered with CE. We can expect that the superconducting CE works as a magnetic shield for the barrier. It is favorable from viewpoint of durability against the entry of flux vortices. Also, the tilted barrier seems to be tough against the vertically applied magnetic field [28]. In the stack type (Fig. 2(f)), a BE surface being parallel to the substrate is exposed before interface engineering. It means that Josephson current must pass in the direction vertical to the CuO_2 plane. It is technically difficult to fabricate an appropriate barrier for Josephson tunneling current along the direction with short coherence length. However, Kimura et al. [27] reported an encouragingly high I_cR_n value in their stack-type JJ. Development of reproducible fabrication technique is desired.

3. Preparation of Ramp-Egde Type JJs

Moeckly and Char [24] prepared YBCO ramp-edge JJs by modifying the edge surface through an ion bombardment and/or vacuum annealing process prior to CE deposition. This type of JJ has been called an "interface-engineered junction (IEJ)". Satoh et al. [29] demonstrated fabrication of JJs with a small I_c spread ($1\sigma = 8\%$ at 4.2 K for a 100-JJ series-array) utilizing a similar technique without an intentional ion bombardment. They called it as "interface-modified junction (IMJ)". The reported small I_c spread implied that this kind of method is promising to prepare well-controlled JJs with high reproducibility.

Wen et al. [30] studied the IMJ barrier prepared by Satoh et al. [29] in terms of structure and composition by means of a transmission electron microscope (TEM) and energy dispersive X-ray (EDX) spectroscopy. They revealed that an amorphous layer with a significantly Cu-poor or nearly Cu-free composition was formed on the surface of an ion-bombarded YBCO BE ramp edge before YBCO CE deposition. After the CE deposition, a thin barrier layer with a Cu-poor composition as compared with the stoichiometric YBCO was formed. They reported Ba:Y:Cu = 43:30:27 for the barrier layer, indicating that 27% Cu was supplied from

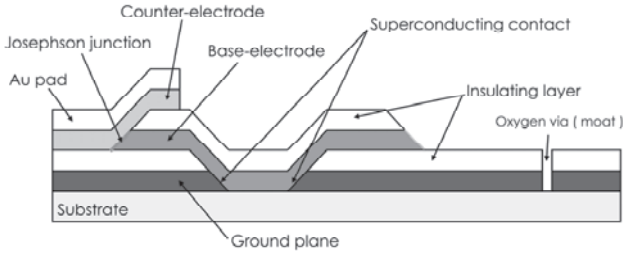

Fig. 3 Schematic illustration of cross-section of an HTS-SFQ circuit.

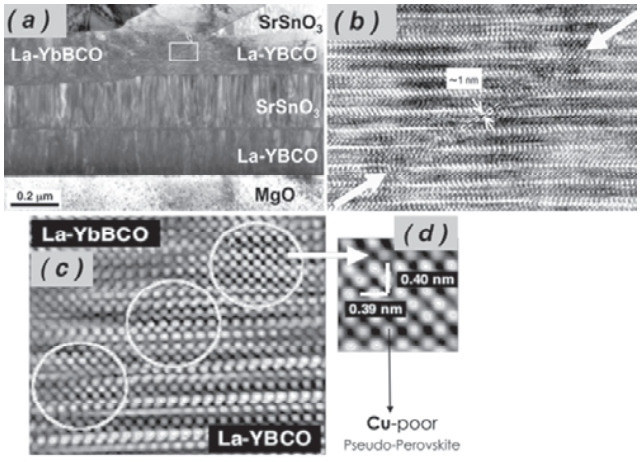

Fig. 4 TEM images of the barrier region of ramp-edge JJ prepared by the IMJ method. (a) Low magnified image, (b) high resolution one, (c) Fourier transformed one, and (d) atomic image at the barrier region.

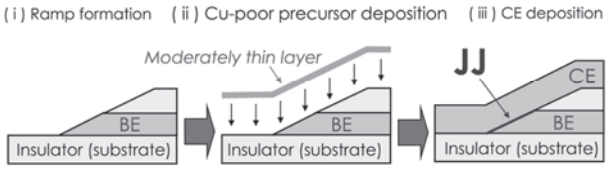

Fig. 5 Schematic illustration of Cu-poor precursor method.

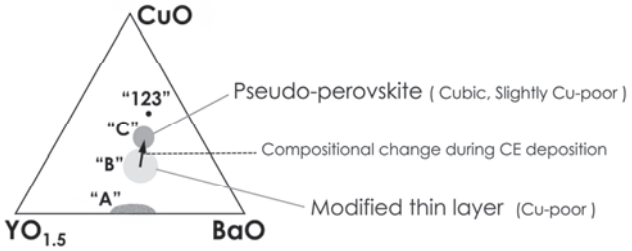

Fig. 6 Compositional changes at the interface or the barrier region of ramp-edge JJ prepared by the Cu-poor precursor method.

electrodes during CE deposition and significant diffusion of Cu took place.

We also investigated the fabrication process of ramp-edge type JJs for HTS-SFQ circuits [31]. Schematic illustration of cross-sectional view of an HTS-SFQ circuit is drawn in Fig. 3. The thickest portion consists of five oxide layers with a total thickness of more than 1 μm. We used $Y_{0.9}Ba_{1.9}La_{0.2}Cu_3O_y$ (La-YBCO) for the BE and ground plane layers, and $Yb_{0.9}Ba_{1.9}La_{0.2}Cu_3O_y$ (La-YbBCO) for the CE. $SrSnO_3$ (SSO) was used for insulating layers. The oxide films except La-YbBCO were deposited by off-axis magnetron sputtering. The CE layer was prepared by pulsed laser deposition (PLD). Junction barriers were prepared by using the IMJ method.

We investigated the obtained barrier in terms of structure and composition [32]. TEM images of the junction interface are shown in Fig. 4. A low magnified image (Fig. 4(a)) indicates that an oxide multilayer structure with sharp interfaces is successfully constructed. A successive line with a different crystal symmetry and a thickness of approximately 1 nm, which is indicated by arrows, can be seen at the interface between BE and CE in a high resolution image of Fig. 4(b). In both images, no appreciable segregated phase is found. A Fourier transformed image and the enlarged one of the barrier region are shown in Figs. 4(c) and 4(d), respectively. In the barrier region, the ordered structure along the c-axis of triple perovskite disappears and a cubic-like unit with lattice parameters of $0.39 \times 0.40\,\mathrm{nm}^2$ is seen. EDX analysis revealed that the atomic ratio of Cu/(other cations) was less than unity, suggesting Cu and some other cations occupy the atomic site for small cation of the perovskite oxide. We speculated that small Yb ions enter the site [10]. The EDX analysis also revealed that the barrier region had a slightly La-rich composition comparing with those of electrodes, implying that La ions stabilized a cubic-like perovskite phase at the barrier.

It was likely that significant Cu diffusion from electrodes to the barrier region took place during CE deposition, because the applied technique was similar to Satoh et al.'s [29]. It seems possible that such significant change in composition may promote impurity segregation, although the appreciable precipitate is not observed in our samples of Fig. 4 fortunately. To reduce such possibility, we have developed a new method for JJ preparation [33], namely Cu-poor precursory method, as illustrated in Fig. 5. Between the ramp formation and CE deposition, a deposition step for a Yb-Ba-La-Cu-O thin layer with a thickness of a few nm is inserted. The same target was used for the following CE deposition. To obtain a Cu-poor composition, PLD condition was altered from that for the CE. In this method, the composition at the ramp surface is artificially controlled, as described in Fig. 6.

Before deposition of the Cu-poor thin layer, the composition at the ramp surface seemed to be significantly Cu-poor by preferential sputtering of Cu during ion milling [30]. That region is indicated by "A" in Fig. 6. Then, the Cu-poor precursory layer having a composition indicated by "B" is deposited. During the sequential CE deposition, the composition at the interface gradually changes to the region "C" by Cu diffusion form electrodes. This thin layer with the composition "C" is expected to be a junction barrier. It is expected that moderately Cu-poor composition of "C" can

Table 1 Successful operations of HTS-SFQ devices at SRL-ISTEC.

Circuit	Number of JJs	Temperature
Confluence buff.	23	< 61 K
RS-FF	20	< 69 K
T-FF	26	< 62 K
Inverter	24	< 45 K
1:2 switch	37	< 60 K
OR	34	< 50 K
AND	33	< 71 K
100 JJ-JTL	101	< 38 K
1:2 DEMUX	50	< 20 K

suppress local segregation of impurity phase at a barrier region, since no significant Cu diffusion is required to form the barrier with the composition "C". Formation of a clear barrier having sharp interfaces between electrodes was also expected. Enhancement in I_cR_n values was actually observed for JJs prepared in this method [33].

4. HTS-SFQ Circuits

We had fabricated elementary HTS-SFQ circuits using the multilayer structure as schematically shown in Fig. 3. The fabrication technology for many JJs with homogeneous characteristics in a chip is required. A small spread of sigma = 7.3% in I_c's for 1000 JJs was reported by our group [34]. We found that the JJ properties are affected by local layout design around individual JJ, and devised a method to overcome the problem, namely a "separated base layout (SBL)" method [35]. Our activities on HTS-SFQ were previously reported in this journal [11]. Here, HTS-SFQ circuits in which successful logic operation was demonstrated by our group are listed in Table 1.

5. HTS-SQUIDs

5.1 Fabrication of Gradiometers and Magnetometers

We have fabricated HTS-SQUIDs by applying the above-mentioned process developed for HTS-SFQ. Our fabrication process was previously described [36]. In the process, some modifications have been made in thin film materials for HTS-SQUIDs. La-YBCO ground plane was replaced by non-superconducting $Pr_{1.4}Ba_{1.6}Cu_{2.6}Ga_{0.4}O_y$ (P4G4) [37]. It is expected that this black-colored P4G4 works as a temperature homogenizer during deposition of the upper layers. $SmBa_2Cu_3O_y$ (SmBCO) and $Er_{0.95}La_{0.1}Ba_{1.95}Cu_3O_y$ (L1ErBCO) are used for the BE and CE, respectively. A cross-sectional view of our HTS-SQUID taken by a scanning electron microscope (SEM) is shown in Fig. 7. A thin buffer layer of $BaZrO_3$ (BZO) was inserted between MgO substrate and P4G4 to improve the quality of P4G4. The surface of BE was covered by a thin SSO layer, called 1st SSO. This works as a protective layer for BE during the patterning

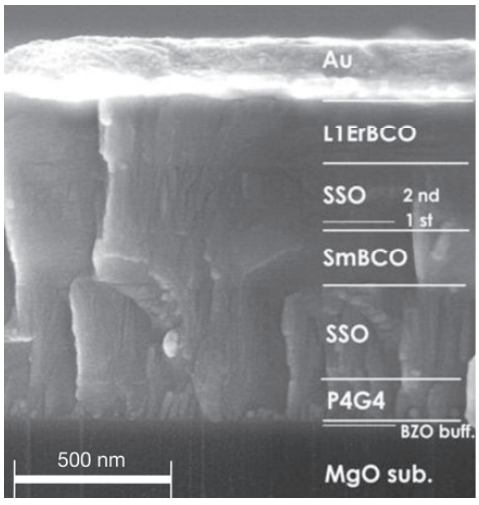

Fig. 7 An SEM photo of cross-sectional view of multilayer for HTS-SQUID.

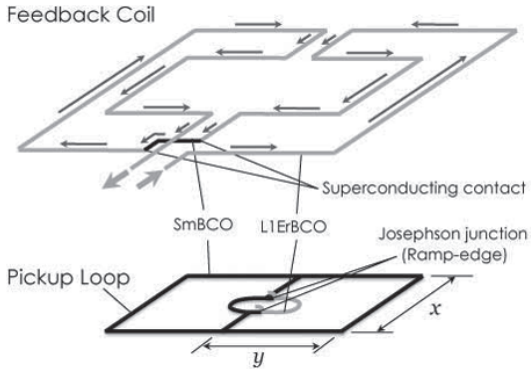

Fig. 8 Schematic illustration of HTS-SQUID gradiometer with integrated feedback coil.

procedure by photolithography and ion-milling. Sharp interfaces and no columnar growth suggest that oxide multilayer structure was successfully constructed.

We fabricated directly-coupled HTS-SQUID gradiometers. Figure 8 is a schematic illustration of the gradiometer. A feedback coil was integrated on the pickup loop using the multilayer technology. Gradiometers with different sizes ($x \times y$) of the pickup loop were fabricated. Typical inductance of a SQUID inductor and JJ width were 40~60 pH and 2~3 μm, respectively. For instance, an optical micrograph (OM) image for a gradiometer with ($x \times y$ = (0.5 × 1.0) in mm is shown in Fig. 9.

Figure 10 shows typical properties measured at 77 K for a gradiometer with a size of (1.0 × 1.0) in mm. $2I_c$ and $R_n/2$ were measured to be approximately 12 μA and 7.8 Ω, respectively. Relatively large I_cR_n product of 93 μV was observed. Assuming the occurrence of thermal noise rounding in the I-V curve shape, the actual I_c value might be approximately 20 μA. Then, I_cR_n product is estimated to be 156 μV. Peak-to-peak modulation voltage V_{mod} of 60 μV was obtained. This gradiometer showed a rather low flux noise

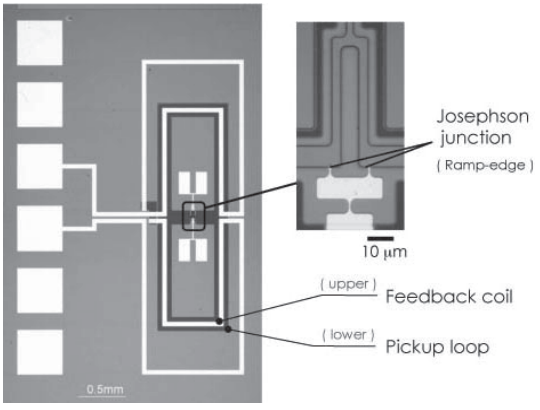

Fig. 9 OM images of a gradiometer with $(x \times y) = (0.5 \times 1.0)$ in mm.

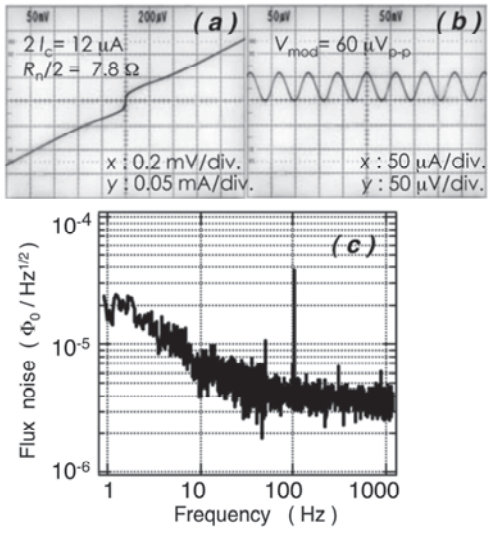

Fig. 10 Properties of an HTS-SQUID gradiometer with $(x \times y) = (1.0 \times 1.0)$ in mm. (a) I-V, (b) V-Φ curves and (c) flux noise measured in AC bias mode at 77 K.

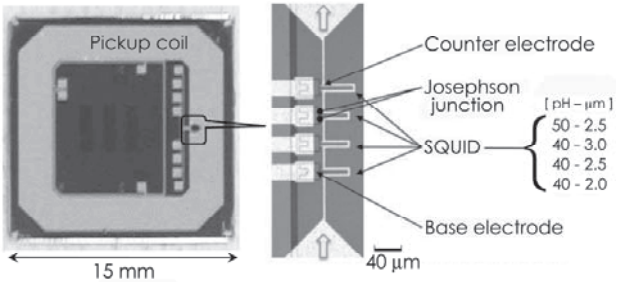

Fig. 11 A directly-coupled HTS-SQUID magnetometer.

evaluated in AC bias mode of $3.8\,\mu\Phi_0/\mathrm{Hz}^{1/2}$ in the white noise region. The $1/f$ corner was about several tens Hz for this gradiometer.

We fabricated two types of HTS-SQUID magnetometers on MgO substrate with a size of $15 \times 15\,\mathrm{mm}^2$ [38]. These are directly coupled and inductively coupled ones. Figure 11 shows a photo of a directly-coupled magnetometer chip and an optical micrograph (OM) image of SQUID inductors. This layout has 4 SQUIDs with different designs in JJ width (W_{JJ}) and inductance (L_S) in order to improve production yield of the chip. We can choose a SQUID suitable to particular application. The obtained result of field noise measurement in AC bias mode at 77 K for a chip is shown in Fig. 12. A SQUID inductor with $L_S = 40\,\mathrm{pH}$ and $W_{JJ} = 2.0\,\mu\mathrm{m}$ was used. The effective area (A_{eff}) was $0.3\,\mathrm{mm}^2$. Quite low noise characteristics were observed. A white noise level was measured to be $30\,\mathrm{fT/Hz}^{1/2}$. With decreasing frequency, the noise increases appreciably below a few tens Hz. However, the chip exhibits a rather low noise of $200\,\mathrm{fT/Hz}^{1/2}$ even at 1 Hz.

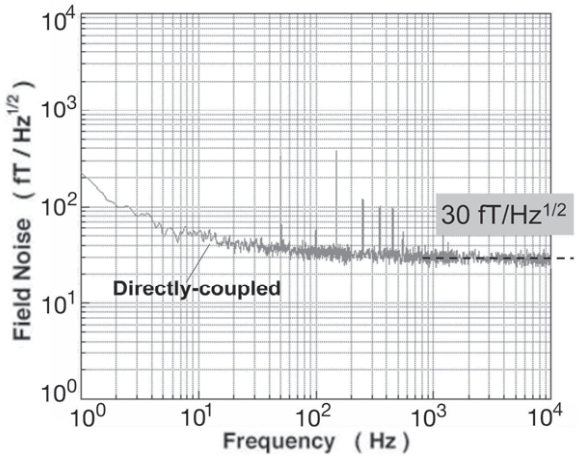

Fig. 12 Field noise characteristics for a directly-coupled HTS-SQUID magnetometer. Data were collected in AC bias mode at 77 K.

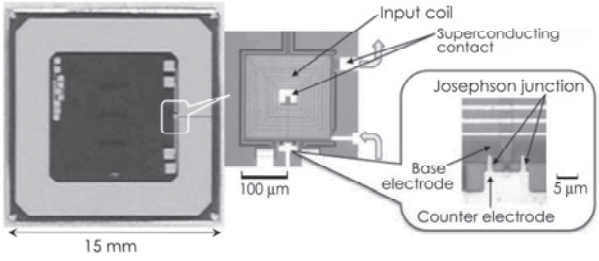

Fig. 13 An inductively-coupled HTS-SQUID magnetometer.

Figure 13 shows a photo of an inductively-coupled magnetometer chip and OM images around SQUIDs [38]. That is so-called Ketchen-type. Design of the pickup coil is almost identical with that of the abovementioned directly-coupled one. A 20-turn input coil was prepared on a washer with a size of $200 \times 200\,\mu\mathrm{m}^2$. Both widths of the line and the space for the input coil are $2\,\mu$m. W_{JJ} and L_S are $2\,\mu$m and 30 pH, respectively. A_{eff} was $2.0\,\mathrm{mm}^2$. Field noise spectrum taken in AC bias mode at 77 K is shown in Fig. 14. Noise level lower than the directly-coupled magnetometer was recorded above 200 Hz. White noise level was measured to be $10\,\mathrm{fT/Hz}^{1/2}$. However, the noise increases appreciably below 400 Hz with decreasing frequency. Presently the origin is not clear.

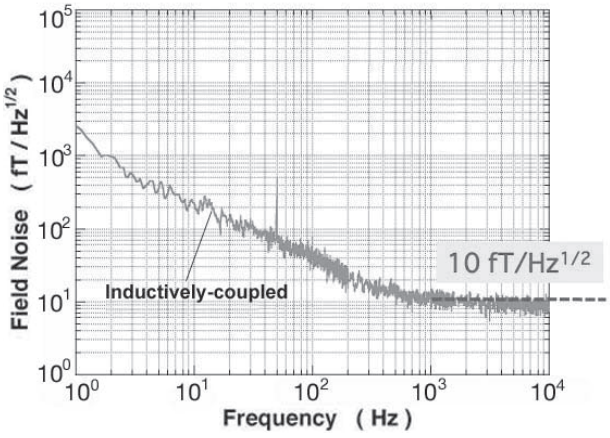

Fig. 14 Field noise characteristics for an inductively-coupled HTS-SQUID magnetometer. Data were collected in AC bias mode at 77 K.

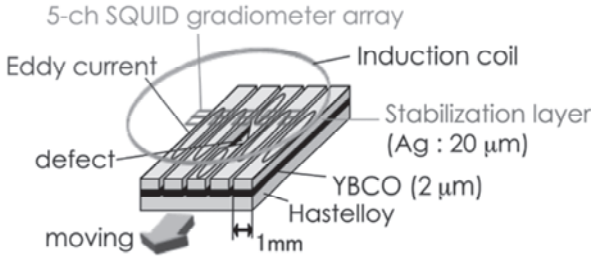

Fig. 15 Principle of the NDE system for striated CCs with five filaments using a 5-ch HTS-SQUID gradiometer array.

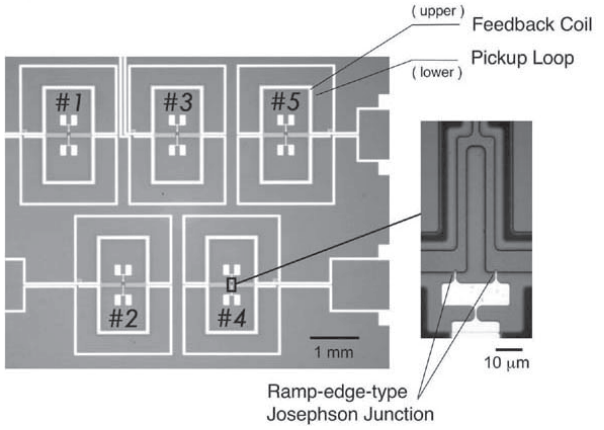

Fig. 16 OM photos of 5-ch HTS-SQUID gradiometer array.

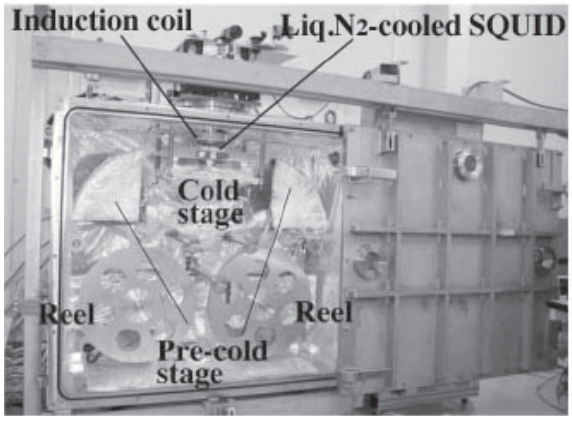

Fig. 17 Photograph of the RTR-NDE system for striated CC using HTS-SQUID gradiometer array.

5.2 Non-Destructive Evaluation (NDE) System for Striated HTS Coated Conductors (CC)

Recently, the research and development for HTS-CC have been intensively carried out. Successful fabrication of several-hundred-meter long CCs with high critical currents over a few hundreds amperes has been achieved [39]. Striating techniques of the CCs have been also developed for application to AC power devices such as transformers and motors [40]. However, there was no NDE system that enabled us to examine striated CCs in reasonably high resolution, high sensitivity and high speed. We proposed a new NDE system using HTS-SQUIDs [41].

In the system, an HTS-SQUID gradiometer array was used. Eddy currents are induced in superconducting layer of CCs by using an induction coil, and the variation of magnetic field gradient generated by the eddy currents is monitored by the gradiometers. Figure 15 is an illustration describing the principle of our NDE system. We fabricated the system for 5-mm-wide CCs divided to 5 filaments, and consequently the width of each filament was nealy 1 mm. OM images of the array are shown in Fig. 16. Each gradiometer has a design of the abovementioned (1.0×1.0)-gradiometer shown in Fig. 8 [42]. To reduce effects of cross-talk between adjacent feedback coils, five gradiometers were arranged in two lines forming a "W" character.

Figure 17 shows the whole NDE system for reel-to-reel (RTR) examination of striated HTS-CCs. In a vacuum chamber, a cooling system for CC is installed. CC under the gradiometer array is cooled below T_c by thermal conduction to a cold stage and pre-cold stages. To achieve sufficient contact between CC and the stage, a back tension of 2 N/m was applied to CC by controlling torque power of reel shafts. After some additional improvement in the system, we succeeded in achieving the maximum testing speed of 80 m/h.

An example of test results is shown in Fig. 18. The upper image in the figure was taken by a scanning laser microscope. It enables us to examine the height of the sample. The bright area suggested the occurrence of delamination in Lanes 1 and 5. The lower two graphs shows the SQUID signals for Lanes 1 and 5. Anomalies in the signals at positions corresponding to the bright portions in the laser microscope image are seen. It suggested that delamination in the filaments was detected by the SQUID-NDE system. We confirmed that the system could detect other types of defects such as shorts between adjacent filaments, regions with significantly reduced critical current and so on. This system is very convenient to check striated HTS-CCs before utilizing

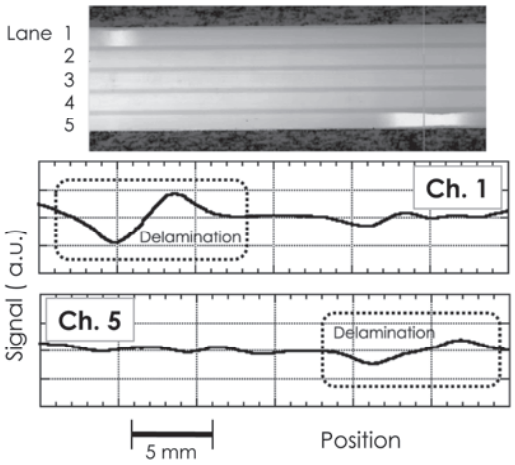

Fig. 18 An example of NDE test results for a striated HTS-CC. The upper image was taken by a scanning laser microscope. The lower two graphs are signals for the gradiometers of channels 1 and 5, positioned above Lanes 1 and 5, respectively.

them for fabrication of various power devices. Moreover, it is also useful to check CCs before the striation process. The system can detect inhomogeneity in superconducting properties such as some precipitates and scratches introduced by handling mistakes and so on. We can thus choose CCs appropriate to execute striation procedure.

5.3 Non-Destructive Evaluation (NDE) System for Deep-Lying Defects

NDE using SQUIDs has advantages over conventional NDE techniques. Since SQUID has high sensitivity even at low frequencies which enable penetration of eddy current into deep regions of a conducting sample, weak magnetic signals generated from deep regions can be detected, even when the sample is covered with some materials. We fabricated a 2-axis planar-type HTS-SQUID gradiometer chip-shown in Fig. 19 [43], [44]. Two gradiometers having a baseline of 8.5 mm were orthogonally prepared on a chip. (see Fig. 19(a)). Figure 19(b) is a layout design of the center area. Superconducting cross-over wiring and superconducting contacts between BE and CE were prepared. Each gradiometer has four SQUID inductors with W_{JJ} = 2.0–3.0 μm. We can choose suitable one among them.

We constructed an NDE system consisting of a liquid-nitrogen cryostat, a double-D type induction coil, an X-Y stage and electronic equipments including flux-locked loop (FLL) circuits. Figure 20(a) is a photographic view of the cryostat and induction coil. There is a sapphire window at the bottom of the cryostat. Inside the window, the gradiometer is located in an evacuated space. We examined an aluminum plate having a slit hole as a defect. Measurement of the distribution of magnetic signals from the plate was carried out. The configuration of the gradiometer and the sample in the present experiment is illustrated in Fig. 20(b). Distorted eddy current around the slit hole is detected. One gradiometer in a chip was used. By inserting aluminum

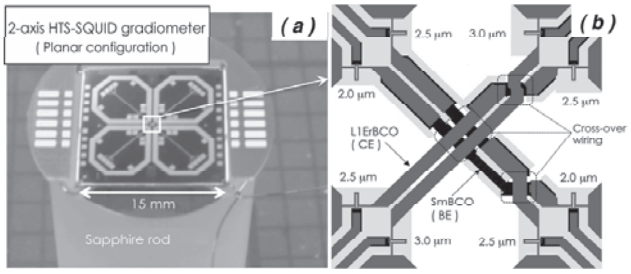

Fig. 19 2-axis planar-type HTS-SQUID gradiometer chip. (a) Photographic view of a chip mounted on a sapphire rod, and (b) the layout design of center area of the chip.

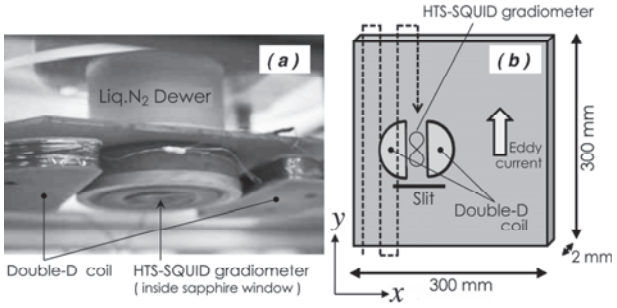

Fig. 20 (a) Photographic view of the cryostat and double-D type induction coil. Inside the window, the gradiometer was set in an evacuated space. (b) Schematic illustration of configuration of the gradiometer and the sample in the present experiment.

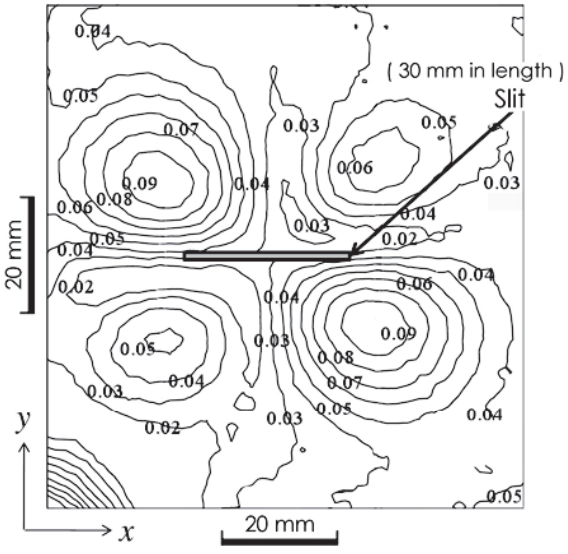

Fig. 21 Contour map of the magnitude signal around a slit defect in the sample. 9-layer aluminum plates (total thickness of 18 mm) without a slit was inserted between the sample and the cryostat. The position of the deep-lying slit is indicated. Numbers in the map are signal intensities in arbitrary unit.

plates without a slit between the sample and the cryostat, the distance between the gradiometer and the slit or the slit depth was changed.

Figure 21 shows an example of the obtained results. A 2-mm thick aluminum plate having a 30 mm long slit

was examined. 9-layer aluminum plates (total thickness of 18 mm) without a slit were inserted between the sample and the cryostat. This contour map of signals is correspondent to the slit in the bottom aluminum plate. This clearly indicates that our NDE system successfully detected the slit existing at 20 mm deep position, even though 9-layer aluminum plate was inserted. It was estimated that our system possibly could detect the slit at 50 mm deep position [44].

6. Conclusion

Various types of JJs using HTSs were briefly explained. Bicrystal junction and step-edge one have been widely used. Ramp-edge junctions enable us to realize devices having relatively complicated layout designs. We have studied the fabrication process of the ramp-edge JJs, and fabricated HTS-SFQ circuits and HTS-SQUIDs. We have developed a method to prepare JJ barriers reproducibly, namely "Cu-poor precursor" method. In this method, an appropriate JJ barrier is obtained by re-crystallization of the artificially deposited Cu-poor precursory layer. It is speculated that composition of the precursory layer, being Cu-poor and containing small rare earth elements, is important. Recently, we fabricated NDE systems using HTS-SQUIDs with ramp-edge JJs and multilayer structures. By using a 5 ch HTS-SQUID gradiometer array, a RTR testing system for striated HTS-CCs was developed. It has been actually utilized for research & development of HTS power devices. We also fabricated a chip of 2-axis planar-type HTS-SQUID gradiometer having a rather long baseline of 8.5 mm. An NDE system with this chip was fabricated to search for deep-lying defects in a metallic plate.

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