FOREWORD

Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology

By virtue of the continuing advancement in CMOS device scaling, the number of transistors on a VLSI chip has been ever-increasing. It is reaching the level of 10 giga-transistors on a single chip, the equivalent of the total number of neurons in the human brain, which seems certain to provide great opportunities for the development of new applications and information processing.

Continuing current trends of device scaling dictate that several issues be solved: device leakage, process variation, performance degradation by aging, low noise-tolerance, neutron-induced soft-errors, high fabrication costs, high design costs, and others. To resolve those issues, R&D efforts must be made in each layer of architecture, circuit, device, and design methodology, in addition to extensive cooperative research among those four technical layers.

This Special Section presents outstanding results of original research related to the subjects described above. The section includes 2 invited papers, 31 regular papers, and 3 brief papers, which were selected from a lot of submitted papers through careful review process. Technical papers published here are classified as follows: VLSI architecture (10), digital circuits (3), memory (8), analog circuits (8), sensors (2), design methodology (3), and device technology (2).

The Guest Editor-in-Chief expresses his sincere appreciation to all authors for their contributions and to all reviewers for their critical readings. He also thanks the Editorial Committee for their work on this special section.

Masahiko Yoshimoto, Guest Editor-in-Chief

Masahiko Yoshimoto *(Senior Member)* joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in 1977. From 1978 to 1983 he had been engaged in the design of NMOS and CMOS static RAM. Since 1984 he had been involved in the research and development of multimedia ULSI systems. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. Since 2000, he had been a professor of Dept. of Electrical & Electronic System Engineering in Kanazawa University, Japan. Since 2004, he has been a professor of Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activity is focused on the research and development of an ultra low power multimedia and ubiquitous media VLSI systems and a dependable SRAM circuit. He holds on 70 registered patents. He has served on the program committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. Also he served as Guest Editor for special issues on Low-Power System LSI, IP and Related Technologies of IEICE Transactions in 2004. He was a chair of IEEE SSCS (Solid State Circuits Society) Kansai Chapter from 2009 to 2010. He is also a chair of The IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011–2012. He received the R&D100 awards from the R&D magazine for the development of the DISP and the development of the realtime MPEG2 video encoder chipset in 1990 and 1996, respectively. He also received 21st TELECOM System Technology Award in 2006.