INVITED PAPER *Special Section on Solid-State Circuit Design — Architecture, Circuit, Device and Design Methodology*

Digital Calibration and Correction Methods for CMOS Analog-to-Digital Converters

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SUMMARY Along with the miniaturization of CMOS-LSIs, control methods for LSIs have been extensively developed. The most predominant method is to digitize observed values as early as possible and to use digital control. Thus, many types of analog-to-digital converters (ADCs) have been developed such as temperature, time, delay, and frequency converters. ADCs are the easiest circuits into which digital correction methods can be introduced because their outputs are digital. Various types of calibration method have been developed, which has markedly improved the figure of merits by alleviating margins for device variations. The above calibration and correction methods not only overcome a circuit's weak points but also give us the chance to develop quite new circuit topologies and systems. In this paper, several digital calibration and correction methods for major analog-to-digital converters are described, such as pipelined ADCs, delta-sigma ADCs, and successive approximation ADCs.

key words: *analog circuits, Moore's law, high performance, system LSIs, miniaturization, digital calibration, correction*

1. Introduction

System LSIs have been developed as essential devices for communication, mechanical control and medical care. Such application fields are still expanding.

The fundamental index of system-LSI technologies is Moore's law [1], which resulted in an amazing revolutionary increase in the integration density of the LSI, becoming hundredfold larger during the past decade. Even the 22 nm CMOS process will be in practical use at an early date.

Now system LSIs are frequently used in sensing systems, which makes them much closer to us. Unlike in previous cases of dealing with video or audio signals, many recent system LSIs digitize analog signals output from sensors, such as temperature, acceleration, and angular velocity, and so on.

In previous CMOS processes such as the 0.25 or 0.5 μm CMOS process, most sensor systems were composed of analog-rich circuits, because a digital cell is too large for complex digital sensors.

However, the situation drastically changed owing to the further development of CMOS processes. This means that we can use more digital circuits than old process to realize sensing systems.

Figure 1 shows such a situation, which shows the number of digital transistors equivalent to the energy consumption of an ADC. These graphs are based on typical 2006 ADC energy per conversion number. It is clear that the number drastically increases as CMOS processes are miniaturized.

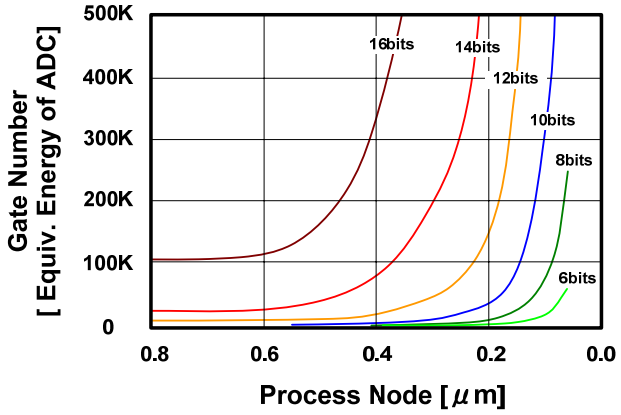

Fig. 1 Number of transistor gates equivalent to power consumption of ADC [2].

Therefore, in the present system LSIs, it is mainstream to digitize analog signals as early as possible, which allows us to use more advanced signal processing including nonlinear processes using huge resources of digital gates. This approach encourages the development of various types of analog-to-digital converter collaborating with digital calibrations and corrections. Finally, the performance of ADCs is markedly improved as compared with the performance several years ago.

In this paper, main techniques for calibrating or correcting ADCs are described. "Calibration" means a method of maximizing the performance and "Correction" means a method of one-to-one conversion for correct output codes. In Sect. 2, recent major types of ADC are introduced. In Sects. 3 to 7, calibration techniques for such ADCs are shown.

2. Circuit Configurations of Recent ADCs

2.1 Classification

Figure 2 shows the classification of ADC configurations. There are four main configurations of ADCs: oversampling, pipeline, successive approximation, and flash ADCs. Each configuration of ADC has a specific digital calibration technique.

Manuscript received August 31, 2011.
Manuscript revised October 21, 2011.

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DOI: 10.1587/transele.E95.C.421

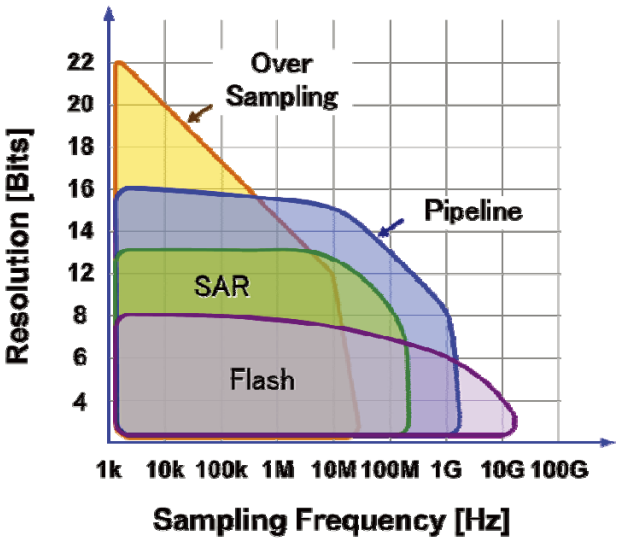


Fig. 2 Classification of ADC configurations.

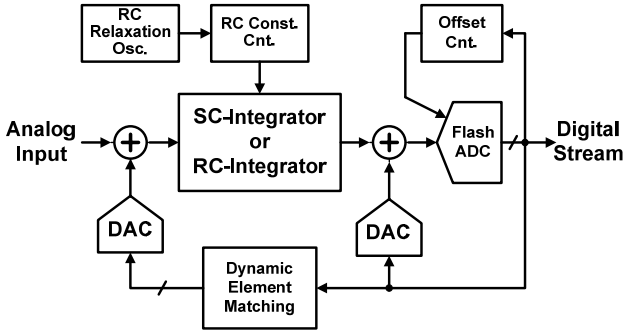


Fig. 3 Block diagram of oversampling ADC.

2.2 Oversampling ADCs

Figure 3 shows a block diagram of an oversampling ADC whose architecture is suitable for ADCs with a higher dynamic range and a lower bandwidth less than 20 MHz [3]–[5].

Those ADCs are a type of filter system for quantization noise using a feedback loop. As shown in Fig. 3, the effect of the integrator pushes the quantization noise up to the high-frequency region so that the SNR in the low-frequency region becomes very high.

There are two means of realizing the integrator: one is to use a switched capacitor circuit and the other is to use a continuous time integrator. ADCs with the switched-capacitor (SC) integrator show stable operation and ease of changing the signal bandwidth at the cost of large power dissipation. In contrast, ADCs with the continuous-time (CT) integrator realize a higher bandwidth with a lower power dissipation. However, they are beset with a loop stability problem. In addition it is difficult for CT integrators to adjust the signal bandwidth because the bandwidth depends on the absolute value of the RC constant.

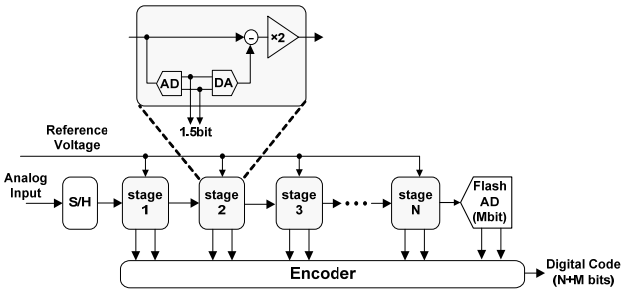


Fig. 4 Block diagram of pipelined ADC.

In addition, it is essential for CT modulators to calibrate the offset mismatch in flash ADCs and the current mismatch of each cell in the DAC for maximizing its signal to noise ratio.

2.3 Pipeline ADCs

Figure 4 shows a block diagram of the pipelined ADC consisting of cascaded pipe stages [6]. The pipe stage is a switched capacitor circuit with a low-resolution ADC.

The function of the pipe stage is to subtract a constant analog value from the input signal and to output the digital code corresponding to the value to be subtracted.

In actual implementation, the output residue of the pipe stage is amplified so that the dynamic ranges of all pipe stages are equal. It is the largest advantage of the pipeline ADC to introduce redundancy very easily, which makes the ADC insensitive to the offset of the comparator.

Thus, it is relatively easy to achieve ADCs with a resolution higher than 12 bits using the above architecture. In addition, pipelined ADCs are suitable for high-speed operation owing to the simplicity of each of the pipe stages [7]. Another important characteristic of this ADC is that the later the pipe stage is, the closer it is to the ideal operation of the pipe stage. This means that we can use later pipe stages for calibrating the earlier pipe stages that are more sensitive to the parasitic and mismatch of transistors.

Therefore, various calibration methods have been developed to date [8].

2.4 SAR-Type ADCs

Figure 5 shows a block diagram of the successive approximation register (SAR) type ADC [9]. The architecture is very simple because the SAR requires no opamp, but only switches, capacitors and comparators. Thus, the SAR-type ADC is compatible with deep submicron CMOS processes.

First, an input voltage signal is stored in the plate on the comparator side of the capacitor array that is binary-weighted. Next, the binary search is conducted so that quantized voltage is applied to the opposite side of the capacitor array.

This type of ADC was invented in the early days of CMOS technologies. The architecture of the SAR has not changed for about 30 years. However, drastic improvement

has been carried out in recent years, because it has the potential to realize the lowest FOM among ADCs as long as the resolution of the ADC is less than 10 bits [10].

Multiple approaches to reducing the area of the capacitor array, to operating asynchronously for high-speed operation and to calibrating the mismatch of the capacitor array have been developed [11]. In a very recent paper, a 10 bit SAR with an FOM of 15.5 fJ/conv.-step in 100 MHz operation has been reported [12].

2.5 Flash ADCs

Figure 6 shows a block diagram of the flash ADC. The architecture is the most basic, which outputs the thermometer code using comparators whose number is equal to the quantization levels of the ADC.

The flash ADC has the highest operating speed because it requires no sample hold circuit. Sometimes, the input transistors of the comparator use the minimum gate length to enhance operating speed. Thus, an offset calibration scheme is required [13]. In addition, trimming schemes for both clock timing and frequency characteristics of each comparator are also essential.

Aside from the ADC mentioned above, other architectures exist: a dual-slope-type ADC for measurement hardware, a subranging ADC and an interpolated ADC [14]. However, the digital calibration schemes for the above ADCs are based on those for the four fundamental types of ADC. Here, we will not discuss the other types of ADC individually.

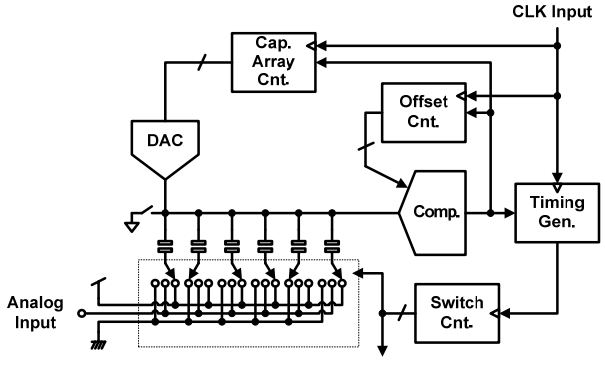


Fig. 5 Block diagram of successive approximation register.

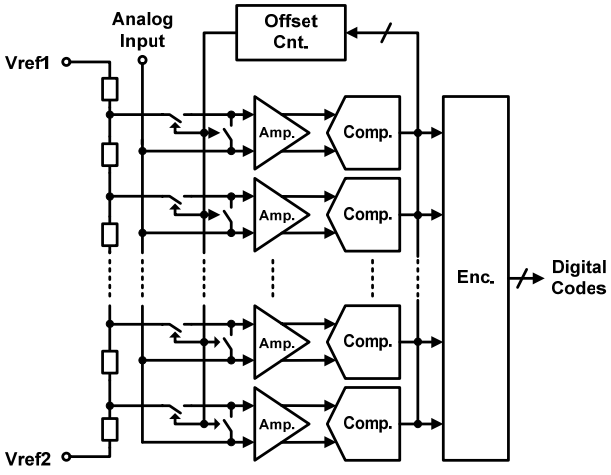


Fig. 6 Block diagram of flash ADC.

3. Digital Calibration Scheme for ADCs

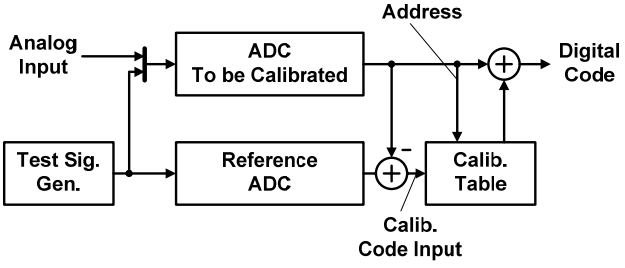
Figure 7 shows the fundamental calibration schemes for ADCs [15]. Figure 7(a) shows the oldest and the most general calibrating way. The system has two ADCs: an ADC to be calibrated and a high-accuracy and low-sampling-rate ADC for use as a reference. The same test signals are input into both ADCs and the differences between those outputs are stored in a table for calibration.

Although this method is applicable to most ADCs, the area of additional circuits becomes very large. Thus, it is a rare case to apply the method to practical use as it is.

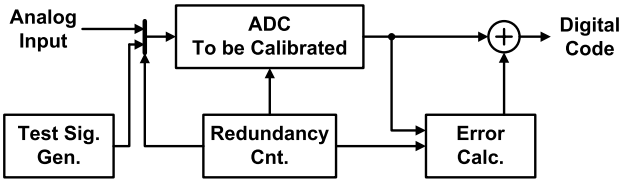
Moreover, the error becomes larger when the frequency of the input signal becomes higher because the table is based on the data from the reference ADC with a low sampling rate.

A more efficient method is shown in Fig. 7(b), which uses an ADC with redundancy to generate calibration codes. In general, an ADC with redundancy can generate two output codes of the ADC by switching the circuit configuration. In an ideal case, the difference between the two codes should be zero. If the difference is not zero, it means that there is an error. Thus, the error can be used to calibrate the output code of the ADC.

The later method is the typical correction method for pipeline ADCs. Figure 7(b) shows a control block for changing the operation mode of the redundant path in an ADC. The table for calibration stores each error of the out-



(a) Using High-Resolution and Lower-Sampling-Rate ADC



(b) Using Redundancy of ADC

Fig. 7 Fundamental calibration schemes for ADCs.

put codes corresponding to the switching modes of the redundant block of the ADC. The details of the calibration method of the pipeline ADC will be discussed later.

The increase in system size shown in Fig. 7(b) is much smaller than that shown in Fig. 7(a), because the correction table only stores errors whose number is equal to the number of the combination of redundant paths in the ADC.

However, note that we can use this method to calibrate the DNL only, because the method compensates for the continuity of the output codes. It should depend on the other means to calibrate global characteristics such as INL.

4. Digital Calibration Methods for Pipelined ADCs

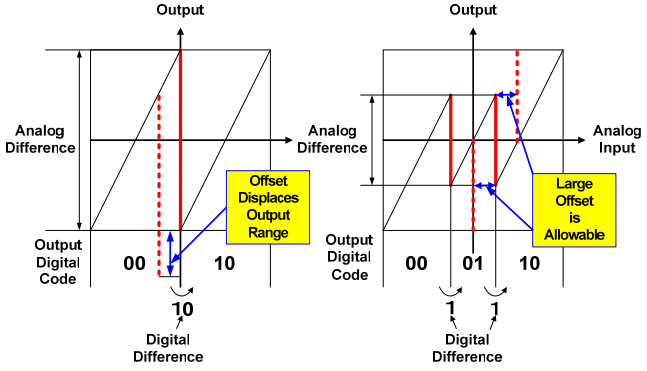
In this section, we describe three major calibration methods: DNL error calibration, calibration of the DNL in the background, and calibration of the memory effect arising when we use a double-sampling architecture.

4.1 DNL Calibration Method

One of the distinguishing characteristics of the pipeline ADC is that we can calibrate earlier pipe stages using the output code from later pipe stages because the later the pipe stage is, the more the gain of the pipe stage relaxes the required performance of itself. Figures 8(a) and 8(b) show the input-output characteristics of the 1- and 1.5-bit pipe stages, respectively.

Provided that the comparator has an offset voltage at its input, the output of the 1-bit pipe stage is outside of the dynamic range, which makes it impossible to estimate the input value from the output code of the pipe stages connected after the stage for calibration. On the other hand, the 1.5-bit pipe stage tolerates a much larger offset of the comparator. As long as the input offset is less than one-fourth of the input range, the output voltage is within the dynamic range [16].

In the pipeline ADC, each pipe stage subtracts the analog value, and the residue is amplified and sent to the successive pipe-stage. Each stage outputs a digital code corresponding to the analog value subtracted at the pipe stage.



(a) 1-bit stage (b) 1.5-bit stage

Fig. 8 Input-output characteristics of pipe stage.

Thus, the most important thing is to find an accurate digital code corresponding to the actually subtracted analog value. That is to say, the question is how to determine the digital code. In Fig. 8(b), output digital codes corresponding to the operation modes of the pipe stage are shown along the x-axis. The subtracted analog values are the output differences between the operation modes that are discontinuous changes at boundaries of the operation modes [thick line in Fig.(9)].

In an ideal case, the analog subtraction is half of the output range that is equal to the difference between the output digital codes, which is 1 in this case (00→01 or 01→10).

However, the nonideality of the pipe stage, such as the capacitance mismatch of the switched capacitor circuits or the finite gain of the amplifier breaks the assumption. Thus, we have to measure real digital codes corresponding to the subtracted analog values.

Figure 9 shows the method for determining the digital code corresponding to the subtracted analog value. First, the input test signal is set to one-fourth of the input range, which is close to the boundary of the operation mode. Next, the DAC in the pipe stage is forced to be modes ① and ② successively and each output code is measured in the following pipe stages.

If the characteristics of the following pipe stages are ideal, the difference between digital codes ① and ② is the real digital value corresponding to the subtracted analog value [17]. Fortunately, this assumption works well, because the later the pipe stage is, the more its nonidealities are suppressed by the gain of the stage.

Thus, we have to start the calibration at the most subsequent stage needed for calibration. When the calibration at the stage is finished, the stage seems to operate ideally.

Next, the calibration moves to the previous stage, and the calibration continues until the first pipe stage is calibrated.

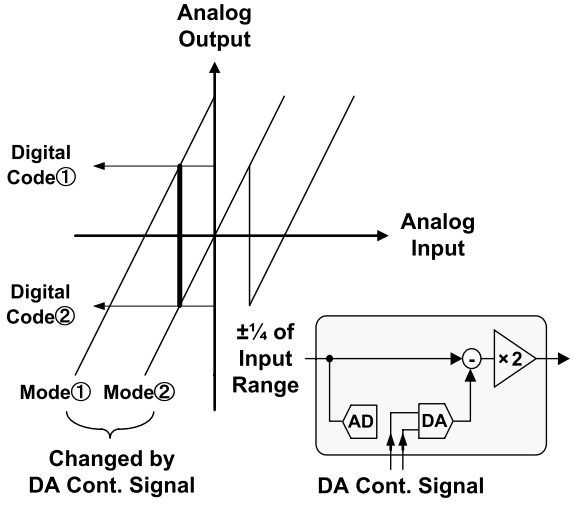


Fig. 9 Measurement method of determining digital code corresponding to subtracted analog value.

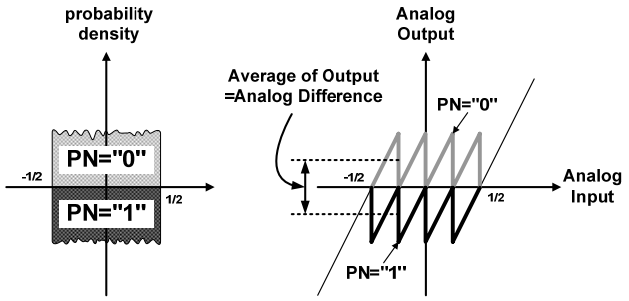


Fig. 10 Background calibration.

4.2 Calibration in Background

The calibration method mentioned in Sect. 4.1 requires a certain period to perform, which means that the A-to-D conversion has to be stopped in the period. Thus, several ways of calibration along with the A-to-D conversion have been developed in recent years.

These calibration methods are called "Background Calibration". A typical background calibration uses both redundancy and pseudo-random (PN) codes.

An outline of the background calibration is shown in Fig. 10 [18]. The input-output characteristics of the pipe-stage are slightly different from those in Fig. 8(b), which has two types of characteristic: one corresponds to the PN=0 (faint line) and the other corresponds to the PN=1 (black line). The probabilities of the pipe stages choosing each conversion characteristic converge to 50% after a sufficient period. Provided that the probability density distribution of the input signal is flat, the difference between two averages of the digital output for each conversion characteristic expresses the subtracted analog value. Thus, we can calibrate the pipe stage in the background.

4.3 Memory Effect Calibration in Double Sampling Pipeline ADC (DSPADC)

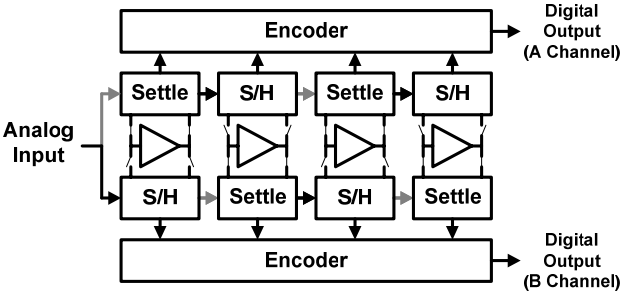
DSPADC is an interesting circuit configuration that realizes high-speed and efficient operation. Figure 11 shows the block diagram and operation of the DSPADC.

The DSPADC includes two pipeline ADCs whose opamps are shared [19]. Thus, as shown in Fig. 11(b), one is in the sample hold operation and the other is in the settling operation. Only the settling operation requires an opamp. Thus, an opamp can be shared by interleaving.

However, there is no period for resetting capacitors during the operation, resulting in the memory effect problem. Here, the memory effect means that the residual charge in the settling period causes an error in the next settling period of the opposite pipe stage.

The effect becomes larger at a higher sampling speed, because DC gain tends to be lower in such a case.

The actual residual charge can be derived from the relationships shown in Fig. 12. The output voltage of the pipe stage is calculated as follows.



(a) Block Diagram

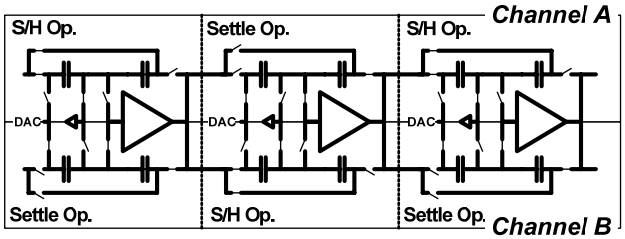
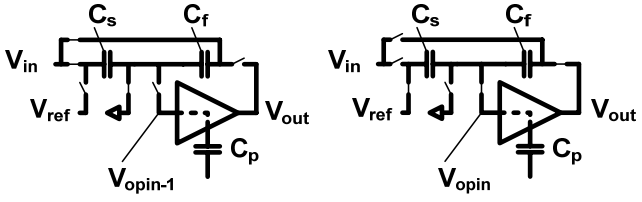


Fig. 11 Block diagram and operation of DSPADC.



(a) S/H Operation (b) Settling Operation

S/H Period	Settling Period	Relational Expression of Charge Conservation
$Q_s=-C_s\cdot V_{in}$	$Q_s'=-C_s\cdot(V_{ref}-V_{opin})$	$Q_s+Q_f+Q_p'_{-1}=Q_s'+Q_f'+Q_p'$
$Q_f=-C_f\cdot V_{in}$	$Q_f'=-C_f\cdot(V_{out}-V_{opin})$	$V_{out}=-A\cdot V_{opin}$
$Q_p'_{-1}=-C_p\cdot V_{opin-1}$	$Q_p'=-C_p\cdot V_{opin}$	$V_{out-1}=-A\cdot V_{opin-1}$

(c) Equations for each operation

Fig. 12 Block diagram and operation of DSPADC.

$$\begin{aligned} Vout &= \alpha\cdot Vin \pm \beta\cdot Vref + \gamma\cdot Vout_{-1} \\ &= \frac{Cs+Cf}{Cf+\frac{Cs+Cf+Cp}{A}}\cdot Vin \pm \frac{Cs}{Cf+\frac{Cs+Cf+Cp}{A}} \\ &\quad \cdot Vref + \frac{Cp}{Cs+(1+A)\cdot Cf+Cp}\cdot Vout_{-1} \end{aligned} \quad (1)$$

In Eq. (1), the α, β and γ are the output gain, the coefficient of the subtracted analog value and the coefficient of the memory effect, respectively. In the DSPADC, there are two sets of β and γ, because it includes two pipeline ADCs. Here, we use the following variables: β_A, β_B, γ_A, and γ_B.

Thus, there are four variables for describing the outputs of the pipe stages. This means that we need four test patterns to derive these variables.

Figure 13 shows the four test patterns for deriving the coefficients of the memory effects. We measure four digital

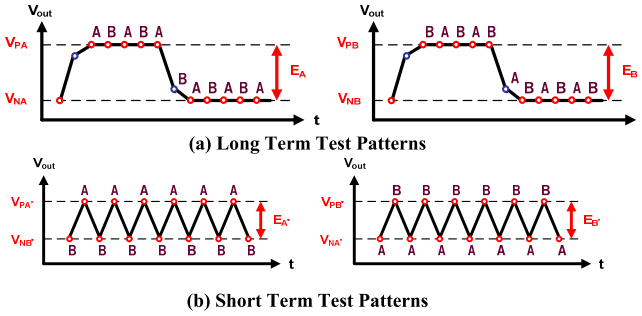


Fig. 13 Test patterns for calculating coefficients of memory effect.

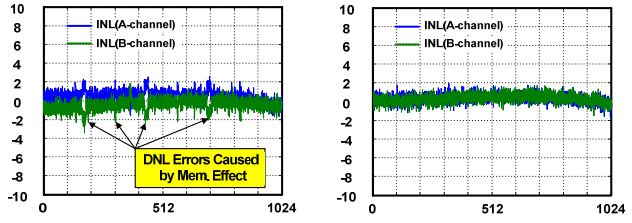


Fig. 14 Measurement result of DSPADC with memory effect calibration.

codes, E_A, $E_{A'}$, E_B and $E_{B'}$, shown in Fig. 13. These variables correspond to the subtracted analog value of the pipe stage.

Finally, the following equations are used to derive the coefficients of the memory effect.

$$\gamma_A = \frac{E_A - E'_A}{E_B + E'_B}, \quad \gamma_B = \frac{E_B - E'_B}{E_A + E'_A} \tag{2}$$

Other variables, β_A and β_B, are derived simultaneously. Instead of measuring the gain of the pipe stage, α, we measure the total gain of the ADC, which is derived by the least-mean-square (LMS) method. Thus, we input four test signals to the ADC. The slope of the output is approximated by the LMS method.

Figure 14 shows the measurement result of the DSPADC with the memory effect calibration. The test chip was fabricated in 40 nm CMOS; it includes a 10-bit DSPADC with an operating speed of 260 MHz. It is obvious that the errors caused by the memory effect shown in Fig. 14(a) disappear after the calibration, as shown in Fig. 14(b). In addition, the difference between the two pipeline ADC is sufficiently close for practical use.

5. Calibration Methods for Delta-Sigma ADCs

Delta-sigma ADCs are an oversampling ADCs which are a type of filter system whose quantization noise is localized in a high-frequency region owing to the filter effect. Thus a low-frequency signal has a very high signal to noise ratio (SNR).

Although delta-sigma ADCs have a potential to realize a high SNR, each block of these ADCs requires a very high linearity that cannot be realized in CMOS processes.

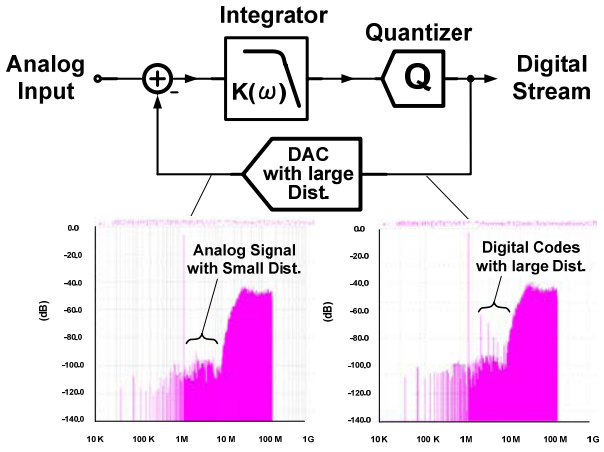


Fig. 15 Simulation results of modulator with large distortion DAC.

Thus, several techniques have been developed to relax the required linearity of each block in delta-sigma ADCs.

In this section, we introduce essential calibration methods for delta-sigma ADCs.

5.1 Dynamic Element Matching

In delta-sigma ADCs, the block most sensitive to linearity of the output codes is the feedback DAC. The delta-sigma modulator is a feedback system, which means that the feedback signal coincides with the input signal at an accuracy of 1/K [K is the DC gain of the K(ω)]. This is effective even if the feedback DAC has a large distortion.

Even if the DAC in Fig. 15 has a large distortion, the analog feedback signal (DAC output) has a small distortion due to the suppression by the large feedback gain. In contrast, the digital codes (Quantizer output) have a large distortion to compensate for the better linearity of the analog feedback signal. Therefore, the DAC linearity is one of the most important factors in achieving sufficient SNDR of the modulator.

The main factor of the nonlinearity of the DAC is the mismatches between current cells in the DAC. The most popular means of alleviating the mismatch in the DC is to convert it to high-frequency components. This is called as "data-weighed averaging (DWA)" [20].

Figure 16 shows the block diagram of the DWA [21]. In the DWA, each DAC cell has its own address. The cells are selected in the next turn so that the next address starts from one plus the maximum address among the cells used at a given moment. If the maximum address at a given moment is n and the number of DAC cells used in the next turn is m, the address in the next turn is from n+1 to n+m. The encoder in Fig. 16 outputs the number of DAC cell used in the current turn and the accumulator outputs the address to be used in the next turn. The switch matrix rotates DAC cells so that the lowest comparator in Fig. 16 is connected to the DAC cell whose address is the first address to be used in the next turn.

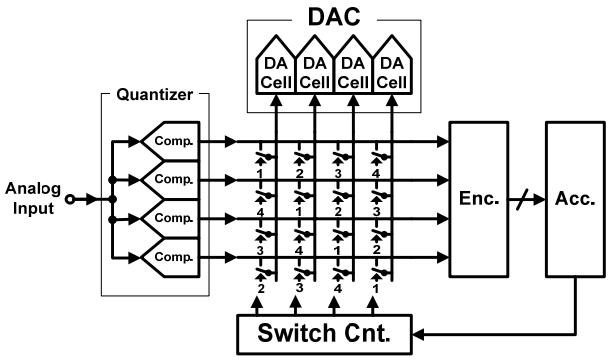


Fig. 16 Block diagram of data-weighted averaging.

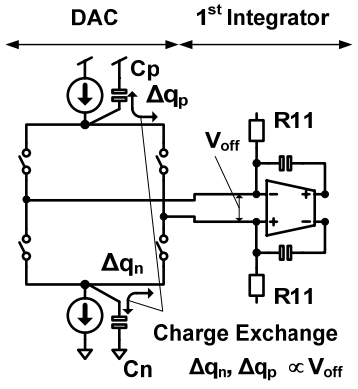


Fig. 17 Sources of 2nd-order distortion.

5.2 Suppression of 2nd-Harmonic Distortion

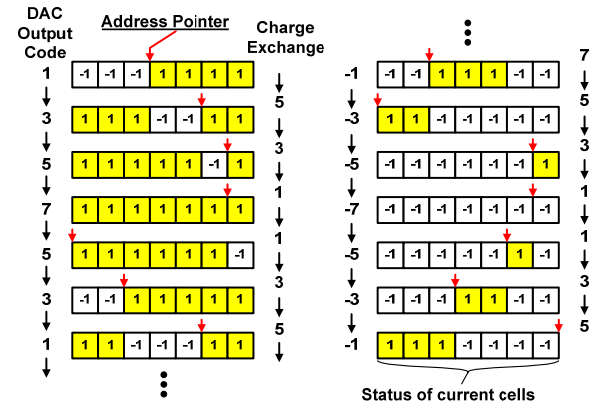
Although the DWA effectively alleviates the distortion caused by the mismatch effect of DAC cells, it generates a 2nd-order distortion when the opamp in the 1st integrator has an offset voltage. Figure 17 shows sources of the 2nd-order distortion. When the 1st integrator has an offset voltage of ΔV, this offset voltage interacts with the parasitic capacitances of the current source of the DAC cell, C_p and C_n, and generates a 2nd-order distortion.

The details of generating a 2nd-order distortion are given in Fig. 18. When the 1st integrator has an offset voltage, DWA varies the charge stored in parasitic capacitances at the current source with a half-period of the input signal. Thus a 2nd-order distortion is generated by the interaction.

Figure 19 validates the effect of the offset calibration using the test chip. The DWA and the offset calibration of the 1st integrator are applied to a 3rd-order delta-sigma modulator. A more than 10 dB SFDR improvement has resulted from the offset calibration of the 1st integrator. In this case, the means of calibration is to use an offset DAC for canceling the offset at the output of the input differential stage.

5.3 Calibration of RC Constant

In the case of continuous time delta-sigma modulators, aside



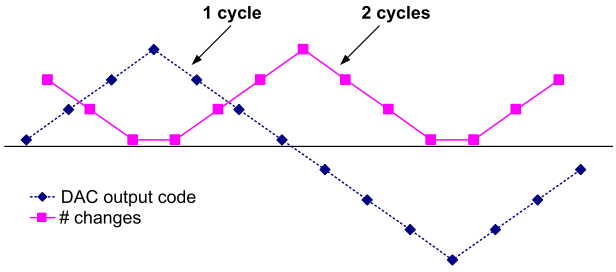
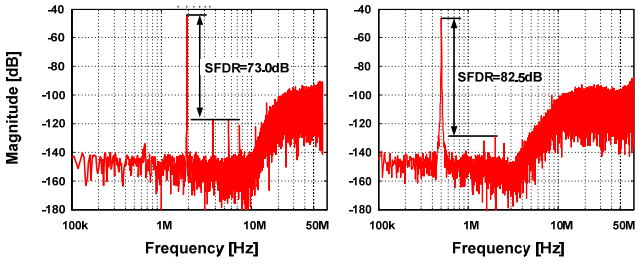


Fig. 18 Generation mechanism of 2nd-order distortion.



(a) Without offset Calib. **(b) With offset Calib.**

Fig. 19 Effect of the offset calibration for 2nd-order distortion.

from the DWA and offset calibration, the calibration of the RC constant of the integrator is essential, because the RC constant is an absolute value that varies too widely.

Figure 20 shows the circuit configuration of the RC relaxation oscillator for RC constant calibration [22]. In the oscillator shown in Fig. 20, the threshold voltage of the comparator is controlled by the feedback loop so that the integral of the oscillator output is constant. This control loop realizes an ideal oscillator insensitive to PVT variation. The oscillation frequency of the oscillator is determined by the following equations.

$$(1-\alpha)(T_{OSC}/RC) = 1 - e^{-(T_{OSC}/RC)}, \quad \therefore \alpha = \frac{V_{ref}}{V_{dd}} \qquad (3)$$

In Eq. (3), we can easily make a variable α constant using a resistor ladder. Thus, the oscillation frequency (T_{osc}) depends on only the RC constant. Thus, we can determine accurately the RC constant by measuring the oscillation period of the oscillator. Resistors in the modulator are changed

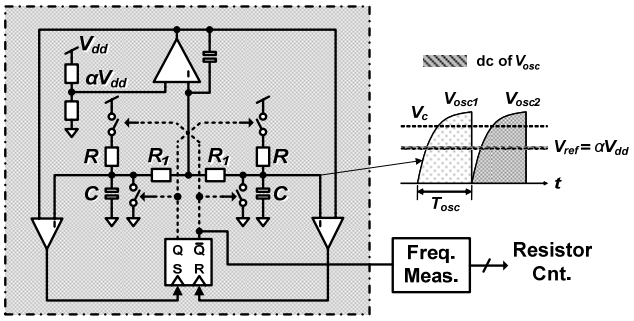


Fig. 20 RC Relaxation oscillator for RC constant calibration.

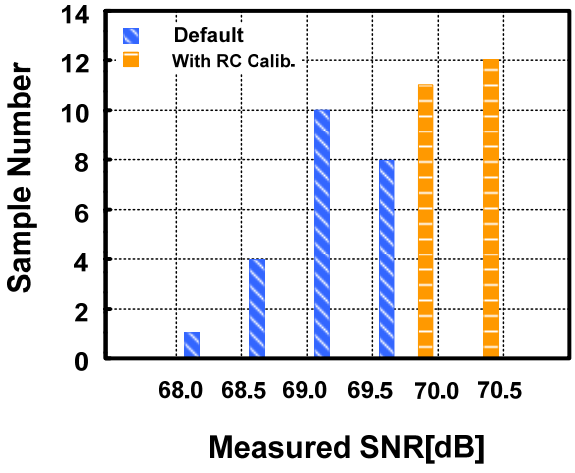


Fig. 21 Improvement in SNR by RC constant calibration.

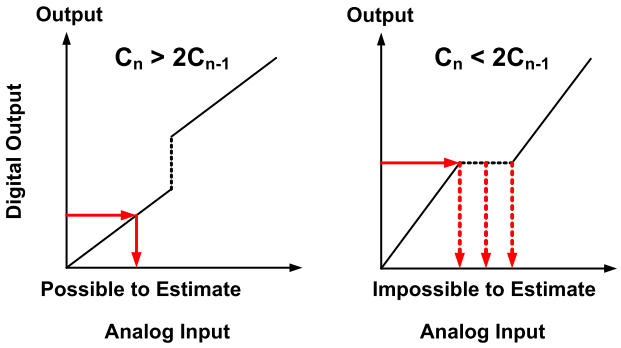


Fig. 22 Classification of in-out characteristics of SAR.

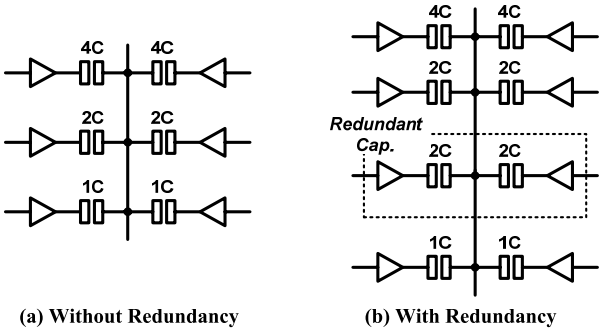


Fig. 23 Capacitor array DAC with redundancy.

so that the RC constant of the modulator can be set to the target value.

Figure 21 shows the measurement result of the improvement in SNR by RC constant calibration. RC-constant calibration can improve the SNRs of all samples to more than 69.5 dB.

6. Calibration Methods for SAR-Type ADCs

The classification of the input-output characteristics of SAR is shown in Fig. 22. There are two cases: one in which the array capacitance of the upper bit is larger than twice that of the lower bit, and the other is the opposite of the first case. In the former case, we can specify the analog input corresponding to the digital output code as shown in Fig. 22(a). However, it is impossible to specify the analog input in the latter case as shown in Fig. 22(b), because plural analog inputs correspond to one digital output.

Thus, the SAR is not suitable to be calibrated only in the digital domain. Some modifications of the analog parts are essential to realize an efficient and simple calibration of SARs.

Actually, a SAR using 1.86-bit coding instead of binary coding was reported [23]. However, this circuit configuration increases both the complexity and area of the SAR. Moreover, it deteriorates the FOM of the SAR, which is originally very small by its nature.

Therefore, the most popular means of calibrating the SAR is to use an additional capacitive DAC, which is shown in Fig. 5. The calibration method using the DAC is very simple. First, the offset of the comparator is calibrated to zero. Then, the capacitance of the capacitor to be calibrated is compared with capacitance corresponding to all of the lower bits of the capacitor to be calibrated so that the two objects being compared are equal.

On the other hand, it is suitable to increase the sampling speed to introduce redundancy into a SAR. Figure 23 compares a capacitor array with and without a redundancy. Figure 23(a) shows a capacitor array of 3bit configuration. On the other hand, Fig. 23(b) shows an additional array for a 2nd bit with a 3-bit configuration to introduce redundancy. The easiest way to explain redundancy is to draw a tree of binary search. Figure 24 shows a comparison of binary search trees. Figure 24(a) shows the conventional type tree of DAC shown in Fig. 23(a), Fig. 24(b) corresponds to Fig. 23(b). In the conventional tree, if the comparator errs in the comparison, the output data never return the correct code. In contrast, in the search tree in Fig. 23(b), the output data can return the correct code even if the comparator errs, because each of the six digital codes from the center have two search paths.

The drawback of introducing redundancy is the increase in the conversion period of one comparison cycle.

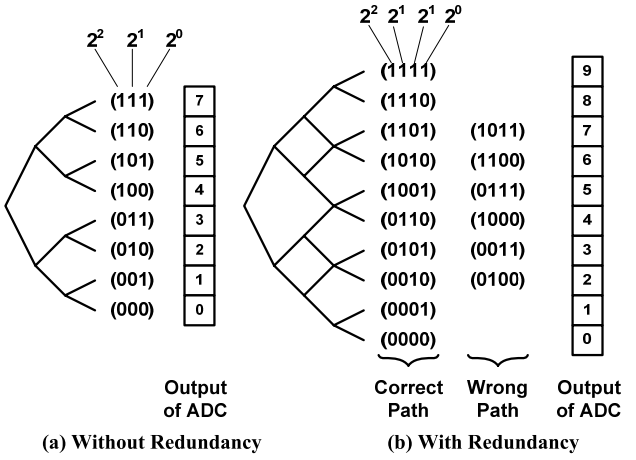


Fig. 24 Binary search tree of SAR.

However, the total period would be shorter than the conventional one because each redundancy allowing a larger settling error shortens the every comparison cycle. A 10-bit SAR with a 100 MHz operating clock has been reported [12].

7. Calibration Methods for Other ADCs

7.1 Delta-Sigma Modulator Using Open-Loop VCO

In this section, we describe an outline of a recent new ADC that uses a time dimension [24].

Figure 25 shows a block diagram of the 1st-order delta-sigma ADC using a time dimension. The input analog voltage is converted to timing information by the VCO. At this moment, input voltage is converted to the phase of the VCO, which means that the input signal is integrated. Then the phase information is quantized. Finally, the quantized phase is converted to frequency information by differentiation. Thus, the quantization noise shifts to the high-frequency region by differentiation. On the other hand, the input signal that is digitized as frequency information is not affected by the frequency operations, because the signal is integrated and differentiated, the effects of which cancel out each other.

A dummy VCO is linearized by the feedback loop using the LMS method. The main VCO is also linearized by the same information of the dummy loop. Thus, the main VCO is linearized within the relative accuracy of two VCOs. When we apply the LMS to a high-order polynomial, we have to solve simultaneous equations. However, the implementation of such solver in the LSI is not appropriate, because it is complex and takes a large chip area.

A simpler means of solving high-order polynomials is to use the steepest descent method. For example, to approximate measured result as a third-order polynomial, $y(x) = a_0 + a_1x + a_2x^2 + a_3x^3$, the following recurrence formulas are used.

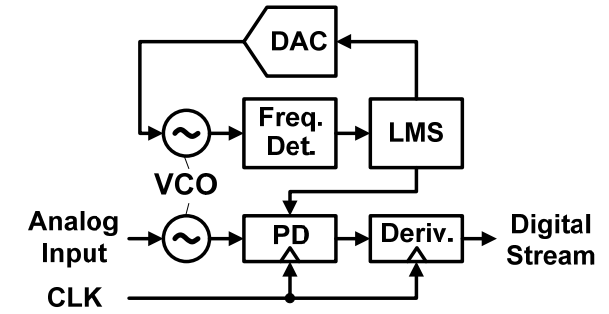


Fig. 25 Block diagram of the 1st-order delta-sigma modulator using VCO.

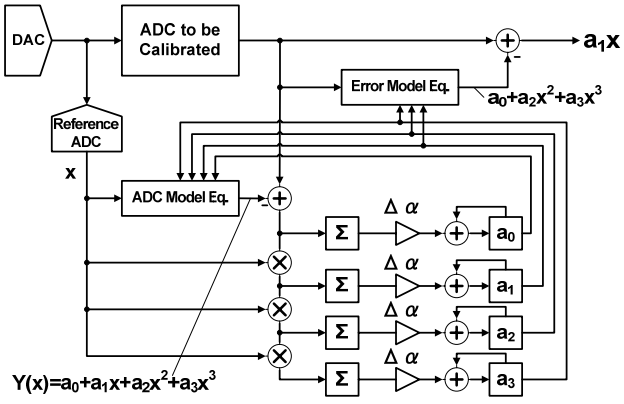


Fig. 26 Block diagram of steepest descent method for LMS.

$$\begin{cases} \alpha_0^{(k+1)} = \alpha_0^{(k)} + \dfrac{2\Delta\alpha}{m}\sum\limits_{i=1}^{m}(t_i - y(x_i)) \\ \alpha_1^{(k+1)} = \alpha_1^{(k)} + \dfrac{2\Delta\alpha}{m}\sum\limits_{i=1}^{m}(t_i - y(x_i))x \\ \alpha_2^{(k+1)} = \alpha_2^{(k)} + \dfrac{2\Delta\alpha}{m}\sum\limits_{i=1}^{m}(t_i - y(x_i))x^2 \\ \alpha_3^{(k+1)} = \alpha_3^{(k)} + \dfrac{2\Delta\alpha}{m}\sum\limits_{i=1}^{m}(t_i - y(x_i))x^3 \end{cases} \tag{4}$$

Here, m is the number of samples and Δa is the parameter for approximating speed and accuracy. Figure 26 concretizes the idea in Eq. (4). The steepest descent method gives us a simple circuit configuration and it is applicable to almost all circuits. However, we have to carefully consider the drawback that it rarely falls into a local minimum point or that it cannot converge into the solution.

7.2 Remaining Issues and Notifications

Thus far, we have calibrated various analog characteristics using digital circuits. However, there are some issues that need to be solved in the future. One of these issues is calibrating a time interleaving system. When we use an ADC with time interleaving, the high-frequency spurious effect falls into a signal band due to sampling skew. In addition, the variation in the frequency characteristics of each ADC causes harmonic distortions. Although some interesting approaches have been reported, it would be difficult to put the

methods practical use owing to both size and power overhead issues [25], [26].

Another point to remember in using digital calibration is noise contamination during the calibration. Noise contamination sometimes deceives a calibration system. Thus, we have to avoid contamination during the calibration period.

8. Conclusions

In this paper, we briefly discussed calibration and correction methods for CMOS-ADCs. The performance of ADCs has been improved markedly by combining with digital collection methods over the last decade. It is very interesting that some circuit configurations thought not to work at a glance are now put into the center stage by using the digital calibration. Thus, this fact will give ADC designers a chance to produce innovative circuits by the digital calibration. We hope for this exciting condition to continue as long as possible.

Acknowledgment

The author would like to express his gratitude to the members of the Panasonic ADC design group, especially to Mr. K. Matsukawa, Dr. K. Obata, Mr. Y. Mitani, Mr. M. Takayama, Dr. Y. Tokunaga, Dr. T. Morie, Mr. S. Sakiyama and Mr. T. Miki for offering materials for the preparation of this paper. The author is also grateful to the Associate Editor and the anonymous reviewers for their constructive and valuable comments and suggestions for the improvement of the quality of this paper.

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