INVITED PAPER *Special Section on Electronic Displays*

Self-Aligned Four-Terminal Planar Metal Double-Gate Low-Temperature Polycrystalline-Silicon Thin-Film Transistors for System-on-Glass

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SUMMARY Self-aligned four-terminal (4T) planar metal double-gate (DG) polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) were fabricated on a glass substrate at a low temperature (LT), which is below 550°C, to realize high performance and low power dissipation system-on-glass (SoG). The top gate (TG) and bottom gate (BG) were formed from tungsten (W); the BG was embedded in the glass substrate and the TG was fabricated by a self-alignment process using the BG as a photomask. This structure is called embedded metal double-gate (E-MeDG) in this paper. The poly-Si channel with lateral large grains was fabricated using a continuous-wave laser lateral crystallization (CLC). The self-aligned 4T E-MeDG LT poly-Si TFT, with a gate length of 5 μm and TG and BG SiO_2 thicknesses of 50 and 100 nm, respectively, exhibited a subthreshold swing of 120 mV/dec and a threshold voltage (V_{th}) of −0.5 V in the connecting DG mode; i.e. when TG is connected to BG. In the TG operation at various BG control voltage, a threshold voltage modulation factor ($\gamma = \Delta V_{th}/\Delta V_{BG}$) of 0.47 at negative BG control voltage and 0.60 at positive BG control voltage are demonstrated, which values are nearly equal to theoretical prediction of 0.40 and 0.75. Trend of subthreshold swing (s.s.) of TG operation under different BG control voltage are also consistent with theoretical prediction. In addition to TG operation, successful BG operation under various TG control voltages was confirmed. Field-effect mobility derived from g_m also varied depending on control gate voltage. The high controllability of device parameter of individual LT poly-Si TFTs is caused by excellent crystalline quality of CLC poly-Si film and will enable us to the fabrication of high-speed and low power-dissipation SoG.

key words: *poly-Si, TFT, double-gate, four-terminal, system-on-glass*

1. Introduction

Low-temperature (LT) polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) with a high on-current are attractive as pixel TFTs in high resolution mobile display such as active-matrix organic light-emitting diodes (AMOLED) and active-matrix liquid crystal displays (AMLCD). Particularly for system-on-glass (SoG), which is expected to be one candidate as future information mobile display, high-performance poly-Si TFTs must be fabricated on a transparent glass substrate in addition to high resolution display, so as to integrate logic and memory circuits monolithically. However, it is difficult for LT poly-Si TFTs on a glass substrate to scale down to the nanometer level because of, first, variation in the size of the glass substrate after the heating process and, second, the surface roughness of the glass substrate. Thus, approaches that do not depend only on scaling are required to improve the performance of LT poly-Si TFTs on glass substrate.

Multigate structures such as double, triple, pi, omega, and gate-all-around structures can potentially be used to realize ideal Si transistors in a nanometer-scale complementally metal-oxide-semiconductor (CMOS) era. Such multigate structures have attracted considerable attention in the area of poly-Si TFTs [1]–[51], for three dimensional (3D) large-scale integrated (LSI) circuits in addition to display application. One of the authors of this paper (A. H.) previously reported self-aligned planar metal double-gate low-temperature (LT) poly-Si TFTs in which a tungsten (W) bottom gate (BG) was embedded in a glass substrate, a W top gate (TG) was fabricated by a self-alignment process using the BG as a photomask, and the TG and BG were electrically connected each other. These TFTs are called embedded metal double-gate LT poly-Si TFTs (E-MeDG LT poly-Si TFTs) [50], [51]. The E-MeDG LT poly-Si TFTs comprise lateral grains larger than 2 μm, which are fabricated using diode-pumped solid-state (DPSS) continuous-wave (CW) laser lateral crystallization, which is called the CLC method [52], [53]. The E-MeDG LT poly-Si TFTs exhibited high performance with a nominal mobility greater than 500 cm^2/Vs and a subthreshold swing (s.s.) of 140 mV/dec. However, it was difficult to control threshold voltage (V_{th}) because a thin undoped poly-Si film (75-nm-thick) was used, and the same metal gate material was used for both n-ch and p-ch TFTs. For fabricating high performance and low-power-dissipation circuits on a glass substrate for SoG, it is necessary to control V_{th} of TFTs. As mentioned earlier, we have already developed the fabrication process for self-aligned E-MeDG LT poly-Si TFTs. In this work, we fabricated four-terminal (4T) self-aligned E-MeDG poly-Si TFTs by modulating the self-aligned E-MeDG LT poly-Si TFT fabrication procedure. The high V_{th} controllability, their small s.s, and high mobility of self-aligned 4T E-MeDG LT poly-Si TFTs will enable us to fabricate high-speed and low-power-dissipation CMOS circuits on a glass substrate.

2. Device Fabrication

Fused quartz glass was used as the substrate in this exper-

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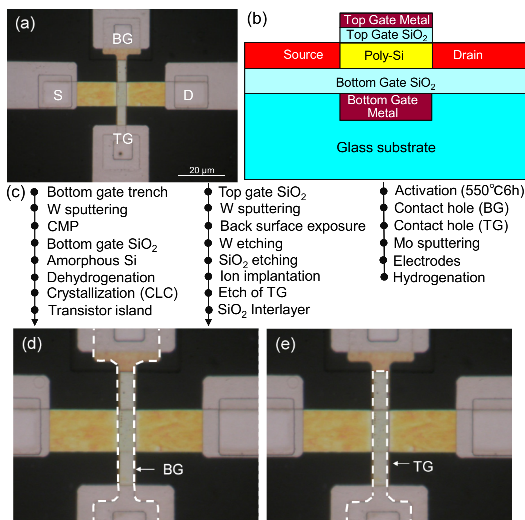

Fig. 1 (a) Top-view image of a completed 4T E-MeDG LT poly-Si TFT, (b) gate stack of 4T E-MeDG LT poly-Si TFT, (c) process flow of 4T E-MeDG LT poly-Si TFT, (d) layout of BG, and (e) layout of TG.

iment. Figure 1(a) and (b) show a top-view photograph of the completed TFT and schematic diagram of cross-section of the 4T E-MeDG LT poly-Si TFTs, respectively. Figure 1(c) shows the process steps involved in the fabrication procedure.

After the fabrication of the BG trench into the glass substrate using reactive ion etching (RIE), a tungsten (W) film was deposited by sputtering at 325°C. The W gate was selected because the work function of W is nearly in the middle of the Si band gap. In addition, W is a refractory metal, and W chemical mechanical polishing (CMP) slurry is commercially available. Next, CMP was employed to form an embedded BG. A 100 nm-thick BG SiO_2 layer and a 75 nm-thick undoped amorphous Si (a-Si) layer were then deposited using PECVD at 325°C. After dehydrogenation annealing in N_2 gas at 500°C for 60 min, the a-Si layer was transformed into a poly-Si film using the CLC method. Overlap laser scanning along the source-drain (SD) direction was used to coat the substrate with a uniform lateral-grained poly-Si film. After the formation of transistor islands, a 50 nm-thick TG SiO_2 layer was deposited using PECVD at 325°C and, then, sputtering of W with a thickness of 40 nm and, next, a positive resist was coated. We used the self-alignment process to fabricate the TG by carrying out back-surface exposure of the g-line using the embedded BG as a photomask. This technique is advantageous for glass substrates. In generally, heat process changes glass size, but this technique enable us to apply self-alignment process even after heat treatment processes. The top W layer was removed by RIE using CF_4+O_2 to form top W gate metal. Subsequently, the SiO_2 layer on the S/D region was removed by dry etching using the TG as a self-aligned mask. The SD regions were doped with phosphorous by ion implantation; the acceleration energy and ion dose used were 10 KeV and 2×10^{15} cm^{-2}, respectively. After the removal of the TG edge region in order to open the space to connect the electrode and the BG, an SiO_2 isolation layer was formed through PECVD at 325°C, following which activation annealing was performed at 550°C for 6 h in N_2. After the formation of a contact hole to connect the electrode and BG, a contact hole connecting the electrode and TG and S/D was formed. Further, an Mo electrode was deposited by sputtering. Finally, hydrogenation was performed through step cooling [54]. Figure 1(d) and (e) show the layouts of the BG and TG, respectively. The device fabrication was performed at a maximum temperature of 550°C.

3. Experimental Results

Figure 2 shows field-emission scanning electron microscopy (FE-SEM) photograph of CLC poly-Si film on BG. Vertical white ribbon in central region corresponds to BG and several white dots correspond to markers to achieve other evaluations of poly-Si film. The poly-Si film was treated by Secco's solution to clarify grain boundaries. It is confirmed that lateral growth of poly-Si was performed without breaking its lateral growth on BG and, as a result, lateral large grains with length more than 5 μm are formed.

Cross sectional transmission electron microscopy (TEM) of TFTs with bottom gate SiO_2 thickness being 50 nm-thick is shown in Fig. 3. The surface of BG includes strong roughness caused by CMP. This figure in-

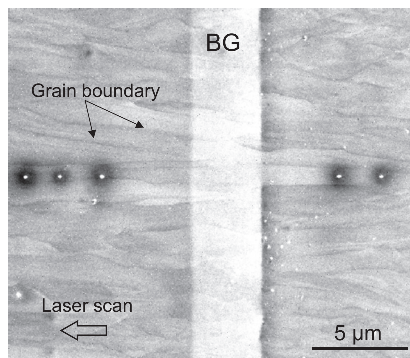

Fig. 2 Field-emission scanning electron microscopy (FE-SEM) image of lateral large grains on BG. To observe grain boundaries, Secco's etching was performed.

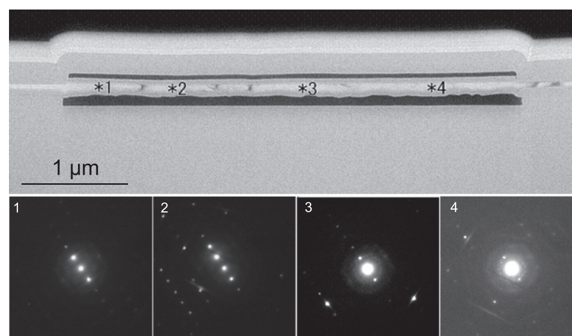

Fig. 3 Cross-sectional transmission electron microscopy of 4T E-MeDG LT poly-Si TFT and electron diffraction pattern at four different points in channel region.

cludes electron diffraction pattern at four points in channel region. Though intensity of diffraction spots is different at every measuring points, they show resemble pattern.

Figure 4 shows the transfer characteristics of the 4T E-MeDG LT poly-Si TFT with gate length of 5 μm in the connecting DG mode under drain voltage of 50, 100 mV and 1.0 V; i.e. when TG is connected to BG. A steep on-current increase with subthreshold swing (s.s.) of 120 mV/dec and V_{th} of −0.5 V was observed.

Figure 5 (a) shows the transfer characteristics of the TG operation of the 4T E-MeDG LT poly-Si TFTs for different BG control voltages (V_{BG}). In this case, drive gate and control gate correspond to TG and BG, respectively. The TG voltage was swept from −2.0 V to 2.0 V with drain voltage of 50 mV and BG control voltage was changed with 0.5 V steps from −2.0 to 1.5 V. Bold solid line in this figure shows transfer characteristic of connected DG mode under drain voltage of 50 mV. The V_{th} was shift from negative to positive with decreasing BG control voltage. Figure 5 (b) shows the transfer characteristics of the BG operation of the 4T E-MeDG LT poly-Si TFTs under different TG control voltages (V_{TG}). In this case, drive gate and control gate become BG and TG, respectively. The V_{th} was shifted from negative to positive with decreasing control voltage, but the amount of shift of V_{th} at each step is larger than that at TG operation.

Figure 6 shows V_{th} of drive TFT under different control gate voltage, in which V_{th} was determined from linear extrapolation method under V_d=0.05 V. We defined γ as modulation magnitude of V_{th} of drive TFT under small variation of control gate voltage (V_{CG}), namely $\gamma = |\Delta V_{th}/\Delta V_{CG}|$, according to research of M. Masahara et al. [55], [56], where ΔV_{th} means variation of threshold voltage of drive TFT and ΔV_{CG} means small variation of control gate voltage. In the case of TG operation under different BG control voltage, γ of 0.47 at negative BG control voltage and 0.60 at positive BG control voltage are obtained. While, in the BG operation under different TG control voltage, they show 1.5 and 2.0, respectively.

Figure 7 shows variation of s.s. of drive TFT under different control gate voltage. The s.s. of TG operation under negative BG control voltage becomes smaller than those of positive BG control voltage, while s.s. of BG operation under different TG control voltage is larger than those of TG operation.

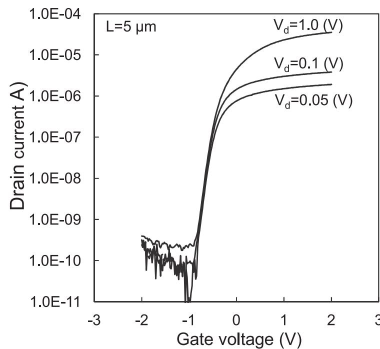

Fig. 4 Transfer characteristics of the 4T E-MeDG LT poly-Si TFT in the connecting DG mode with drain voltages of 50, 100, and 1000 mV.

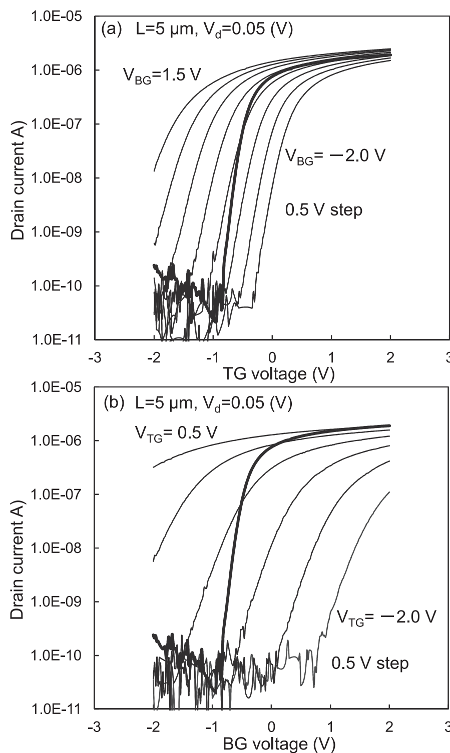

Fig. 5 (a) Transfer characteristic of the TG derive for various BG voltages. (b) Transfer characteristic of the BG drive for various TG voltages. Bold solid lines in each figure show the transfer characteristic of the connecting double-gate mode shown in Fig. 4.

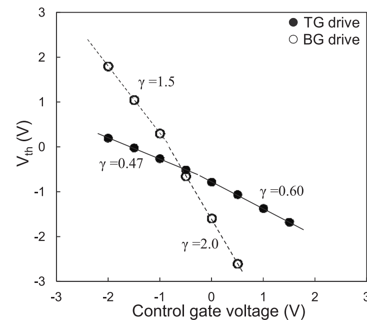

Fig. 6 γ as a function of various control gate voltages.

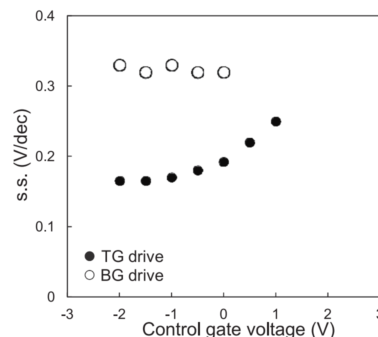

Fig. 7 The s.s. as a function of various control gate voltages.

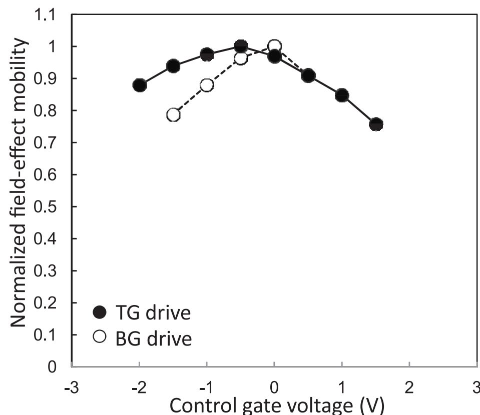

Fig. 8 Variation in field-effect mobility for various control gate voltages. The mobility was normalized by the maximum value.

Figure 8 shows filed-effect mobility of TG and BG operations, respectively. They are normalized by maximum mobility of each mode. The maximum field-effect mobility of TG and BG operation are both 165 cm^2/Vs, which are calculated from g_m. The filed-effect mobility of each mode shows convex shape; namely, they decrease at positive and negative control gate voltage. Ratio of reduction of mobility is larger for BG operation than that of TG operation.

4. Discussion

Our crystallization method facilitates the formation of large grains over a wide range of laser-beam energies at high laser-scanning speeds. Laser scanning generates a temperature gradient at the liquid-solid interface, in which front (molten Si) and rear (solid Si) regions are high and low, respectively, stabilizes the crystallization process and leads to formation of lateral large grain. This mechanism is expected to be established on BG, because the region of BG is localized to small area compared to the size of laser beam (400 × 20 μm^2). Other mechanism to makes easy to form lateral large grains on BG is that there is no step at boundaries between glass and embedded BG due to application of CMP process. The flat surface suffers from nucleation of crystalline defects during solidification.

An excellent s.s. of 120 mV/dec was performed in the connecting DG mode because of operation as a fully-depleted mode. This mode is achieved by following mechanisms. The first is that poly-Si film is made up of high quality film with large grains. This leads to low electrical defects in channel region. Another mechanism is that the poly-Si film is undoped and thin. As a result of combination of these effects, the potential of the Si channel becomes nearly constant in depth in the subthreshold region. This phenomenon is known as “volume inversion,” in which the potential of Si directly follows the gate voltage [57]. This leads to a steep increase in the drain current in the connecting DG mode in the subthreshold region.

Next, we discuss modulation factor of $\gamma = |\Delta V_{th}/\Delta V_{CG}|$. The γ in BG drive are very larger than those of TG drive.

Table 1 Comparison of γ and s.s.

	TG drive(BG control)				BG drive(TG control)			
	γ		s.s.(V/dec)		γ		s.s.(V/dec)	
Control gate	N	P	N	P	N	P	N	P
Theory	0.40	0.75	0.08	0.11	1.3	2.5	0.14	0.21
Experiment	0.47	0.60	0.16	0.25	1.5	2.0	0.32	–

N:negative, P:positive.

This is reasonable because large gate voltage swing of BG is required for small variation of TG control voltage owing to thick BG SiO_2 and thin TG SiO_2 thickness. The s.s. value in TG drive under negative BG control voltage becomes small than those of TG drive with positive BG control voltage. This is caused by generation of back (bottom) channel when positive BG control voltage is applied. The s.s. values of BG drive is inferior to those of TG drive due to thick BG gate SiO_2 thickness.

To achieve more detail analysis of γ and s.s., we compared γ of our data with theoretical approach done by M. Masahara et al. [55], [56]. Their simple model is based on following assumption that, first, Si channel is thin and undoped single crystal, which is free from crystalline defects, and second, interface charge states between Si/SiO_2 and defects in SiO_2 are absent. Though these assumptions are not necessary satisfied for LT poly-Si TFTs, we used their model for simple analysis of our data. According to their model, γ becomes 0.40 and 0.75 for TG drive at negative and positive BG control voltage, respectively. For BG drive under TG as a control gate, γ are 1.3 and 2.5 at negative and positive TG control voltage, respectively. The s.s. of TG drive under negative and positive BG control voltage are 0.08 and 0.11, respectively. While, s.s. of BG drive under negative and positive TG control voltage are 0.14 and 0.21, respectively. These data are summarized in Table 1 with experimental results. Trend in theoretical prediction is consistent with experimental data, but with slight different from experimental data. This is caused by, first, existence of electrical defects caused by grain boundaries of poly-Si film and, second, existence of interface state at SiO_2/Si and defects charge state in SiO_2 due to fabrication of SiO_2 by PECVD, and, third, low temperature TFT fabrication process at 550°C.

Maximum field-effect mobility of TG and BG drive was 165 cm^2/Vs. This is relatively small compared to those of previously reported CLC LT poly-Si TFTs [50], [51]. This may be caused by insufficient optimization of S/D region in 4T E-MeDG LT poly-Si TFTs. As shown in Fig. 3, poly-Si film thickness of S/D region becomes thinner than 75 nm, which is caused by over etching at process to remove top gate SiO_2 layer on S/D region. Thin S/D leads to high resistance of this region and, as a consequane, this leads to inferior field-effect mobility which calculated from g_m. Reduction of mobility at negative control gate voltage is caused by increase of carrier scattering owing to ion- and roughness-scattering by pushing electron to TG SiO_2/Si interface for TG drive [58]. Same mechanism leads to reduction of mobility of BG drive because of electron pushing to BG SiO_2/Si interface. Ratio of reduction of mobility at

negative control gate voltage is larger at BG drive than that of TG drive. It may be caused by strong roughness of BG SiO_2/Si interface caused by CMP process.

The developed in this research is different from groundplane 4T metal-oxide-semiconductor (MOS) field-effect transistors (FETs) because the TFT developed in this research enable us to control V_{th} of individual TFTs. The performance reported in this paper is superior to that previously reported in pioneering work on 4T poly-Si TFTs fabricated on glass substrates [4]. The high controllability of device parameter of individual LT poly-Si TFTs enables us to the fabrication of high-speed and low-power-dissipation CMOS circuits on a glass substrate.

5. Conclusion

In summary, high-performance 4T E-MeDG LT poly-Si TFTs were fabricated on a glass substrate at a low temperature of 550°C. The poly-Si channel with lateral large grains was fabricated using a CLC method. Trends of threshold voltage modulation magnitude, $\gamma = |\Delta V_{th}/\Delta V_{CG}|$, and s.s. were consistent with theoretical prediction, but they are not exactly same values. This is owned to following. First, though our TFTs are made up of lateral large grained poly-Si film, it is not single crystalline Si but poly-Si film. Second, TFTs developed in this research is fabricated by low temperature process, thus quality of SiO_2 and SiO_2/Si interface is inferior to those of high temperature processes. In spite that, the high controllability of device parameter of individual LT poly-Si TFTs will enable us to the fabrication of high-speed and low power-dissipation CMOS circuits on a glass substrate.

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