IEICE TRANS. ELECTRON., VOL.E97–C, NO.3 MARCH 2014

INVITED PAPER Special Section on Leading-Edge Technology of Superconductor Large-Scale Integrated Circuits

# Nb 9-Layer Fabrication Process for Superconducting Large-Scale SFQ Circuits and Its Process Evaluation

Shuichi NAGASAWA[†a)], *Member*, Kenji HINODE[†], Tetsuro SATOH[†], *Nonmembers*, Mutsuo HIDAKA[†], Hiroyuki AKAIKE[††], Akira FUJIMAKI[†], Nobuyuki YOSHIKAWA[†††], Kazuyoshi TAKAGI[††††], *and* Naofumi TAKAGI[††††], *Members*

**SUMMARY** We describe the recent progress on a Nb nine-layer fabrication process for large-scale single flux quantum (SFQ) circuits. A device fabricated in this process is composed of an active layer including Josephson junctions (JJ) at the top, passive transmission line (PTL) layers in the middle, and a DC power layer at the bottom. We describe the process conditions and the fabrication equipment. We use both diagnostic chips and shift register (SR) chips to improve the fabrication process. The diagnostic chip was designed to evaluate the characteristics of basic elements such as junctions, contacts, resisters, and wiring, in addition to their defect evaluations. The SR chip was designed to evaluate defects depending on the size of the SFQ circuits. The results of a long-term evaluation of the diagnostic and SR chips showed that there was fairly good correlation between the defects of the diagnostic chips and yields of the SRs. We could obtain a yield of 100% for SRs including 70,000 JJs. These results show that considerable progress has been made in reducing the number of defects and improving reliability.

***key words:*** *superconducting fabrication technology, Nb/AlOx/Nb Josephson junction, single flux quantum, planarization, shift register*

## 1. Introduction

We have been developing many superconducting single flux quantum (SFQ) circuits using two Nb fabrication processes, called the standard process and the advanced process. The standard process involves using up to four Nb layers and Josephson junctions (JJ) with a critical current density of 2.5 kA/cm$^2$ [1], [2]. On the other hand, the advanced process uses six to ten Nb layers and JJs with a critical current density of 10 kA/cm$^2$ [3]–[8]. Although the advanced process has disadvantages in a longer turn-around time of the fabrication and a larger amount of the photomask costs, it enables SFQ circuits to operate at a higher frequency and to be integrated at a higher density than the standard process. It also requires planarization technology to construct a multi-layer structure having more than six Nb layers and higher reliability than the standard process. To construct the multi-layer structure, we have developed caldera planarization technology [3], [4] and complemented caldera planarization technology [7], [8]. To improve the reliability of the advanced fabrication process, we have designed diagnostic chips and shift register (SR) chips and have been evaluating them over a long term of time [5], [8], [19]–[21].

In this paper, we focus on the advanced process. We describe the recent progress on the Nb nine-layer fabrication process, called ADP2. Its device structure is described in the next section. The process conditions are summarized together with the fabrication process flow and a description of our equipment in Sect. 3. Finally, we describe a long-term evaluation of diagnostic chips and SR chips and discuss the correlation of their results.

## 2. Device Structure of Advanced Process

The device structures in the advanced process have changed slightly as fabrication technology has progressed [3]–[8]. We previously developed the Nb 10-layer fabrication process [8]. After that, since we could manage to compose the SFQ cell structure of the ADP2 without the top Nb layer, we eliminated it to reduce the load on the fabrication process. Figure 1 illustrates the device structure of the current Nb nine-layer fabrication process (ADP2). It is composed of an active layer including JJ and resistor layers at the top, passive transmission line (PTL) layers in the middle, and a DC power layer at the bottom. Although the upper two Nb layers (M8, M9) are not planarized, every other Nb layer (M1-M7) is planarized using the caldera planarization technology [3], [4]. The insulation between M6 and M7 layers is formed by using complemented caldera planarization technology, which enables us to place PTL1 and PTL2 patterns and C1-C5 contacts anywhere, even just below the junctions [7], [8].

The structure shown in Fig. 1 enables us to reduce the influence of magnetic fields due to large bias currents, since the active layer including the JJs, which are very sensitive for magnetic fields, is separated magnetically from the DC power layer and shielded by several ground planes (GND1, GND2, GND3, GP) [9]. This structure also enables us to form the Nb/AlOx/Nb junction layer in the last part of the fabrication process. Its advantages include reducing the damage that the JJs suffer during the fabrication and allowing the future utilization of a high-temperature process such as chemical vapor deposition (CVD) for fabricating the underlying layers of the JJs.

We used an RC type junction [5], [6] to eliminate any degradation in JJ quality due to internal stress of the Nb

Manuscript received July 17, 2013.
Manuscript revised November 5, 2013.

[†]The authors are with AIST, Tsukuba-shi, 305-8568 Japan.
[††]The author is with Nagoya University, Nagoya-shi, 486-0913 Japan.
[†††]The author is with Yokohama National University, Yokohama-shi, 240-8501 Japan.
[††††]The authors are with Kyoto University, Kyoto-shi, 606-8501 Japan.
a) E-mail: s-nagasawa@aist.go.jp

DOI: 10.1587/transele.E97.C.132

Copyright © 2014 The Institute of Electronics, Information and Communication Engineers

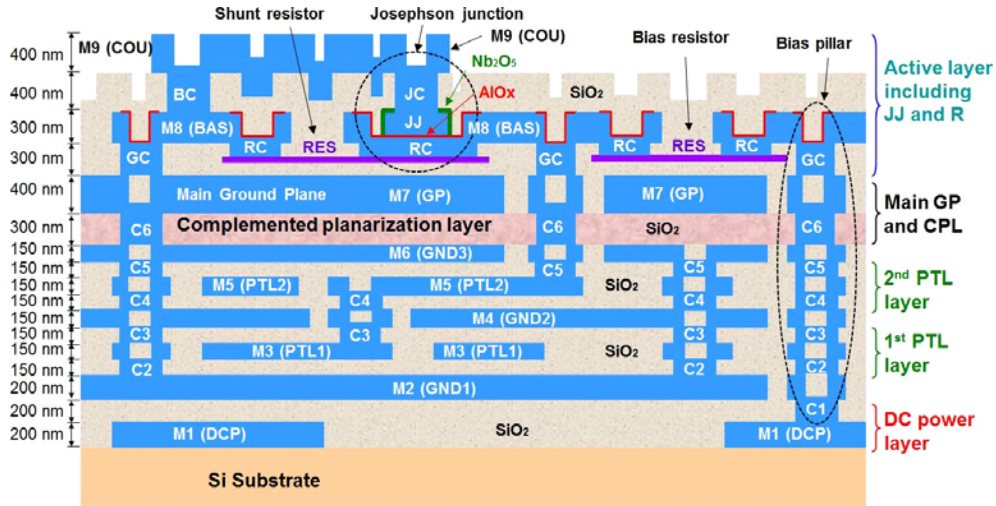



**Fig. 1** Device structure of Nb 9-layer fabrication process (ADP2). JJ: Nb/AlOx/Nb junction, M1-M9: Nb layers, M2, M4, M6, M7: Ground planes, RES: Mo resistor (thickness: 45 nm), C1-C6, GC, RC, BC, JC: Contacts between metal layers, $SiO_2$: Interlayer insulator.

**Table 1** Design rule for ADP2.

| | |
|---|---|
| Critical current density ($J_c$) of JJ | 10 kA/cm$^2$ |
| Minimum JJ size including the shrinkage | $1.1 \times 1.1$ µm$^2$ |
| Critical current ($I_c$) for minimum JJ | 0.1 mA |
| Ic scatterings ($1\sigma$) for minimum JJs | < 2.0% |
| Shrinkage of JJ size | 0.1 µm |
| Sheet resistance (Mo) | 2.4 Ω |
| Minimum line width and space | 1.0 µm |
| Minimum contact for C1 – C6, GC, RC, BC | $0.8 \times 0.8$ µm$^2$ |
| Minimum contact for JC | $0.7 \times 0.7$ µm$^2$ |
| Alignment margin | 0.25 µm |
| Shrinkage for wirings (M1 – M7, M9, RES) | 0 |
| Shrinkage for wiring of M8 (BAS) | 0.2 µm |

films. The RC type junction also has the advantage of being able to reduce the circuit area, since part of the shunt resistor can be formed just below the junction. Optical proximity correction (OPC) patterns are used to reduce shrinkage in small junctions and to obtain critical current values that are linear with respect to the design sizes of the junctions [10].

The concave region on each contact is filled with $SiO_2$ to obtain a flat surface by caldera planarization [4], [5]. Therefore, the stack contact has a shape in which $SiO_2$ is sandwiched between upper and lower contacts. The electrical connection between them is made in the periphery region of the contacts. A multi-stack contact like a bias pillar [11] can be constructed by connecting several stack contacts vertically.

Moreover, effective moat configuration [12], SFQ cell structure [11], and CAD design tools [13], [14] for ADP2 were developed. Until now, many SFQ circuits have been developed by using these ADP2 technologies [15]–[17].

The design rule of ADP2 is shown in Table 1. The shrinkage is one of design parameters to adjust the difference between the designed value and the fabricated one. For example, the minimum JJ designed with $1.1 \times 1.1\,\mu m^2$ becomes $1.0 \times 1.0\,\mu m^2$ when it was fabricated, since it was shrunk by $0.1\,\mu$m.

## 3. Fabrication Technology of ADP2

In this section, we describe the fabrication technology of ADP2, which has undergone numerous developments and improvements. In particular, we describe the process conditions and the fabrication flow and equipment.

We use 3-inch Si wafers whose surfaces are thermally oxidized. A particle detector (Topcon WM-7) is used to select wafers with fewer particles as the fabrication substrate.

### 3.1 Process Flow

Figure 2 shows a flowchart of ADP2 with the fabrication equipment. The fabrication process basically consists of deposition, patterning, etching, cleaning, and probing. $Nb/AlO_x/Nb$ tri-layer, Nb, Mo, and $SiO_2$ films are deposited by three magnetron sputtering systems. The photoresist patterns are formed using an i-line stepper and a coater-developer system. The deposited films are then patterned in the corresponding reactive ion etching (RIE) systems. After dry etching, the residual photoresist is removed using an automatic spin cleaning system. The diagnostic chips including the process test elements are then measured by using an automatic probe system. Besides this basic sequence, chemical mechanical polishing (CMP) and post CMP cleaning are added in the case that planarization is carried out. This sequence is repeated to construct the ADP2 device structure. All fabrication processes are performed at a temperature less than 140°C.

### 3.2 Deposition

The $Nb/AlO_x/Nb$ junction tri-layer is formed with an Nb/Al sputtering system that has a load-lock chamber and three

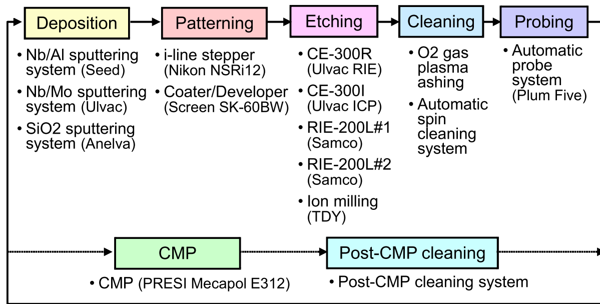



**Fig. 2** Flowchart of ADP2 with fabrication equipment.

**Table 2** Deposition conditions for Nb, Al, and Mo.

| | Nb (JJ) | Al | Nb (wiring) | Mo |
|---|---|---|---|---|
| Deposition system | Nb/Al sputtering system (Seed) | | Nb/Mo sputtering system (Ulvac) | |
| B.G. pressure (Pa) | $5 \times 10^{-6}$ | $5 \times 10^{-6}$ | $5 \times 10^{-6}$ | $5 \times 10^{-6}$ |
| Sputtering method | DC mag. | DC mag. | DC mag. | DC mag. |
| Process gas | Ar | Ar | Ar | Ar |
| Pressure (Pa) | 0.13 | 0.13 | 0.13 | 0.2 |
| RF power (W) | 708 | 92 | 368 | 164 |
| Sputtering target | 8 inch ϕ | 8 inch ϕ | 10 inch ϕ | 10 inch ϕ |
| Deposition rate (nm/min) | 80 | 15 | 95 | 67 |

vacuum chambers for Nb deposition, Al deposition, and oxidation of Al. 300-nm-thick Nb and 10 nm-thick Al films are continuously deposited by DC magnetron sputtering. Once the deposition is finished, the Al film surface is oxidized by introducing an Ar and 1%-$O_2$ mixture gas into the oxidation chamber. This oxidation step lasts for half an hour at a substrate temperature of 20°C. The critical current density of Josephson junctions is mainly determined by the pressure of the Ar and 1%-$O_2$ mixture gas. The target critical current density of 10 kA/cm$^2$ is obtained at the mixture gas pressure of 80 Pa. Under these conditions, the Al film surface is oxidized to a thickness around 1 nm. After that, a 150 nm-thick Nb film is deposited. The Nb/$AlO_x$/Nb tri-layer is continuously formed without breaking the vacuum.

Mo film and Nb films other than the junction tri-layer are deposited with a Nb/Mo sputtering system which has a load-lock chamber and three vacuum chambers for Nb deposition, Mo deposition, and RF Ar plasma cleaning. Table 2 shows the deposition conditions for the Nb, Al, and Mo films.

$SiO_2$ interlayer insulators are deposited with an $SiO_2$ sputtering system that has a load-lock chamber and two vacuum chambers for $SiO_2$ deposition and Pd deposition. The $SiO_2$ insulators are deposited by bias sputtering under two different bias conditions. The RF power of 900 W for the $SiO_2$ target stays the same, but the RF power for the substrate bias is different. One is a soft bias condition which has a substrate RF power of 100 W. The other is a normal bias condition which has a substrate RF power of 300 W. Increasing the substrate RF power improves the step coverage of the $SiO_2$, but increases damage to the underlying Nb [2].

**Table 3** Deposition conditions for $SiO_2$.

| | Soft bias | Normal bias |
|---|---|---|
| Deposition system | $SiO_2$ sputtering system (Anelva) | |
| B.G. pressure (Pa) | $2.0\times10^{-5}$ | $2.0\times10^{-5}$ |
| Sputtering method | RF mag. | RF mag. |
| Process gas | Ar | Ar |
| Pressure (Pa) | 0.5 | 0.5 |
| RF power for $SiO_2$ target (W) | 900 | 900 |
| Sputtering target size | 8 inch ϕ | 8 inch ϕ |
| RF power for substrate bias (W) | 100 | 300 |
| Deposition rate (nm/min) | 20 | 16 |

Table 3 shows the deposition conditions of the $SiO_2$ films. $SiO_2$ interlayer insulators are formed with a combination of bias conditions. For example, the 400-nm-thick interlayer insulator between M8 (BAS) layer and M9 (COU) layer is composed of 60-nm-thick $SiO_2$ with the soft bias condition, 200-nm-thick $SiO_2$ with the normal bias condition, and 140-nm-thick $SiO_2$ with the soft bias conditions. The initial 60-nm-thick $SiO_2$ is used to reduce damage to the surface of the underlying metal layer. The middle 200-nm-thick $SiO_2$ layer is deposited to ensure good step coverage. The last 140 nm-thick $SiO_2$ is deposited to obtain a thick enough step-edge region in the underlying metal layer patterns.

### 3.3 Patterning

We used an i-line stepper (Canon FPA-2500 i3), which has a resolution of 350 nm, numerical aperture of 0.60, and an alignment accuracy of less than 0.1 $\mu$m from 2009 to June 2012. In July 2012, we introduced a new i-line stepper (Nikon NSR-2205i12D). It has a resolution of 350 nm, numerical aperture of 0.63 ~ 0.5, and alignment accuracy of less than 55 nm. Photoresists (Sumitomo Chemical PFI-68, PFI-26) are coated and developed in a coater/developer system (Screen SK-60BW). We do not use any anti-reflective coating technology. The thickness of the PFI-68 and PFI-26 photoresists is 0.7 $\mu$m and 1.0 $\mu$m at 4000 rpm, respectively. The pre- and post-bake temperatures of the photoresists are 90°C and 110°C, respectively.

### 3.4 Etching

The Nb, Al, Mo, and $SiO_2$ films are respectively etched with four etching systems (CE-300R, ion milling, CE300I, RIE-200L). Each etching system has a load-lock chamber and an etching chamber. Table 4 shows the etching conditions for these films. Nb wirings and Mo resistors are formed by reactive ion etching (RIE) with $SF_6$ gas. End-point detection monitoring optical plasma emissions is used for Mo film etching and all of the Nb film etchings except for the ground layers (GND1, GND2, GND3, and GP). The $AlO_x$/Al of the junction is etched by ion milling in Ar gas. The ion beam is accelerated with a voltage of 400 eV at an Ar pressure of $5 \times 10^{-2}$ Pa. The wafer is mounted on the plate that rotates during the milling operation, and the incident angle of

**Table 4** Etching conditions for Nb, Al, Mo, and $SiO_2$.

| | Nb | Al | Mo | $SiO_2$ |
|---|---|---|---|---|
| Etching system | CE-300R (Ulvac) | Ion milling (TDY) | CE-300I (Ulvac) | RIE-200L (Samco) |
| B.G. pressure (Pa) | $3.0\times10^{-4}$ | $3.0\times10^{-4}$ | $3.0\times10^{-4}$ | $7.0\times10^{-3}$ |
| Etching substrate | Quartz | - | Quartz | Carbon |
| Process gas | $SF_6$ | Ar | $SF_6$ | $CHF_3$ |
| Pressure (Pa) | 5 | - | 5 | 2 |
| RF power (W) | 50 | - | 50 | 70 |
| Etching rate (nm/min) | 200 | 4 | 50 | 17 |

the ion beam is 30 degrees for the rotation axis of the plate. Contact holes and a caldera shape for the $SiO_2$ insulators are formed by RIE with $CHF_3$ gas.

### 3.5 Cleaning

First, $O_2$ gas plasma ashing is carried out on every wafer to remove the altered surface of the photoresist due to the RIE. This procedure reduces the number of particles generated in the next cleaning step.

After that, an automatic spin cleaning system completely removes the residual photoresist. This system has a spray nozzle and a high pressure jet nozzle shooting a mildly alkaline solvent called NMP (N-Methyl-2-Pyrrolidone), a pen brash scrub unit, and a 1-MHz ultrasonic deionized (DI) water unit. The temperature of the NMP is 80°C. Several cleaning recipes can be selected in order to control the conditions precisely. An appropriate recipe can be found for each of the process steps.

The cleaning procedure is very important, since even a slight polymer residue can cause fatal defects in the fabrication process.

### 3.6 Probing

Probing is a key technology in increasing the reliability of the fabrication process. We measured diagnostic chips including various process test elements, (described in the next section) by using an automatic probe system (Plum Five PCP-102SL) after each of the Nb and Mo layers was formed. All measured data are compared on site with the expected values, stored in Excel database files, and converted into various tables and figures. Therefore, if there is a defect, we can detect when, where, how it arose. This leads to a prompt resolution of the problem and improvement of the fabrication process.

### 3.7 CMP and Post-CMP Cleaning

Our CMP system (PRESI MECAPOL E312) is very simple compared with the ones used in current semiconductor fabrication plants. The system does not have advanced capabilities such as uniform wafer pressure control, in-line thickness monitor, or in-line cleaning capability. Therefore, the

**Table 5** Polishing conditions.

| | |
|---|---|
| Slurry | Fujimi PLANERLITE-4101 (neutral) |
| Polishing pad | IC1000/suba400 |
| Platen speed | 35 rpm |
| Wafer speed | 30 rpm |
| Weight load | 337 g/cm$^2$ |
| Polishing time | Typically 30 second |

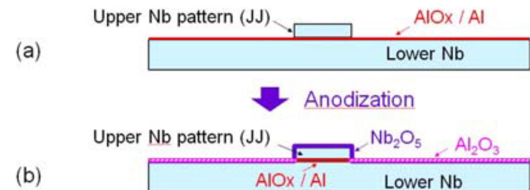



**Fig. 3** Schematic view of anodization for the junction region.

uniformity and run-to-run reproducibility of the polishing rate are not good. For example, there is a large run-to run variation in the polishing rate, which is around 25 nm/min with a variation of +/−10 nm for a flat $SiO_2$ film surface. Moreover, the planarization technology had a pattern-size-dependence problem. However, we overcame these problems by using caldera planarization technology [3], [4], [8]. The uniformity and reproducibility of the planarization are very good, that is, typically within the variation criteria of less than 10%. The polishing conditions are listed in Table 5. Our CMP has few chemical characteristics because it uses a neutral slurry. We can obtain a planar surface with a short CMP, typically 30 seconds. The remaining step height after the caldera planarization is less than 10% of the initial step height (Fig. 4).

The post-CMP cleaning system immediately cleans the polished wafers of slurry left on the wafer. This system has a brush scrub unit, a 1-MHz ultrasonic DI water unit, and a high pressure jet unit. Both sides of the wafer are cleaned with a rotating disk and brush units. After the brush cleaning, residual finer particles are cleaned with a 1-MHz ultrasonic DI water unit. It is possible to choose from several cleaning recipes and thereby precisely control the cleaning conditions.

### 3.8 Anodization

Anodization is carried out to increase the reliability of the junctions [18]. After the upper Nb pattern (JJ) of the Nb/$AlO_x$/Nb tri-layer is formed by RIE (Fig. 3(a)), the entire surface of the wafer is anodized in a mixed solution of ammonium pentaborate (7.8% by weight), ethylene glycol (57.0% by weight), and deionized water (35.2% by weight). The JJ pattern and AlOx/Al barrier are anodized up to a voltage of 15 V with a constant current of 5 mA (0.12 mA/cm$^2$). The JJ pattern surface and $AlO_x$ barrier are anodized to $Nb_2O_5$ and $Al_2O_3$, respectively (Fig. 3(b)). Thickness of anodization is around 30 nm.

We fabricated the Nb nine-layer device structure shown in Fig. 4, by repeating the process flow described above. As

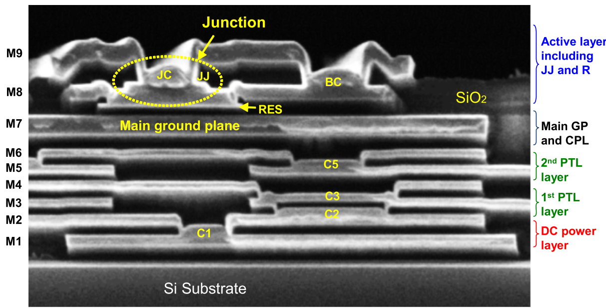



**Fig. 4** Cross-sectional SEM photograph of device fabricated in Nb 9-layer process (ADP2). RC type junction (JJ), single contacts (C1, C5, BC, JC), and stack contact (C2/C3) are shown.

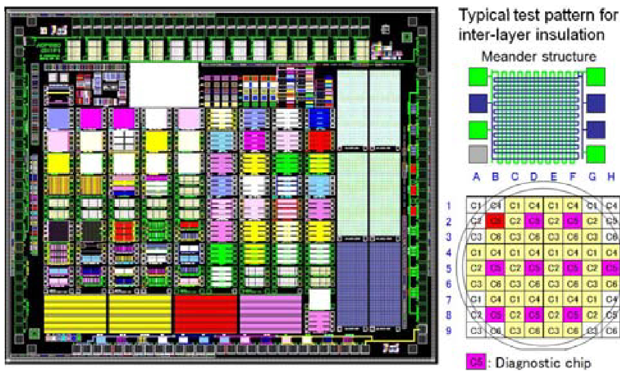



**Fig. 5** Layout of diagnostic chip (8.5 mm × 7.0 mm) and positions of diagnostic chips in a wafer.

shown in this figure, junction region was very flat despite the step edges of several underlying wirings and contacts.

## 4. Process Evaluation

### 4.1 Diagnostic Chip

Figure 5 show a diagnostic chip. It is composed of many different inter-layer and intra-layer insulation patterns, line patterns, junctions, contacts, and resistors [5], [8]. The number of room-temperature test elements per chip is 312. Since ten chips in a wafer are tested, the total number of the probing sites for a wafer is 3120.

Figure 6 plots the run-to-run variation in the total number of defects in diagnostic chips fabricated from March 2011 to July 2012. The total number of probing sites relating to this the defect evaluation was 2110 for every wafer. Many kinds of defects were detected, but the major ones in terms of run-to-run frequency and defect rate of each fabrication were "Contact Open", "JJ Open", and "Contact Inter-layer short" (a short between a layer including the contact and a separate layer over the contacts). The number after the defect name in the figure legend is the measured number of test elements for each defect type. A good fabricated wafer should have fewer than 20 defects, which means no more than two defects per chip, given the measurement results of SR yields described in next section. The ratio of

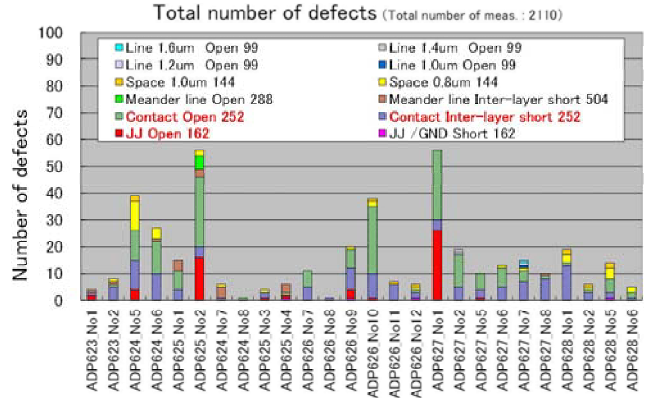



**Fig. 6** Run-to-run variation in defects of diagnostic chips from March 2011 to July 2012.

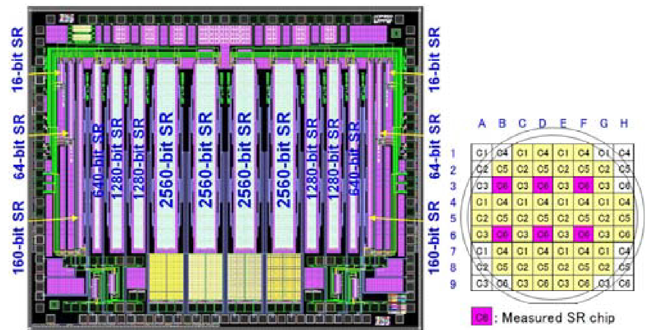



**Fig. 7** Layout of shift register chips and positions of SR chips in a wafer.

**Table 6** Specifications of shift register chip.

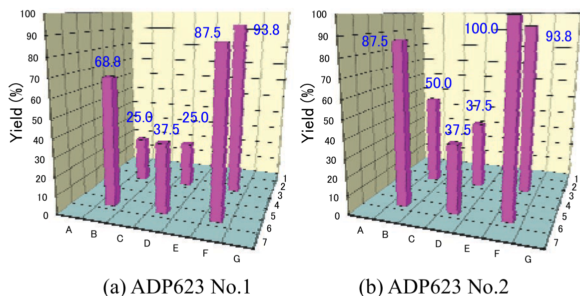
| Bit capacity | Array organization | Total number of JJs | SR_bias (mA) | Number of SRs |
|---|---|---|---|---|
| 16 | 16 x 1 | 90 | 2.75 | 2 |
| 64 | 64 x 1 | 282 | 11 | 2 |
| 160 | 160 x 1 | 666 | 28 | 2 |
| 640 | 160 x 4 | 2589 | 110 | 2 |
| 1280 | 160 x 8 | 5153 | 220 | 4 |
| 2560 | 160 x 16 | 10281 | 440 | 4 |

good wafers was 77% (20/26) during this fabrication period.

### 4.2 Shift Register Chip

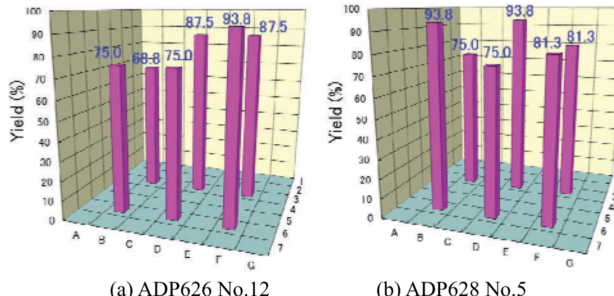
The shift registers (SR) were designed to detect problems that arise from the fabrication of SFQ circuits. Most of the components of the SR cell had the minimum feature size for ADP2. The basic design and device structure for the SR cell are described in reference [8].

To evaluate defects that have a circuit-size dependency, we designed six different SRs which have bit capacities ranging from 16 to 2,560. Figure 7 shows the layout of the SR chip, and Table 6 lists the specifications of the SRs such as array organization, the number of JJs, SR-bias current, and number of SRs. The SR-bias means the total DC bias




(a) ADP623 No.1 (b) ADP623 No.2

**Fig. 8** Yield of shift registers depending on position of chip in a wafer. Six chips (B3, B6, D3, D6, F3, F6) correspond to the positions shown in Fig. 6.




(a) ADP626 No.12 (b) ADP628 No.5

**Fig. 9** Yield of shift registers depending on position of chip in two wafers after making resolution improvements.

current of each SR circuit except for that of the input and output circuits (DCSFQ and SFQDC gates). The number of JJs is about four times the bit capacity because the unit cell is composed of four JJs. Therefore, the total number of JJs is less than 100 for the 16-bit SR and more than 10,000 for the 2,560-bit SR. Since the chip has four circuits for the 1280-bit SR and 2560-bit SR and two circuits for the 16-bit SR to 640-bit SR, the total number of JJs in a chip amounts to around 70,000. Although these SRs were designed for a process evaluation, they also can play a role in demonstrating large-scale SFQ circuits fabricated by ADP2. Figure 7 also shows the positions of the SR chips in a wafer. For each wafer, since 6 SR chips were measured, a total of 12 circuits for the 16-bit to 640-bit SRs, 24 circuits for the 1280-bit and 2560-bit SRs were measured.

The yields of the SRs gradually improved as we developed our fabrication technology described in Sect. 3. Figure 8 shows examples of the measured operating yields of SRs depending on the chip's position in a wafer (ADP623 No.1 and No.2). In this figure, the yields are represented as percentages of correctly operating SRs out of all 16 SRs regardless of the differences in their bit capacities or measured bias margins. From these results, we can see that the distribution of the yields in a wafer is almost the same for these two wafers, in spite of the yield variation between chips being very large. However, we obtained higher yields for the chip of B6, F3, and F6. Especially, we obtained a chip (F6 of ADP623 No.2) having a yield of 100%. This means that SRs including 70,000 JJs in a chip successfully operated [19].

The cause of the large yield difference in the wafers was believed to be pattern resolution instability. We found that the resolution instability came from out-of focus problems due to local wafer flatness variations in the exposure shot area. The stepper could not focus if the large local flatness variation exceeded the depth of focus. Flatness variation was a problem especially because the exposure area of one shot was 17 mm × 21 mm. At first, we doubted that one of the causes of the large local flatness variation was distortion of the wafer due to sputtered film stress in the multilayer structure. However, there was poor resolution even in forming the first layer. Therefore, we examined the flatness of the Si wafers and selected the flatter one. As a result, we obtained high yields for all six chips in the wafers, as shown in Fig. 9 [20], [21].

Figure 10 shows the run-to-run variation in the yields of SR chips. The bar graph shows the yields for SR chips fabricated from March 2011 to July 2012. The bar graphs indicate the measured operating yield depending on the circuit size. The line plots the number of defects detected by the diagnostic chips. As shown in this figure, there is fairly good correlation between the defects and the yields. The yield of larger SRs drastically decreases as the number of defects increases. It is considered that the SRs with more than the certain number of defects cannot operate. There were usually around 10 defects at random locations on the wafer. When the number of defects was less than 20, almost all were random defects, and these random defects did not always affect the SR operation. However, in wafers that had more than 20 defects, the defects included ones due to the variation of fabrication conditions such as etching residue, pattern resolution instability, and insufficient planarization in addition to random defects. These non-random defects seriously affected the SR operation, and they led to the drastic decrease of the yield of the SRs.

We obtained high operating yields (more than 66% (16/24)) for 2560-bit SRs having more than 10,000 JJs in ADP626 No. 8, ADP626 No. 12, and ADP628 No. 5, whose defects were less than 20.

So far, there has been a large variation in the run-to-run yields of the SRs. A few fabrications had low SR yields even though the number of defects was less than 20. We consider that there are still unknown defects or process variations which have not been evaluated by the diagnostic chip. One of causes may be variations of the process conditions that are due to machine problems. The run-to-run yields of the SRs are on the road to improving.

## 5. Conclusion

In this report, we summarized the recent progress in fabrication technology of ADP2 and described the Nb nine-layer device structure, its process conditions, and fabrication equipment.

Diagnostic chips and SR chips were included in every fabrication to improve the reliability of the ADP2. Their

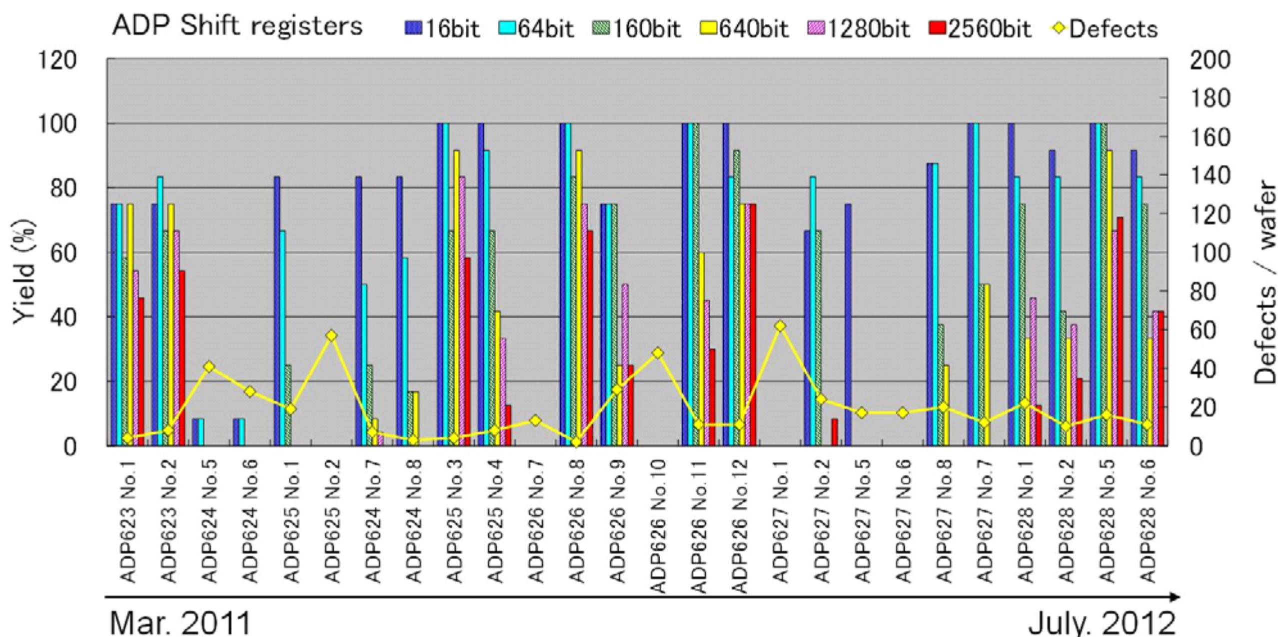



**Fig. 10** Run-to-run variation of the yield of SR chips and number of defects for diagnostic chips. Bar graph indicates yields of the SRs for circuit sizes of from 16 to 2560 bits, and the line graph indicates total number of defects per wafer.

measurements were collected over a long period. We discussed the correlation of the defects between the diagnostic chips and the SR chips. There was fairly good correlation between them.

We obtained an SR yield of 100% as a result of improving our fabrication technology. This means that SRs with 70,000 JJs in a chip operated successfully. However, initially, there was a large yield difference depending on the position of the chip in a wafer. The difference was made smaller by selecting a flatter substrate wafer. As a result, we obtained high yields for all six chips in the wafers and achieved considerable progress in reducing defects and in improving reliability.

## Acknowledgments

This work was mainly carried out in the Superconductivity Research Laboratory, International Superconductivity Technology Center (ISTEC) on the SFQ project titled “Reconfigurable Low-Power High-Performance Processor based on Single-Flux-Quantum Circuitry” supported by the Japan Science and Technology Agency (JST-CREST).

This work was also supported in part by the Japan Society for the Promotion of Science (JSPS: KAKENHI Grant Number 22226009 and 23226019) and the “Low-energy superconductor-spin-optics hybrid systems” project of the Advanced Low Carbon R&D Program (ALCA-JST).

The National Institute of Advanced Industrial Science and Technology (AIST) partially contributed to the fabrication of the circuit.

## References

[1] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, “A 380ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield,” IEEE Trans. Appl. Superconduct., vol.5, no.2, pp.2447–2452, June 1995.

[2] H. Numata and S. Tahara, “Fabrication technology for Nb integrated circuits,” IEICE Trans. Electron., vol.E84-C, no.1, pp.2–8, Jan. 2001.

[3] K. Hinode, S. Nagasawa, M. Sugita, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Pattern-size-free planarization for multilayered large-scale SFQ circuits,” IEICE Trans. Electron., vol.E86-C, no.12 pp.2511–2513, Dec. 2003.

[4] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Development of advanced Nb process for SFQ circuits,” Physica C, vol.412-414, pp.1429–36, 2004.

[5] S. Nagasawa, K. Hinode, T. Satoh, H. Akaike, Y. Kitagawa, and M. Hidaka, “Reliability evaluation of Nb 10 kA/cm$^2$ fabrication process for large-scale SFQ circuits,” Physica C, vol.426-431, pp.1525–1532, 2005.

[6] T. Satoh, K. Hinode, H. Akaike, S. Nagasawa, Y. Kitagawa, and M. Hidaka, “Characteristics of Nb/AlOx/Nb junctions fabricated in planarized multi-layer Nb SFQ circuits,” Physica C, vol.445-448, pp.937–940, 2006.

[7] T. Satoh, K. Hinode, S. Nagasawa, Y. Kitagawa, M. Hidaka, N. Yoshikawa, H. Akaike, A. Fujimaki, K. Takagi, and N. Takagi, “Planarization process for fabricating multi-layer Nb integrated circuits incorporating top active layer,” IEEE Trans. Appl. Supercond., vol.19, no.3, pp.167–170, June 2009.

[8] S. Nagasawa, T. Satoh, K. Hinode, Y. Kitagawa, M. Hidaka, H. Akaike, A. Fujimaki, K. Takagi, N. Takagi, and N. Yoshikawa, “New Nb multi-layer fabrication process for large-scale SFQ circuits,” Physica C, vol.469, pp.1578–1584, 2009.

[9] H. Akaike, K. Shigehara, A. Fujimaki, T. Satoh, K. Hinode, S. Nagasawa, and M. Hidaka, “The Effects of a DC Power Layer in a 10-Nb-Layer Device for SFQ LSIs,” IEEE Trans. Appl. Supercond., vol.19, no.3, part 1, pp.594–597, June 2009.

[10] H. Akaike, Y. Kitagawa, T. Satoh, K. Hinode, S. Nagasawa, and M. Hidaka, "Effect of photomask pattern shape for a junction counter-electrode on critical current uniformity and controllability in Nb/AlOx/Nb junctions," IEEE Trans. Appl. Supercond., vol.15, no.2, pp.102–105, 2005.

[11] H. Akaike, M. Tanaka, K. Takagi, I. Kataeva, R. Kasagi, A. Fujimaki, K. Takagi, M. Igarashi, H. Park, Y. Yamanashi, N. Yoshikawa, K. Fujiwara, S. Nagasawa, M. Hidaka, and N. Takagi, "Design of single flux quantum cells for a 10-Nb-layer process," Physica C., vol.469, no.15-20, pp.1670–1673, Oct. 2009.

[12] K. Fujiwara, S. Nagasawa, Y. Hashimoto, M. Hidaka, N. Yoshikawa, M. Tanaka, H. Akaike, A. Fujimaki, K. Takagi, and N. Takagi, "Research on effective moat configuration for Nb multi-layer device structure," IEEE Trans. Appl. Supercond., vol.19, no.3, part 1, pp.603–606, June 2009.

[13] M. Tanaka, K. Obata, Y. Ito, S. Takeshima, M. Sato, K. Takagi, N. Takagi, H. Akaike, and A. Fujimaki, "Automated passive-transmission-line routing tool for single-flux-quantum circuits based on A* algorithm," IEICE Trans. Electron., vol.E93-C, no.4, pp.435–439, April 2010.

[14] K. Takagi, Y. Ito, S. Takeshima, M. Tanaka, and N. Takagi, "Layout-driven skewed clock tree synthesis for superconducting SFQ circuits," IEICE Trans. Electron., vol.E94-C, no.3, pp.288–295, March 2011.

[15] Y. Yamanashi, T. Kainuma, N. Yoshikawa, I. Kataeva, H. Akaike, A. Fujimaki, M. Tanaka, N. Takagi, S. Nagasawa, and M. Hidaka, "100 GHz demonstrations based on the single-flux-quantum cell library for the 10 kA/cm$^2$ Nb multi-layer process," IEICE Trans. Electron., vol.E93-C, no.4, pp.440–444, April 2010.

[16] M. Tanaka, H. Akaike, A. Fujimaki, Y. Yamanashi, N. Yoshikawa, S. Nagasawa, K. Takagi, and N. Takagi, "100-GHz single-flux-quantum bit-serial adder based on 10-kA/cm$^2$ niobium process," IEEE Trans. Appl. Supercond., vol.21, no.3, part 1, pp.792–796, June 2011.

[17] T. Kainuma, Y. Shimamura, F. Miyaoka, Y. Yamanashi, N. Yoshikawa, A. Fujimaki, K. Takagi, N. Takagi, and S. Nagasawa, "Design and implementation of component circuits of an SFQ half-precision floating-point adder using 10-kA/cm$^2$ Nb process," IEEE Trans. Appl. Superconductivity, vol.21, no.3, part 1, pp.827–830, June 2011.

[18] H. Akaike, Y. Kitagawa, T. Satoh, K. Hinode, S. Nagasawa, and M. Hidaka, "Nb/AlOx/Nb junctions fabricated using ECR plasma etching," Physica C: Superconductivity, vol.412–414, Part 2, pp.1442–1446, Oct. 2004.

[19] S. Nagasawa, K. Hinode, T. Satoh, and M. Hidaka, "Evaluation of advanced fabrication process using both diagnostic chips and shift register chips," Proc. Super-conducting SFQ VLSI Workshop 2011, pp.77–82, 2011.

[20] S. Nagasawa, K. Hinode, T. Satoh, and M. Hidaka, "Yield improvement of shift register chips for Nb-nine-layer fabrication process," Proc. Superconducting SFQ VLSI Workshop 2012, pp.51–54, 2012.

[21] M. Hidaka, S. Nagasawa, K. Hinode, and T. Satoh, "Device yield in Nb-nine-layer circuit fabrication process," IEEE Trans. Appl. Supercond., vol.23, no.3, 1100906, 2013.

**Shuichi Nagasawa** received the M.S. and Dr. Eng. degrees from Nagoya University, Japan, in 1983 and 1998. He has been engaged in research on superconducting integrated circuits, especially on Josephson RAMs since he joined NEC Corporation in 1983. From 1998 to 2013, he was on loan to Superconducting Research Laboratory, ISTEC, where he was engaged in research of single flux quantum (SFQ) circuits and the development of their fabrication process. Since 2013, he has been working at AIST, where he has been engaged in development of a fabrication process for superconducting integrated circuits. Dr. Nagasawa is a member of the Japan Society of Applied Physics.

**Kenji Hinode** received his M.S. degree in 1976 and Ph.D. degree in 1979 both in Materials Science from the University of Tokyo. Since 1979 to 2001 he was engaged in the research and development of LSI at Hitachi, Ltd. He is currently studying the fabrication process of superconductivity devices at National Institute of Advanced Industrial Science and Technology.

**Tetsuro Satoh** received his M.S. in material science from Tohoku University in 1986, and his Ph.D. from the University of Tokyo in 2001. He joined NEC Corporation in 1986, where he was engaged in research on superconducting materials, devices, and fabrication processes. From 2002 to 2012, he worked at ISTEC as a Research Scientist. He is currently working at AIST. Dr. Satoh is a member of the Japan Society of Applied Physics.

**Mutsuo Hidaka** received his M.S. in applied physics from Kyushu University in 1982. He also received his Ph.D. in 1998 in electronics engineering from the University of Tokyo. He joined NEC Corporation in 1982. He was at Arizona State University as a visiting scientist from 1990 to 1991. In 2002, he temporarily transferred to ISTEC, Since 2013, he has been working at AIST, where he has been engaged in development of fabrication process for superconducting integrated circuits. Dr. Hidaka is a member of the Japan Society of Applied Physics.

**Hiroyuki Akaike** received the B.E., M.E., and Ph.D. degrees in electronic engineering from Nagoya University in 1990, 1992, and 1995, respectively. Since 1995, he has been with Nagoya University, where he is currently an associate professor. In 2003, he stayed in Superconductivity Research Laboratory, ISTEC to be engaged in the development of Nb advanced fabrication process for a year. He has been involved in the research of superconducting devices and fabrication processes. He is a member of the Japan Society of Applied Physics.

**Akira Fujimaki** received the B.E., M.E., and Dr. Eng. degrees from Tohoku University, Sendai, Japan, in 1982, 1984, and 1987, respectively. He was a Visiting Assistant Research Engineer at the University of California, Berkeley, in 1987. Since 1988, he has been working on superconductor devices and circuits at the School of Engineering, Nagoya University, Nagoya, Japan, where he is currently a professor. His current research interests include single-flux-quantum circuits and their applications based on low- and high-temperature superconductors.

**Nobuyuki Yoshikawa** received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-electron-tunneling devices, quantum computing devices and cryo-CMOS devices. Prof. Yoshikawa is a member of the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, and the Institute of Electrical and Electronics Engineers.

**Kazuyoshi Takagi** received the B.E., M.E. and Dr. of Engineering degrees in information science from Kyoto University, Kyoto, Japan, in 1991, 1993 and 1999, respectively. From 1995 to 1999, he was a Research Associate at Nara Institute of Science and Technology. He had been an Assistant Professor since 1999 and promoted to an Associate Professor in 2006, at the Department of Information Engineering, Nagoya University, Nagoya, Japan. He moved to Department of Communications and Computer Engineering, Kyoto University in 2011. His current interests include system LSI design and design algorithms.

**Naofumi Takagi** received the B.E., M.E., and Ph.D. degrees in information science from Kyoto University, Kyoto, Japan, in 1981, 1983, and 1988, respectively. He joined Kyoto University as an instructor in 1984 and was promoted to an associate professor in 1991. He moved to Nagoya University, Nagoya, Japan, in 1994, and promoted to a professor in 1998. He returned to Kyoto University in 2010. His current interests include computer arithmetic, hardware algorithms, and logic design. He received Japan IBM Science Award and Sakai Memorial Award of the Information Processing Society of Japan in 1995, and The Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology of Japan in 2005.