

Room-Temperature Gold-Gold Bonding Method Based on Argon and Hydrogen Gas Mixture Atmospheric-Pressure Plasma Treatment for Optoelectronic Device Integration

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SUMMARY Low-temperature bonding methods of optoelectronic chips, such as laser diodes (LD) and photodiode (PD) chips, have been the focus of much interest to develop highly functional and compact optoelectronic devices, such as microsensors and communication modules. In this paper, room-temperature bonding of the optoelectronic chips with Au thin film to coined Au stud bumps with smooth surfaces (R_a : 1.3 nm) using argon and hydrogen gas mixture atmospheric-pressure plasma was demonstrated in ambient air. The die-shear strength was high enough to exceed the strength requirement of MIL-STD-883F, method 2019 (×2). The measured results of the light-current-voltage characteristics of the LD chips and the dark current-voltage characteristics of the PD chips indicated no degradation after bonding.

Key words: *heterogeneous integration, low-temperature bonding, surface-activated bonding, atmospheric-pressure plasma, optical microsystems*

1. Introduction

Heterogeneous integration of materially different optical components made with wide ranges of fabrication processes onto a single platform enables us to construct small, high-performance, and multifunctional optoelectronic devices. Low-temperature bonding methods are important integration techniques for realizing advanced optoelectronic devices [1]. Table 1 summarizes typical bonding techniques used for semiconductor device fabrication. Bonding methods are categorized into two groups: direct bonding, such as anodic bonding and fusion bonding, and intermediate layer bonding, such as solder bonding, thermocompression bonding, and adhesive bonding. All these methods have emerged in response to many different applications. Among these bonding methods, low-temperature bonding methods have been the focus of recent interest to create unique device structures for a wide range of photonic applications. The advantage of low-temperature bonding methods is that they are free from the various problems caused by the large thermal expansion mismatch between the bonding materials during annealing in the conventional bonding methods.

Here, we focus on intermediate layer bonding using gold (Au). Au has several highly desirable properties, such

as oxidation and corrosion resistance, as well as high electrical and thermal conductivities. Due to these properties, Au has been typically used as the top layer metal of the electrodes of many optoelectronic devices. Recently, numerous experimental studies on low-temperature Au-Au bonding have been carried out [2]–[16]. Surface-activated bonding (SAB) is one of the most promising candidates for achieving low-temperature metal bonding. Au-Au SAB enables bonding at low-temperature (from room temperature to 150°C) in ambient air. The SAB of a laser diode (LD) with Au thin films to Au thin film [4], to Au microbumps [6], or to coined Au stud bumps [8] has been reported using low-pressure argon (Ar) radio frequency plasma. Three-dimensional (3D) integration of multiple chips has been demonstrated due to its characteristics of low-temperature solid-state bonding for high-density packaging. However, the low-pressure plasma process requires an expensive vacuum system and has the problem of increased process time for the vacuum processing.

In this paper, to realize a low-cost instrument and to improve productivity, atmospheric-pressure (AP) plasma, which has been successfully applied for a pretreatment method for ultrasonic bonding [17], [18], is applied to Au-Au SAB. The entire bonding process, including surface activation, is carried out in ambient air. In addition, to realize room-temperature bonding, thick Au bumps ($> 10 \mu\text{m}$) with smooth surfaces ($R_a < 3 \text{ nm}$) fabricated by a simple stud bumping and coining process are used for bonding.

2. Experiments

2.1 Bump Fabrication and Bonding Processes

Au bump fabrication and low-temperature bonding processes are shown in Fig. 1. Au stud bumps are formed on silicon (Si) substrates by a stud bonding machine [Fig. 1 (a)]. They can be easily formed on the 3-D structure substrate, because the fabrication process does not require photolithography. However, typical stud bumps have sharp tips on top of the bumps. If the LD chip is bonded on stud bumps with sharp tips, stress concentration will lead to its degradation. Therefore, a coining process using the flat surface of the Si chips was used to flatten the tips and create smooth tops of the stud bumps. The tips of the Au stud bumps are

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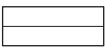

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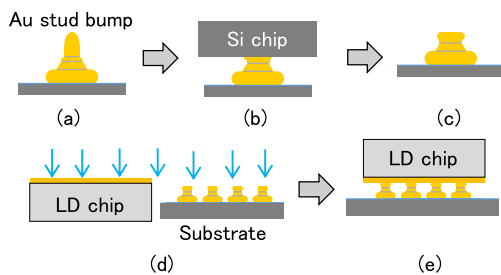
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Table 1 Typical bonding techniques used for semiconductor device fabrication.

Categories	Bonding methods	Typical bonding temperature (°C)	Features
Direct bonding 	Anodic bonding	300–500	High bond strength
	Fusion bonding	600–1200	High bond strength
	Plasma activation bonding	150–400	Low temperature
	Surface activated bonding	Room temperature up to 150	Low temperature, High bond strength
Intermediate layer bonding 	Metallic interlayer		
	Solder bonding/Eutectic bonding	180–450	Tolerant to surface roughness
	Transient liquid phase bonding	180–300	High re-melting temperature
	Thermocompression bonding	300–500	Solid state bonding
	Ultrasonic bonding	Room temperature up to 250	Low temperature, Solid state bonding
	Surface activated bonding	Room temperature up to 150	Low temperature, Solid state bonding
	Insulating interlayer		
Adhesive bonding	Room temperature up to 300	Low temperature, Tolerant to surface roughness	
Glass frit bonding	400–500	Tolerant to surface roughness	

**Fig. 1** Schematic diagram of the bump fabrication and bonding processes: (a) Au stud bumping, (b) coining using Si chip, (c) formation of a flat and smooth top surface, (d) atmospheric-pressure plasma treatment, (e) low-temperature bonding in ambient air.

coined by being pressed against the flat surface of the Si chip [Figs. 1 (b), (c)]. Then, the Au bumps on the Si substrate and the Au thin film on the chips are activated by AP plasma [Fig. 1 (d)]. After plasma activation, the Au bumps and Au thin film are brought into contact for 30 s with a controlled contact load and temperature in ambient air [Fig. 1 (e)].

2.2 Experimental Procedure

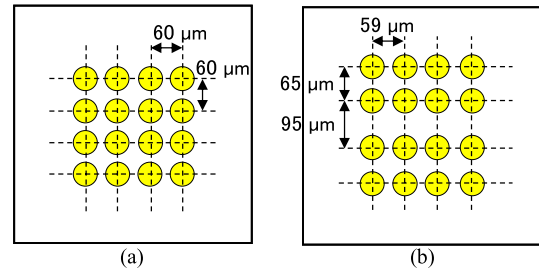
AP plasma based on a dielectric barrier discharge was used for the surface activation of Au prior to low-temperature Au-Au bonding. The plasma treatment was performed with two different mixed gases: argon-oxygen mixed gas (Ar+O₂) and argon-hydrogen mixed gas (Ar+H₂). An AP plasma processing unit (Aiplasma, Matsushita Electric Works Co.) was used for the experiments. The conditions of the AP plasma treatment are shown in Table 2.

For investigation of the AP plasma containing active species, optical emission spectroscopy was performed using a multiband plasma-process monitor (Hamamatsu Photonics, C10346-01).

Bonding strength was evaluated by using Si chips (width: 300 μm, length: 300 μm, height: 100 μm) with Au thin films (thickness: 0.5 μm, R_a: 1.3 nm) instead of real LD chips. The bumps array arrangement for the bonding

Table 2 Atmospheric-pressure plasma treatment conditions.

Gas flow rate	Ar+O ₂ AP plasma; Ar: 2.14 L/min O ₂ : 27.0 mL/min Ar+H ₂ AP plasma; Ar: 2.14 L/min H ₂ : 0.03 L/min
RF Power	150 W
Gap distance	6 mm
Treatment time	30 s

**Fig. 2** Schematic diagram of the arrangement of bump arrays: (a) for die-shear test chips, (b) for LD chips.

of Si chips is shown in Fig. 2 (a). Au stud bumps (purity: 99.99%) coined at 450 gf (28 gf/bump) were used for the experiments. Bonding strength was tested by the shear tester (RHESCA PTR-1100). The fracture mode was analyzed with scanning electron microscopy (SEM) after the die shear test.

InGaAsP/InP buried heterostructure LD chips (width: 400 μm, length: 450 μm, height: 100 μm, wavelength: 1.31 μm) with Au thin film electrodes (thickness: 0.5 μm, R_a: 2.1 nm) were used to evaluate the optoelectronic characteristics before and after bonding. The bumps array arrangement for the bonding of LD chips is shown in Fig. 2 (b). An active region of the buried heterostructure LD chip is buried in the lower refractive indices InP layers on all sides. The bumps were located away from the active region to reduce the stress in the active region, as described later.

Surface-illuminated and flip-chip-mountable InGaAs

PD chips (width: 280 μm, length: 460 μm, thickness: 150 μm), which have the anode and cathode (pad diameter: 80 μm) on the same side, were used to investigate the influence of AP plasma treatment on the electric properties of PD chips. The electrode pads of a PD chip have a metallization consisting of 1 μm of Au.

Light-current-voltage (L-I-V) characteristics of LD chips and dark current-voltage (I-V) characteristics of PD chips were measured by an L-I-V test system (Asahi Data Systems, ALT-7103B) and an electrometer (Keithley Model 6517A), respectively.

3. Numerical Analysis of Stress Distribution during Compressive Loading

To determine the arrangement of bump arrays, the stress distribution in the active region of the buried heterostructure LD chip was analyzed based on the 3D elastic-plastic finite element method. It is known that large stress on an LD chip generates dislocations in the active region and leads to degradations. Therefore, it is required to reduce the stress caused by the compressive loading. Figure 3 shows the three-dimensional analysis model. For comparison, we prepared two models: InP LD chips with Au thin films (thickness: 0.5 μm) to Au thin film (thickness: 0.5 μm) [Fig. 3 (a)] and to Au stud bumps (45 μm square and 10 μm thick) [Fig. 3 (b)]. The location of the active region is 5 μm from the bottom surface of the LD chip (junction-down configuration). The bumps were located away from the active region to reduce the stress in the active region.

Figure 4 shows the simulated cross-sectional profile of the von Mises stress distribution in the LD chip when the bonding pressure of 52 MPa was applied on top of the chip

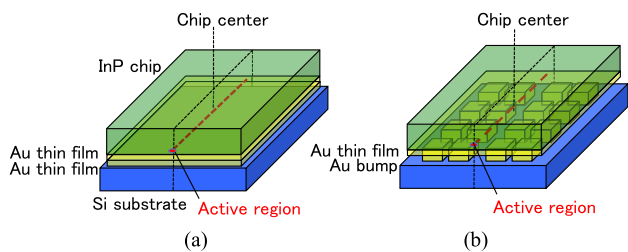


Fig. 3 Schematic diagram of the three-dimensional analysis models: (a) an InP LD chip on Au thin film, (b) an InP LD chip on Au bumps.

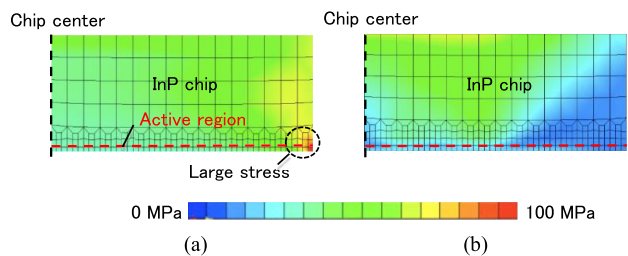


Fig. 4 Simulated cross-sectional profile of the von Mises stress distribution in an InP LD chip when a bonding pressure of 52 MPa was applied on top of the chip: (a) Au thin film, (b) Au bumps.

(no change in temperature). Because there is an axis of symmetry at the center of the LD chip, only one-half of the cross-section is shown. The results show that appropriate arrangement of bump arrays can reduce the stress in the active layer of the LD chip to a value as low as 20 MPa. Alternately, the LD chip on the Au thin film generated a large stress over 100 MPa at the edge of the active region. It has been reported that stress as small as 20 MPa does not affect the characteristics of quantum well structures [19].

4. Experimental Results and Discussion

4.1 Coined Stud Bumps

Coined Au stud bumps (purity: 99.99%) were fabricated using Si chips (R_a : 0.2 nm). Typical SEM images of Au stud bumps before and after coining are shown in Fig. 5. The surface area increased and the height of the Au stud bumps decreased with increasing coining load (Table 3). Figure 6 shows a typical atomic force microscope (AFM) image of the top of a coined bump (28 gf/bump). Thick Au bumps (thickness: 15.3 μm) with smooth surfaces (R_a : 1.3 nm) were realized on the Si substrate. These bumps are easily fabricated at the bottom of the cavity structures.

4.2 Optical Emission Spectroscopy

Typical emission spectra are shown in Fig. 7. The observed

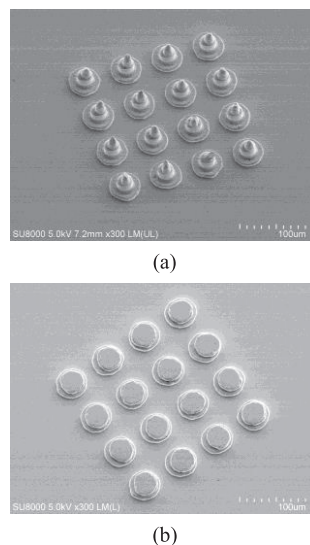


Fig. 5 SEM images of Au stud bumps: (a) before coining, (b) after coining (coining load: 28 gf/bump).

Table 3 Relationship between the coining load, surface area, and height of Au stud bumps.

Coining load (gf/bump)	Surface area (μm ² /bump)	Height (μm)
28	709	15.3
56	1,300	10.5
94	1,373	10.0

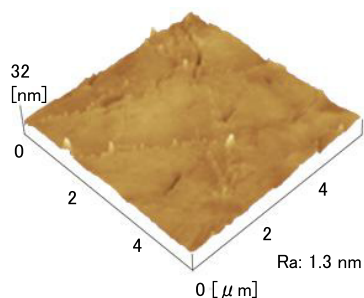


Fig. 6 AFM image of the top surface of an Au stud bump after coining (coining load: 28 gf/bump).

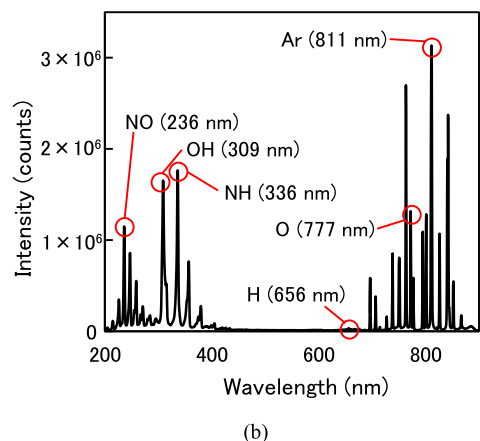
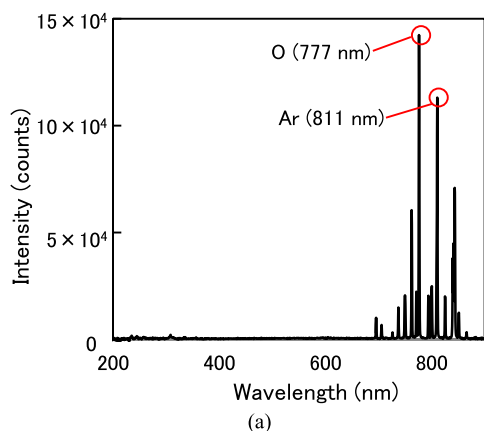


Fig. 7 Measured emission spectra: (a) Ar+O₂ AP plasma, (b) Ar+H₂ AP plasma.

emission spectrum of Ar+O₂ AP plasma [Fig. 7 (a)] is dominated by bands of O (maximum at 777 nm) and Ar (maximum at 811 nm). The atomic oxygen (O) can react with carbon containing contamination on the Au surface to form gas phase products such as CO and CO₂. Alternately, Ar+H₂ AP plasma radiation [Fig. 7 (b)] contains the emission of NO (maximum at 236 nm), OH (maximum at 309 nm), NH (maximum at 336 nm) and Ar (maximum at 811 nm). The NO (NO γ -system) is from the water vapor in the air and is known to react with ozone (O₃) and produce atomic oxygen (O) [20]. Therefore, highly reactive hydroxyl (OH) and O react with organic contaminants on the Au surface to form

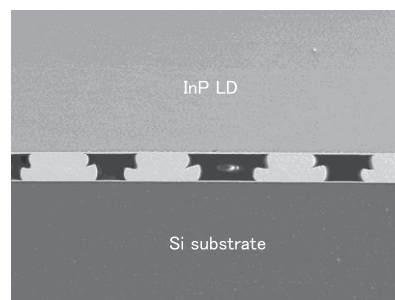


Fig. 8 Typical cross-sectional SEM image of a bonded LD chip on the Si substrate.

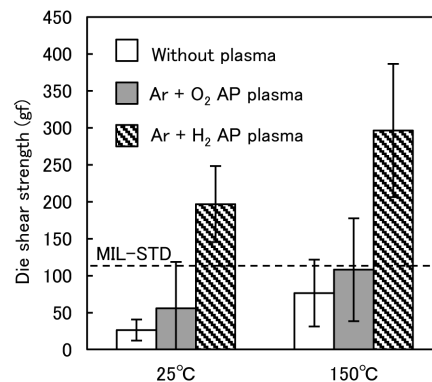


Fig. 9 Die-shear strength with different gases and bonding temperatures (contact load: 680 gf).

gas-phase products.

The plasma-treated surfaces were characterized by X-ray photoelectron spectroscopy (XPS) analysis. The measured C1s region was mainly composed of C-C bonds (284.5 eV) [21] and C-H bonds (285.4 eV) [21] before plasma treatment, and the C1s peak was significantly decreased after the AP plasma treatment (30 s).

4.3 Bonding Strength

Figure 8 shows a typical SEM image of the cross section of a bonded LD chip on the Si substrate. Figure 9 shows the effect of the bonding temperature (25 and 150°C) on the die-shear strength (contact load: 680 gf) of the Si chips. The shear strength failure criteria from MIL-STD-883F, method 2019 ($\times 2$), for the used chips (width: 300 μ m, length: 300 μ m) is 112 gf. The die-shear strength increased with increasing bonding temperature, and Ar+H₂ AP plasma treatment improved the die-shear strength significantly. Even at a bonding temperature of 25°C, the die-shear strength exceeded the failure criteria. However, with Ar+O₂ plasma treatment, the die-shear strength did not exceed the failure criteria.

After the treatment of Ar+O₂ plasma, oxidation of the Au surface (Au₂O₃) was detected by the chemical shift of the 4f levels in XPS spectra [22], [23]. Although Au is most resistant against oxidation in air, even at high temperatures, the plasma oxidation of Au samples has been reported in the

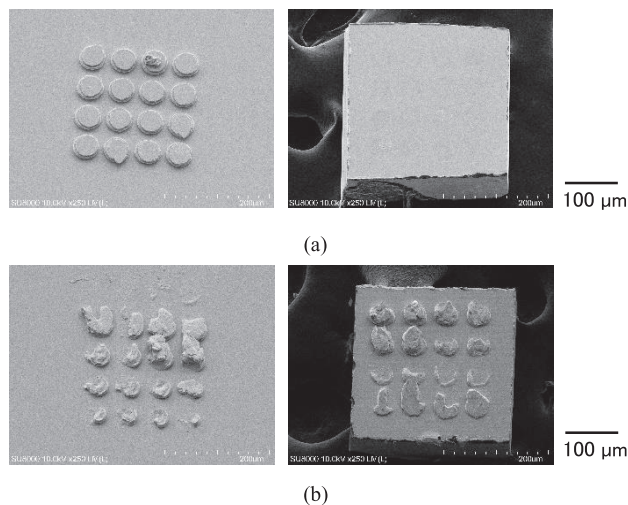


Fig. 10 SEM images of fractured surfaces after the die-shear test (left: substrate side, right: chip side): (a) Ar+O₂ AP plasma treatment, (b) Ar+H₂ AP plasma treatment.

literature [18], [24], [25]. It has also been reported that the gold oxide thermally desorbs in two steps (170 and 260°C) and that an annealing temperature of over 260°C is necessary for the oxide removal [25]. The surface oxide layers impede bonding between Au and Au. Therefore, the need for oxide-free Au surfaces prior to Au-Au bonding is critical for low-temperature bonding. In the case of Ar+H₂ AP plasma treatment, hydrogen radicals may remove the gold oxide.

SEM images of the fractured surfaces after the die-shear test are shown in Fig. 10. In the case of Ar+H₂ AP plasma treatment, Au bumps were transferred to the chip side, as shown in Fig. 10(b). This also indicates that Ar+H₂ AP plasma treatment realizes strong bonding between Au/Au surfaces.

4.4 Electro-Optical Characteristics of LD and PD Chips

InGaAsP/InP LD chips and InGaAs PIN PD chips were bonded with coined Au stud bumps (bonding temperature: 150°C). Figure 11 shows the typical light-current-voltage characteristics of the LD chips and the dark current-voltage characteristics of the PD chips before and after bonding using Ar+H₂ AP plasma treatment. These results indicated no degradation after bonding.

5. Conclusions

Room temperature bonding of the optoelectronic chips in ambient air was demonstrated using Au-Au SAB based on AP plasma treatment. Ar+H₂ AP plasma treatment was effective in improving the bondability between Au/Au surfaces compared with Ar+O₂ AP plasma treatment. It has the advantage of being low-cost because an expensive vacuum chamber and pump for evacuation are not required for plasma generation. This Au-Au SAB method is expected to

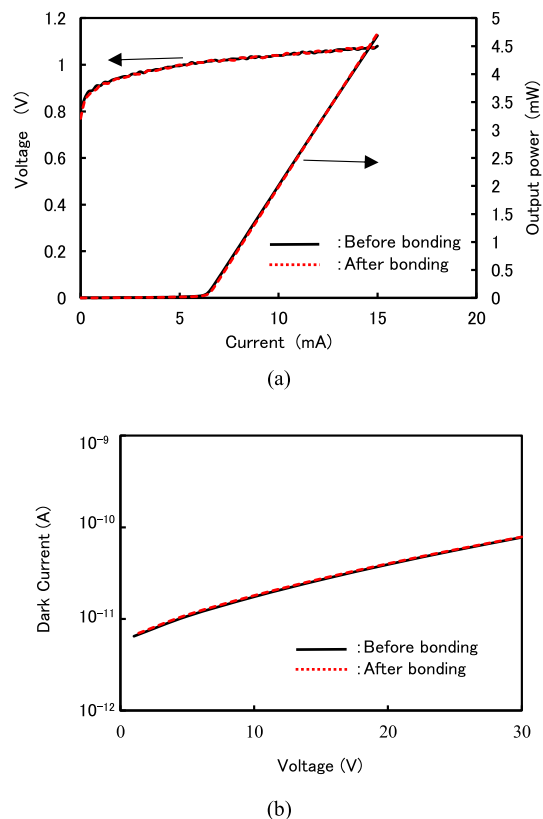


Fig. 11 Typical electro-optical characteristics of LD and PD chips before and after bonding using Ar+H₂ AP plasma treatment: (a) L-I-V characteristics, (b) Dark I-V characteristics.

be a useful technique for future optoelectronic device integration.

Acknowledgments

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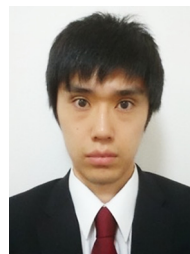


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such as micromirror array, integrated optical displacement sensors, MEMS shearing sensor and MEMS slip sensor, MEMS integrated optical blood flow sensor, integrated scanning microscope, and sensors attachable to animals and humans for network.