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Inductance and Current Distribution Extraction in Nb Multilayer Circuits with Superconductive and Resistive Components

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SUMMARY We describe a calculation tool and modeling methods to find self and mutual inductance and current distribution in superconductive multilayer circuit layouts. Accuracy of the numerical solver is discussed and compared with experimental measurements. Effects of modeling parameter selection on calculation results are shown, and we make conclusions on the selection of modeling parameters for fast but sufficiently accurate calculations when calibration methods are used. Circuit theory for the calculation of branch impedances from the output of the numerical solver is discussed, and compensation for solution difficulties is shown through example. We elaborate on the construction of extraction models for superconductive integrated circuits, with and without resistive branches. We also propose a method to calculate current distribution in a multilayer circuit with multiple bias current feed points. Finally, detailed examples are shown where the effects of stacked vias, bias pillars, coupling, ground connection stacks and ground return currents in circuit layouts for the AIST advanced process (ADP2) and standard process (STP2) are analyzed. We show that multilayer inductance and current distribution extraction in such circuits provides much more information than merely branch inductance, and can be used to improve layouts; for example through reduced coupling between conductors.

key words: *ground plane return currents, inductex, layout extraction, numerical inductance calculation, parasitic coupling*

1. Introduction

In superconducting electronic circuit design, self and mutual inductance are critical design parameters, and need to be controlled to tight margins. Even parasitic coupling between circuit loops, which inherently act as dc transformers, is important to analyze.

An analytical method to calculate the inductance of superconducting microstrip lines [1] is inadequate for all but the most basic circuit designs, so that a host of numerical methods for superconductive inductance calculation have been developed over the last three decades. The tools range from lookup-table based methods for precomputed layout sections [2] to adapted normal metal inductance calculators with fixed skin depth and kinetic inductance correction factors [3]. Later numerical tools inherently support the London equations (such as [4]), but circuit layout extraction only became practical with the introduction of the long-popular Lmeter [5], 3D-MLSI [6]–[8] and InductEx [9].

Numerical calculation models for inductance extraction need to be sufficiently fast to allow calculation in reasonable time (minutes, not days), yet also be sufficiently detailed to allow the extraction of intended and parasitic self and mutual inductances with acceptable accuracy. In earlier work we focused on modelling methods to ensure fast calculation time while retaining calculation accuracy [10], but vast improvements to the numerical engine FFH [11] now mostly makes the time constraint irrelevant. Today, model size is limited for practical purposes only by the available memory on a computer.

Full-gate extraction models that include resistance are becoming more important as process density, layout ingenuity and circuit complexity increase. Circuit operation can be ruined by almost negligible coupling [12] so that reliable full-gate inductance extraction becomes an important pillar of circuit design.

In this paper, we use InductEx [9] and the solver FFH [11] for all inductance calculations. InductEx remains the only simulator other than Lmeter [5] that can handle full-gate superconductive circuit extractions. We discuss the background to 3D inductance extraction, and show how extraction models are constructed and used to find inductances, coupling and current distribution for circuit layouts in the AIST advanced process (ADP2) [13], [14] and standard process (STP2). We also discuss developments and refinements that were necessary to model ADP2 and STP2 layouts. We then report some practical extraction results and the improvements thus enabled in circuit design. These improvements would be very difficult to realize without the analysis methods and tools presented here.

2. Calculation of Branch Impedances for a Network

The numerical solver FFH [11] calculates current density in every segment of a three-dimensional model when one port connected to some structures in the model is excited with 1 Volt at a specified frequency. The segments represent all conducting objects, and may be resistive or superconductive. Resistive segments have an associated conductance parameter in Siemens per unit length, and superconductive segments have an associated London penetration depth.

From current density in every segment, the total current at every port can be computed when any port in a multi-port network such as that shown in Fig. 1 is excited. In the example shown here, the four branches each have inductance and resistance, and there are four meshes. There are also four ports, although larger circuits mostly have fewer ports than

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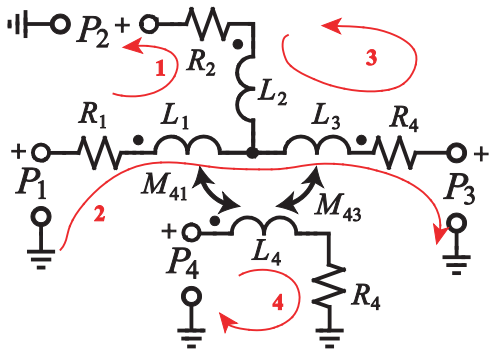

Fig. 1 Multi-port circuit schematic with inductive and resistive branches and coupling. There are four meshes to which Kirchhoff's voltage law can be applied.

meshes.

Branch impedance is solved from circuit theory. For every excited port, when all other ports are zero volt sources (short-circuited), Kirchhoff voltage loops can be constructed for every mesh as long as there are sufficient ports to enable us to find every branch current. In this way, a system of linear equations can be constructed so that

$$\mathbf{b} = \mathbf{A}\mathbf{x}, \tag{1}$$

where **b** is column vector holding loop voltages, **A** is a matrix with a row for every voltage loop and a column entry (derived from branch currents) for every impedance or mutual inductance. The column vector **x** holds the unknown impedance and mutual inductance values.

The system in Eq. (1) can be overdetermined (more equations than unknowns), exactly determined or undetermined, although it is mostly overdetermined in systems with more than 4 or 5 impedances. Use of the singular value decomposition (SVD) is an effective method to solve Eq. (1) in all these cases.

In InductEx, we use Lapack functions [15] to solve the linear systems of equations. Due to the complex impedance and complex branch currents, it is very efficient to use matrices and vectors of complex values in Eq. (1), so that the real components of **x** denote branch resistance, and the imaginary parts of **x** denote the reactive impedance (inductance multiplied by excitation frequency). This can be solved with the double precision complex Lapack function zgelsd, but we report here that results are only reliable when there is no mutual inductance.

This can be demonstrated through example. We can calculate the port currents for the circuit in Fig. 1 if the element values are as shown in Table 1, and use these currents in Eq. (1) to solve **x**. The solution with complex matrices, also shown in Table 1, is inaccurate for the inductance values. The reason is clear from the results for the mutual inductance, which contain real (resistive) parts. This only occurs if there is resistance and mutual inductance in a network (and is therefore not a concern for purely inductive circuits), but a generically reliable solution demands that the real part of mutual inductance be forced to zero.

Table 1 Solutions to branch impedance and mutual inductance for an example problem calculated with real and complex matrix formulations.

Elements	Example values	Solved with complex matrices	Solved with real matrices
$R_1 + L_1$	4 Ω + 1 pH	4 Ω + 0.89 pH	4 Ω + 1 pH
$R_2 + L_2$	3 Ω + 2 pH	3 Ω + 2.05 pH	3 Ω + 2 pH
$R_3 + L_3$	2 Ω + 3 pH	2 Ω + 2.91 pH	2 Ω + 3 pH
$R_4 + L_4$	1 Ω + 4 pH	1 Ω + 3.97 pH	1 Ω + 4 pH
M_{41}	+0.5 pH	-0.13 Ω + 0.504 pH	+0.5 pH
M_{43}	-0.4 pH	0.1 Ω - 0.404 pH	-0.4 pH

We accomplish this by using real matrices only, and rewriting the matrices in Eq. (1) to represent real and imaginary components of every variable as separate real entries. The number of rows in voltage vector **b** and matrix **A** doubles, with every odd row dedicated to the real part of a voltage loop and every even row to the imaginary part of a voltage loop. The vector **x** is constructed to hold all branch impedance values first, with the real (resistive) part in odd rows and the corresponding imaginary (reactive) part in the following even rows. Only the imaginary parts of all mutual inductances are appended to the end. The same pattern is reflected in the rows of matrix **A**. In order to support extraction of circuit models with resistance and coupling such as Adiabatic Quantum Flux Parametron (AQFP) cells [16], we have now improved InductEx to use the double precision real Lapack function dgelsd to solve the purely real matrices. For the example problem in Fig. 1, the results exactly match the example values, as shown in Table 1.

3. Numerical Models and Calculation Accuracy

3.1 Accuracy

Before numerical inductance extraction methods are used for circuit design, it is necessary to gain an understanding of the quality of calculation results when these are compared to experimental measurements, and how variations in modeling parameters influence calculation results.

The quality of calculation results are easy to assess, because inductance can be measured accurately through SQUID modulation [17] and the results compared to calculations for numerical models of such SQUIDs. We have fabricated several inductive structures in ADP2 to calculate line inductance [10] as well as via inductance and coupling [18], [19].

For a selected set of modeling parameters such as segment size and ground plane cropping distance, an artificial set of process parameters (such as layer penetration depth and thickness) can be found through calibration (using the methods described in [20]) to yield inductance calculations that are within 2.5% of experimental measurements over many chips and wafers in a given process. We did such a calibration for ADP2 [10], which delivers calculation results that have less than 1.75% root mean square error (RMSE) to experimental measurements for layers above the main

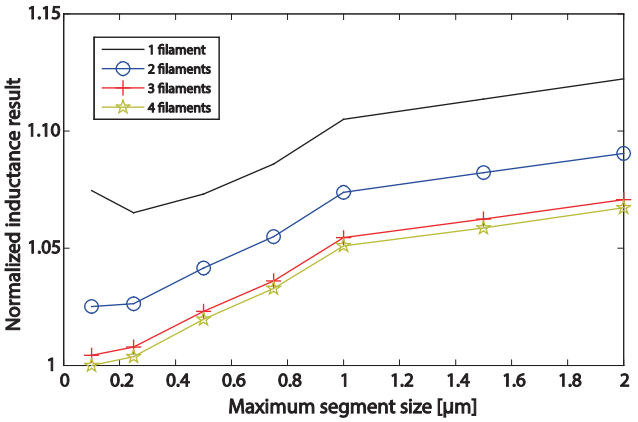

Fig. 2 Normalized inductance calculation result for an ADP2 microstrip line in layer M9 above ground as maximum segment size and filament subdivision are changed. Linewidth is 2 μm.

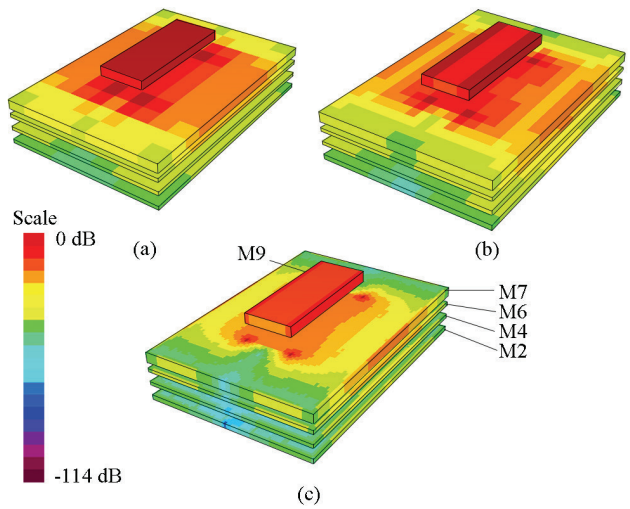

Fig. 3 Calculated current density modulus of a 5 μm long, 2 μm wide microstrip line above ground in ADP2 if the calculation model is segmented with a maximum segment size of (a) 1 μm, (b) 0.5 μm and (c) 0.1 μm. Scale is 6 dB per color, relative to largest value.

ground plane. Our calibrated calculations have better than 2.25% RMSE when the passive transmission line layers M3 and M5 are included for ADP2 (see the device structure in Fig. 1 of [21]).

However, calculation accuracy depends strongly on model accuracy, so that it is crucial to include vertical via segments and the modeling of ground contact (GC [21]) stacks for multilayer processes. Segment size and the number of height filaments into which layers are subdivided also have a strong influence on calculation results, as we show in Fig. 2 for a microstrip line above ground in ADP2. The reason for these variations in calculation results becomes evident when the calculated current density throughout the calculation model is examined for different segment sizes (see Fig. 3) and different filament counts (see Fig. 4). Calculation results approach an asymptotic value when segments are roughly the same size as the penetration depth (in the order of 0.1 μm for Nb thin films), and filament count equals or exceeds layer thickness divided by penetration depth. With such fine segmentation, higher current flow near line edges and near the top of the ground plane is better accounted for, but this comes at a significant cost in terms of computing resources required for full-circuit analysis. For practical purposes, we select a reasonable segment size and use calibration to reduce the inaccuracy of calculation results. It follows then that if segment size is changed, a recalibration may be necessary. For ADP2, we use the modeling parameters listed in Table 2. Calibrated process parameters are listed in [10], and these are contained in a technology definition file together with the modeling parameters.

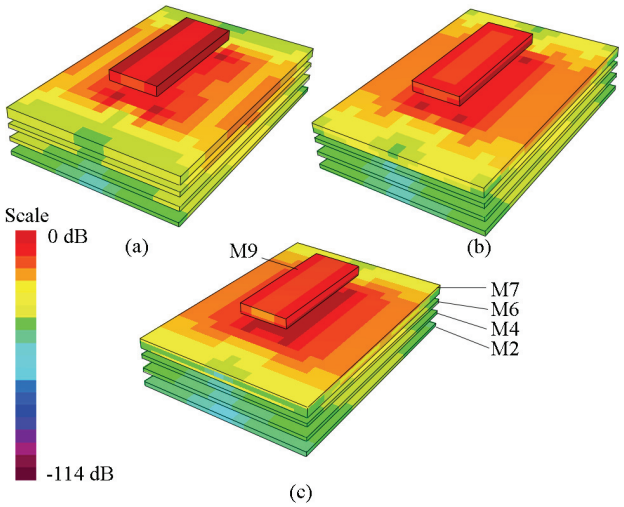

Fig. 4 Calculated current density modulus of a 5 μm long, 2 μm wide microstrip line above ground in ADP2 if the calculation model is segmented with a maximum segment size of 0.5 μm and layers M7 and M9 are subdivided into (a) 1 height filament, (b) 2 height filaments and (c) 3 height filaments. Scale is 6 dB per color, relative to largest value.

Table 2 InductEx modeling parameters for calibrated calculations in ADP2.

Parameter	Value
M9 height filaments	2
M8 height filaments	2
M7 height filaments	3
M1-M6 height filaments	1
Maximum segment dimensions	1.0 µm

3.2 Circuit Modeling for Extraction

With numerical calculations, results can be no better than the models used, so that careful attention to model accuracy is required when sensitive circuit extractions are done. InductEx builds a three-dimensional calculation structure from a layout file and a selected technology definition file. The designer declares excitation ports and a corresponding circuit netlist.

For current density calculations, all that is required is the addition of an excitation port. However, for inductance

and resistance extraction, a circuit netlist for the network must be supplied. The netlist must contain a sufficient number of ports to allow the unique calculation of current in every branch of the network.

It is important to note that a solution to the linear system of equations in Eq. (1) yields a set of component values for the supplied netlist that would cause the same port currents to flow (when excited with the same port voltages) as that found by the numerical solver. If the netlist does not accurately represent the actual layout, for instance in terms of position of connections or coupling, then it follows that the extracted results may be severely skewed. For instance, if we return to the example in Fig. 1 and Table 1 and omit the mutual inductances M_{41} and M_{43} from the circuit netlist (and consequently from the linear system of equations in Eq. (1)), the solutions for L_1, L_2, L_3 and L_4 become 0.85 pH, 2.07 pH, 2.86 pH and 3.31 pH respectively (significant errors). However, a circuit with these inductance values and no coupling will have the exact same branch currents as the original circuit.

4. Extraction Models

Although there are many ways to manipulate layouts, for instance to reduce segment count and improve calculation speed, a straightforward extraction requires only that a suitable circuit netlist containing impedances, mutual inductances and ports is created, and that the ports are identified through text labels on a circuit layout.

InductEx limits components to inductors (which may have resistive parts and represent impedances), coupling elements and ports. Successful solution of the system of linear equations in Eq. (1) requires every branch to have one impedance element. Valid and invalid schematics are shown in Fig. 5.

As an example, consider the AND gate for ADP2, of which the layout is shown in Fig. 2 of [21]. A simulation circuit schematic for a section of an input to the AND gate is shown in Fig. 6. Element values are irrelevant. The schematic shows all standard possibilities for port declarations when the inductance of a circuit network is extracted: junctions, input/output pins and resistive branches.

For most extractions, resistive components are ignored (through a setting in the technology definition file that prohibits segmentation of resistive layers) so that resistive branches can be omitted. A circuit schematic of the netlist for extraction is shown in Fig. 7 (a). Ports are declared on the input pin A (at the edge of the layout) and the junction J_1 (inside the junction area in the layout), as shown in Fig. 8 (a). In order to calculate inductances L_1 and L_2 (rather than just the combination $L_1 + L_2$), the branch containing L_{RB1} needs to be included in the netlist. The port P_{RB1} should then be

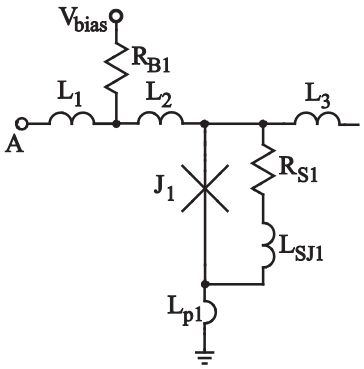

Fig. 6 Circuit schematic for part of an input section of a CONNECT AND gate for ADP2.

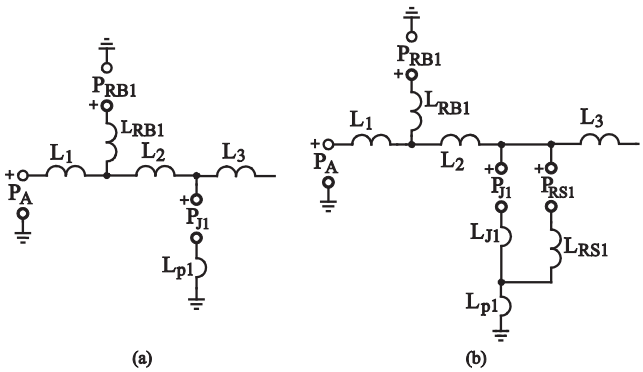

Fig. 7 Schematics of InductEx netlists for part of an input section of a CONNECT AND gate in ADP2 if (a) resistors are neglected for a purely inductive extracted network and (b) resistors are included for extraction.

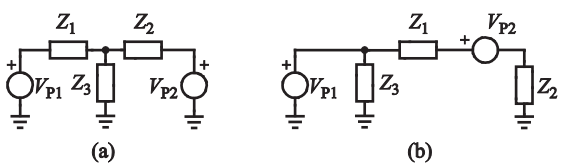

Fig. 5 Example of (a) valid InductEx circuit schematic with one impedance element per branch, and (b) invalid InductEx circuit schematic no impedance elements in the branch containing V_{P1} and two impedance elements in the branch containing V_{P2}.

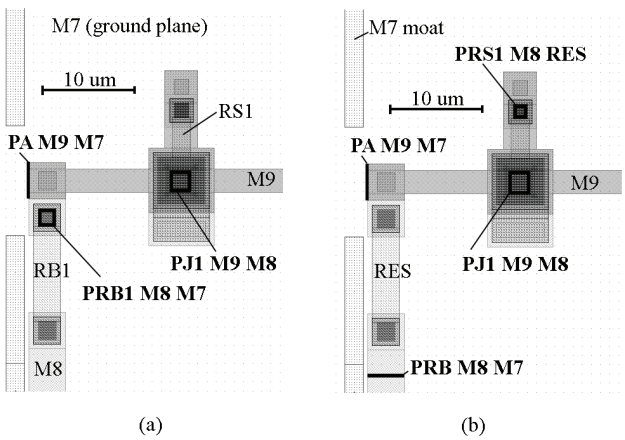

Fig. 8 Layout of an input section of a CONNECT AND gate in ADP2 with InductEx port declarations (in bold text) if (a) resistors are neglected for a purely inductive extracted network and (b) resistors are included for extraction.

placed anywhere between the resistor and the point where the L_{RB1} branch meets L_1 and L_2 in the layout. Each branch has one inductor.

When resistive components are included, the netlist must contain resistive branches. A circuit schematic for this case is shown in Fig. 7 (b). The port P_{RB1} can now be defined at the edge of the cell layout where it connects to the bias pillar, while an extra port P_{RS1} is required for the branch containing R_{S1}. This port is typically defined on one of the vias that connect the resistor to the nearest superconductive layer, as shown in Fig. 8 (b). Polarity must match that of the port in the netlist, otherwise the system of equations in Eq. (1) (and thus the solution) is incorrect. InductEx handles the inductors as impedances that have inductive and resistive parts.

5. Practical Calculation Examples

5.1 Stacked Vias and Grounding Methods

The three-dimensional extraction capabilities developed for InductEx to handle self and mutual inductance in complicated layouts also made it possible, for the first time, to calculate the inductance of stacked vias in the ADP2 process and analyze the coupling between lines that thread ground planes through stacked vias [18], [19]. We were thus able to calculate, and confirm through experimental measurements, inductance of between 0.4 pH and 0.9 pH for typical stacked vias from layer M9 to lower passive transmission line layers M5 and M3 [18]. An important result is that via inductance is influenced by the placement of ground contact stacks that connect the different ground planes, because ground contacts determine return current paths.

The effect of ground contact placement is even more evident when coupling between lines that are on different, shielded wiring layers but that connect through stacked vias are measured and calculated. In such an experiment [18], shown here in Fig. 9 (a), we obtained a significant coupling factor (0.086 calculated, 0.082 measured) between lines that are supposed to be shielded from each other. We can analyze the origin of this coupling by considering the distribution of current when a control line is energized. With InductEx we build a single-port circuit model, as shown in Fig. 9 (b), and excite the current-carrying control line at port P_1. Short circuits to ground in the schematic are marked as zero-volt electrical connections on the layout and processed as such by InductEx. Current density in every segment of the calculation model is then calculated. For viewing purposes, we sum the magnitude of current density at every node (composed of real and imaginary components) as vectors in the x, y and z directions and then find the modulus.

The calculation results in Fig. 10 shows that substantial return current from the energized line flows across the ground planes above and below the victim loop to the ground contacts, which results in coupling.

The unwanted coupling can be reduced if return current paths are tightened, and the most obvious improvement is to move the ground contacts next to the stacked vias. We have shown [19] that in-line placement is better than perpendicular placement.

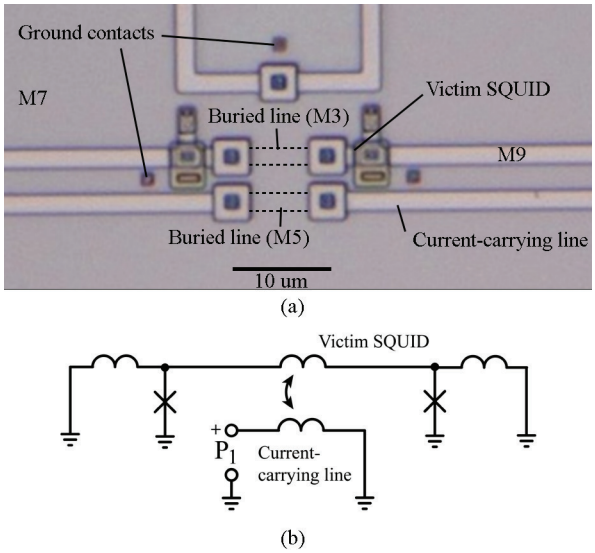

Fig. 9 (a) Microphotograph of a test circuit for measuring the coupling between lines that have ground plane shielded sections in M3 and M5 [18], and (b) schematic diagram of the current distribution calculation model with one excited port and the victim structure inputs and outputs shorted to ground.

The drastic tightening of ground plane current distribution is shown in Fig. 11, and the coupling reduces by almost 50% to 0.047 [19]. These results also highlight the importance of correct modeling for reliable calculations: ground connections between multiple ground planes or shield layers must be included in extraction models exactly as these are placed in layouts.

5.2 Parasitic Coupling in AQFP Gate with Resistive Branches

AQFP logic gates provide fast operation with very low energy dissipation as a result of adiabatic switching operations [22]. AQFP gates have up to now been demonstrated in the STP2 process. An AQFP cell library was built using minimalist design [16], where logic cells are designed by simply arraying several types of building blocks. Using the cell library, AQFP logic circuits with up to approximately 1,000 Josephson junctions have been successfully demonstrated.

AQFP cell layouts need to be carefully designed to suppress unwanted magnetic coupling between the ac clock line and the output inductance. Therefore, in previous works, we adopted superconductor magnetic shields [12] or symmetric layout [16]. In this study, we use AQFP gates with symmetric layout.

An AQFP buffer cell [16] is shown in Fig. 12. The circuit netlist for impedance and mutual inductance extraction with InductEx is shown in Fig. 13, with the shunt resistor branches (L_{S1} and L_{S2}) included. The segmented calcula-

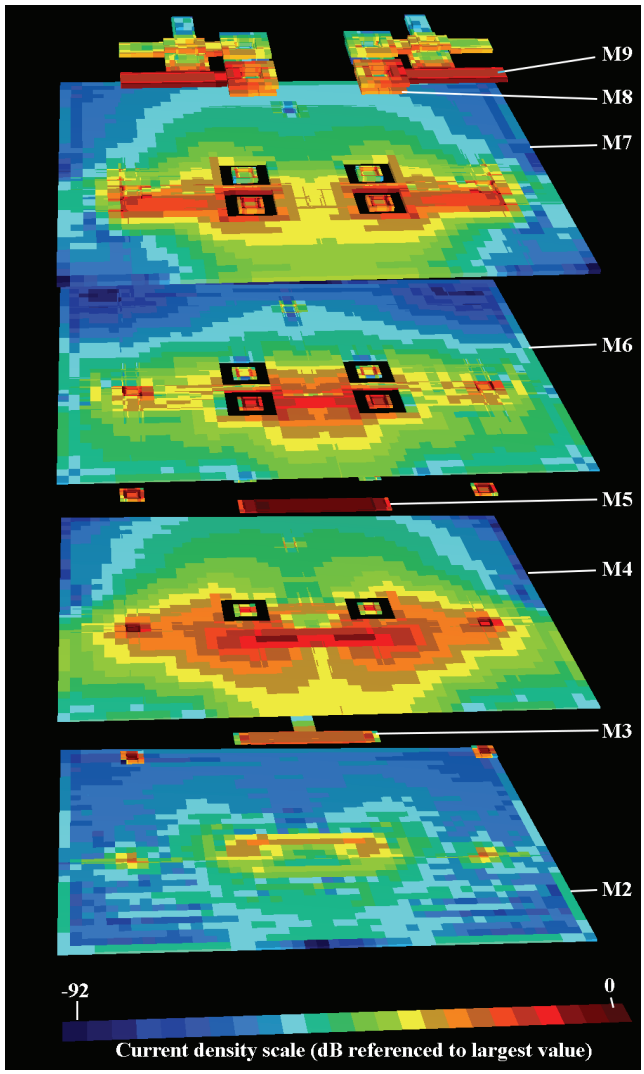

Fig. 10 Exploded rendering of modulus of current density in the calculation model of the coupling structure from Fig. 9 (a). Part of the victim loop is in M3, while part of the current-carrying line is in M5.

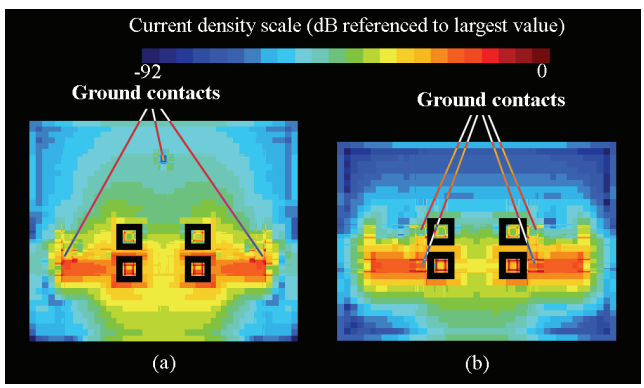

Fig. 11 Modulus of current density in the main ground plane (M7) of (a) the experimental circuit in Fig. 9 (a) and (b) the same circuit with ground contacts placed in-line next to the stacked vias.

tion model is shown in Fig. 14. The ac clock line (inductor L_x) must couple strongly to inductors L_1 and L_2, but have zero coupling with L_q and L_{out}. Inductors L_q and L_{out} should

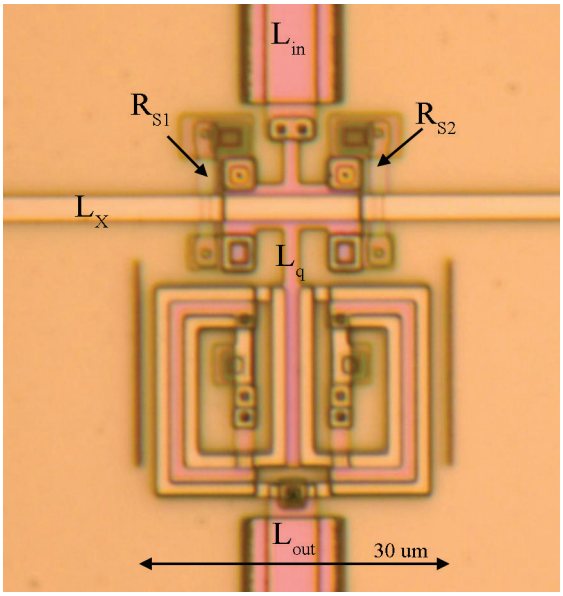

Fig. 12 Microphotograph of an AQFP buffer cell [16].

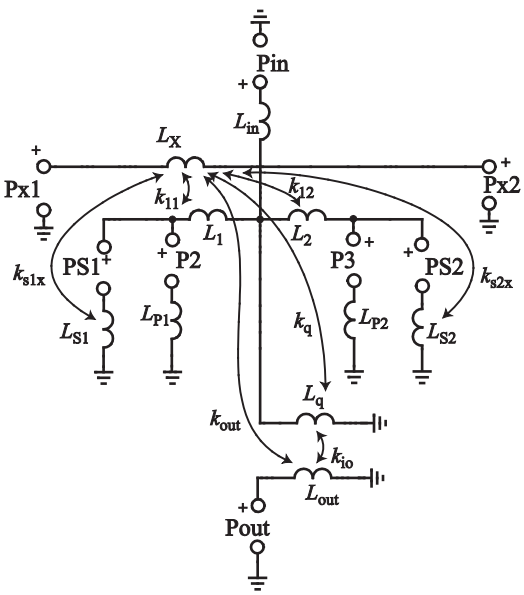

Fig. 13 Schematic diagram of InductEx circuit netlist for impedance and mutual inductance extraction for the AQFP buffer in Fig. 12.

be coupled strongly. These important mutual inductances are shown in Fig. 13, along with the coupling between L_x and the resistive branches (k_{s1x} and k_{s2x}).

With the real matrix SVD method described in Sect. 2, we find the coupling factors k_{io}, k_{11}, k_{12}, k_q and k_{out} as 0.44954, 0.2583, 0.2593, 0.0000 and 0.0000 respectively (signs are omitted).

The complex matrix method from Sect. 2 results in a 2.3% error on the inductance of branches L_{S1} and L_{S2} and gives real components in the range $10^{-5}\,\Omega$ to $10^{-4}\,\Omega$ for the mutual inductances; which confirms that the real matrix method is more reliable.

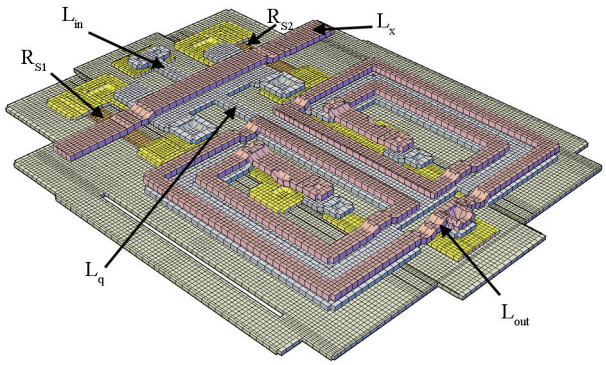

Fig. 14 Segmented numerical calculation model, created with InductEx, for impedance and mutual inductance extraction for the AQFP buffer circuit in Fig. 12.

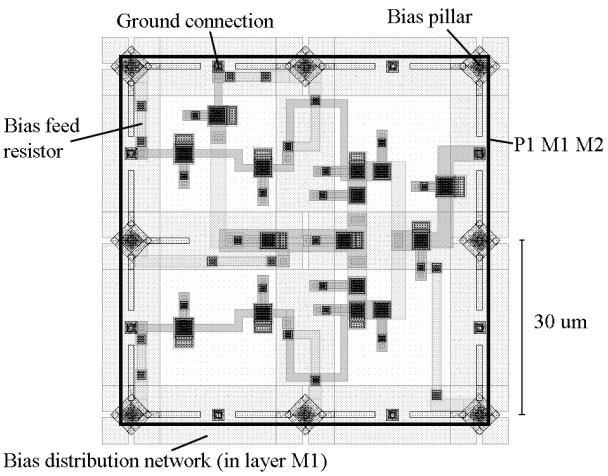

Fig. 15 Mask layout of AND gate in ADP2 cell library with port definition for the calculation of bias current distribution with InductEx.

Finally, if we are interested in coupling between other inductor combinations, more mutual inductance elements can be added to the circuit netlist in Fig. 13 until the matrix **A** in Eq. (1) becomes rank deficient. For the AQFP buffer circuit, rank deficiency occurs when we have 18 or more mutual inductances in the netlist model, after which the extracted results become unreliable.

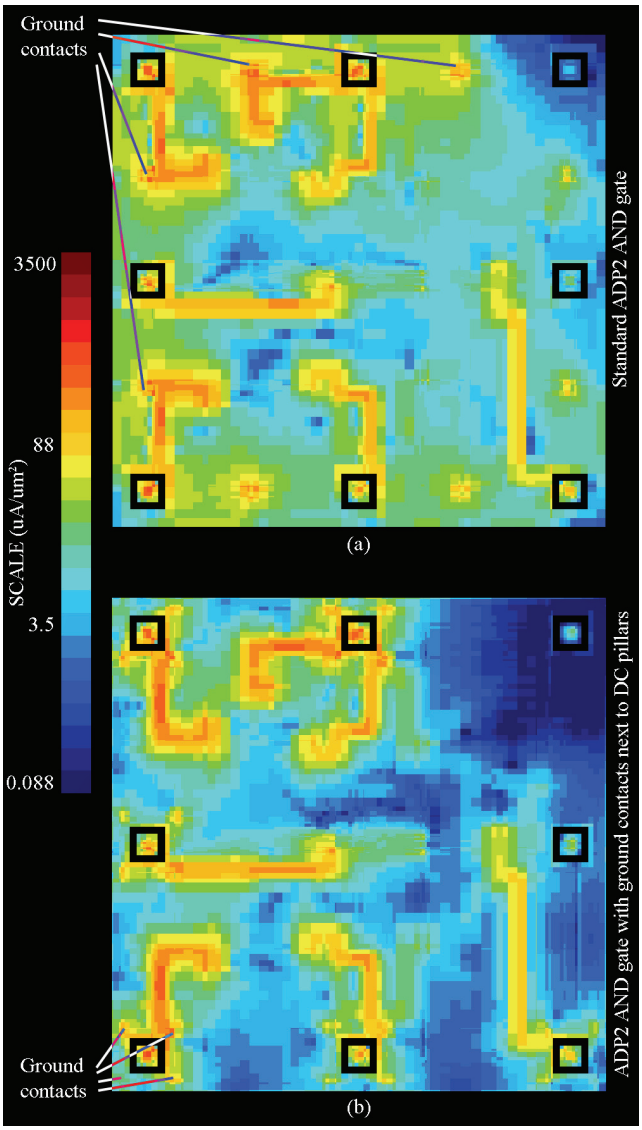

Fig. 16 Modulus of current density in the main ground plane (M7) of (a) an AND gate in the ADP2 cell library using the standard device structure [21] when the cell is biased with 2.5 mV, and (b) the same AND gate with the same bias, but with the ground contact stacks placed around the dc bias pillars as proposed in [19].

5.3 Ground Return Currents in a CONNECT AND Gate

The CONNECT AND gate in the AIST ADP2 process (discussed in [21]) has multiple dc supply lines, which limits the maximum current in any dc bias pillar and assures a more even distribution of ground plane return current.

Inductance extraction for the full AND gate circuit netlist is straightforward with InductEx, but we propose a method here to extract ground return currents and evaluate the biasing strategy.

For current density calculation, as discussed in Sect. 5.1, we need only a single excitation port. This should be placed so that it feeds all bias currents. The circuit can then be modeled as single impedance in parallel to the excitation port.

For the model, we assume that there are no static leakage currents through gate inputs and outputs, and these are left open circuit. Junctions are modelled as vias, which disregards the junction inductance, but we contend that the effect on bias current distribution is small enough not to invalidate the current distribution calculations.

Although bias current is dc, the formulation for superconductivity in FFH does not allow solution at 0 rad/s. We thus solve current distribution at an arbitrary ac frequency that is low enough so that the skin depth of the resistive layers is much larger than any resistor dimensions.

The final modeling choice is the placement of the excitation port in the layout. In isolation we do not know how

currents will distribute outside the AND gate cell area and from which direction in the dc bias grid most of the bias current will arrive. However, if the cell is part of a larger network of tiled cells, we assume that bias current can arrive from any direction. We thus create the port as a thin rectangular equipotential strip around the entire cell, as shown in Fig. 15, and connect the positive terminal to the dc power plane (M1) and the negative terminal to the closest ground plane (M2) to this power plane.

FFH solves current density for an excitation voltage of 1 V, while the actual bias voltage is 2.5 mV. We thus scale all calculated current density values down by a factor 400 to obtain the current density scale in Fig. 16 (a). The results show that current density over the ground plane is high, and is crowded near the GC stacks instead of only underneath the bias lines.

An improved device structure layout was proposed in [19], where GC stacks are placed in close proximity around the dc bias pillars. This needs to be done in a way that does not impede passive transmission line routing below the cell. As a result of the analysis capabilities described in this paper, we suggest as a further improvement (over that described in [19]) that the GC stacks in the center of each cell side be removed completely. Such changes to the device structure would require redesign of the routing architecture underneath cells, but the advantage is clear. With such a grounding strategy, the ground plane current is reduced significantly everywhere except underneath the bias lines, as shown in Fig. 16 (b).

6. Conclusion

The development of three-dimensional inductance and current distribution calculation methods (both in terms of field solvers and modeling methods) for multilayer integrated circuit structures has given us new capabilities in circuit layout. Apart from just extracting self and mutual inductance networks for layouts that might have complicated structures, holes and isolated ground planes, we can now also determine and eliminate parasitic coupling that would otherwise destroy circuit operation. Furthermore we showed in this paper that the visualization of current distribution, especially in ground planes, now makes it possible to identify sources of parasitic coupling and reduce such effects.

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References

[1] W.H. Chang, "The inductance of a superconducting strip transmission line," J. Appl. Phys., vol.50, no.12, pp.8129–8134, 1979.
[2] K. Gaj, Q.P. Herr, V. Adler, A. Krasniewski, E.G. Friedman, and M.J. Feldman, "Tools for the computer-aided design of multigigahertz superconducting digital circuits," IEEE Trans. Appl. Supercond., vol.9, no.1, pp.18–38, 1999.
[3] Z. Du, S.R. Whiteley, and T. Van Duzer, "Inductance calculation of 3D superconducting structures," Appl. Supercond., vol.6, no.10-12, pp.519–523, 1998.
[4] G. Hildebrandt and F.H. Uhlmann, "Inductance calculation for integrated superconducting structures by minimizing free energy," IEEE Trans. Appl. Supercond., vol.5, no.2, pp.2766–2769, 1995.
[5] P.I. Bunyk and S.V. Rylov, "Automated calculation of mutual inductance matrices of multilayer superconductor integrated circuits," Ext. Abs. ISEC, p.62, 1993.
[6] M.M. Khapaev, A.Y. Kidiyarova-Shevchenko, P. Magnelind, and M.Y. Kupriyanov, "3D-MLSI: Software package for inductance calculation in multilayer superconducting integrated circuits," IEEE Trans. Appl. Supercond., vol.11, no.1, pp.1090–1093, 2001.
[7] M.M. Khapaev, M.Y. Kupriyanov, E. Goldobin, and M. Siegel, "Current distribution simulation for superconducting multi-layered structures," Supercond. Sci. Technol., vol.16, no.1, pp.24–27, 2003.
[8] M.M. Khapaev and M.Y. Kupriyanov, "Inductance extraction of superconductor structures with internal current sources," Supercond. Sci. Technol., vol.28, no.5, 055013, 2015.
[9] C.J. Fourie, O. Wetzstein, T. Ortlepp, and J. Kunert, "Three-dimensional multi-terminal superconductive integrated circuit inductance extraction," Supercond. Sci. Technol., vol.24, no.12, 125015, 2011.
[10] C.J. Fourie, A. Takahashi, and N. Yoshikawa, "Fast and accurate inductance and coupling calculation for a multi-layer Nb process," Supercond. Sci. Technol., vol.28, no.3, 035013, 2015.
[11] K. Jackman and C.J. Fourie, "Fast multicore FastHenry and a tetrahedral modeling method for inductance extraction of complex 3D geometries," Proc. 2015 IEEE Superconductive Electronics Conference (ISEC2015), Nagoya, Japan, pp.1–3, 2015.
[12] K. Inoue, N. Takeuchi, T. Narama, Y. Yamanashi, and N. Yoshikawa, "Design and demonstration of adiabatic quantum-flux-parametron logic circuits with superconductor magnetic shields," Supercond. Sci. Technol., vol.28, no.4, p.045020, 2015.
[13] S. Nagasawa, T. Satoh, K. Hinode, Y. Kitagawa, M. Hidaka, H. Akaike, A. Fujimaki, K. Takagi, N. Takagi, and N. Yoshikawa, "New Nb multi-layer fabrication process for large-scale SFQ circuits," Physica C, vol.469, no.15-20, pp.1578–1584, 2009.
[14] S. Nagasawa, K. Hinode, T. Satoh, M. Hidaka, H. Akaike, A. Fujimaki, N. Yoshikawa, K. Takagi, and N. Takagi, "Nb 9-layer fabrication process for superconducting large-scale SFQ circuits and its process evaluation," IEICE Trans. Electron., vol.E97-C, no.3, pp.132–140, 2014.
[15] E. Anderson, Z. Bai, C. Bischof, S. Blackford, J. Demmel, J.J. Dongarra, J. Du Croz, A. Greenbaum, S. Hammarling, A. McKenney, and D. Sorensen, LAPACK Users' Guide, 3rd ed. Philadelphia, PA: Society for Industrial and Applied Mathematics, 1999.
[16] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron cell library adopting minimalist design," J. Appl. Phys., vol.117, no.17, 173912, 2015.
[17] W.H. Henkels, "Accurate measurement of small inductances or penetration depths in superconductors," Appl. Phys. Lett., vol.32, no.12, pp.829–831, 1978.
[18] C.J. Fourie, X. Peng, R. Numaguchi, and N. Yoshikawa, "Inductance and coupling of stacked vias in a multilayer superconductive IC process," IEEE Trans. Appl. Supercond., vol.25, no.3, 1101104, June 2015.
[19] C.J. Fourie, S. Miyanishi, and N. Yoshikawa, "Grounding methods to reduce stray coupling in multi-layer layouts," Proc. 2015 IEEE Superconductive Electronics Conference (ISEC2015), Nagoya, Japan, pp.1–3, 2015.
[20] C.J. Fourie, "Calibration of inductance calculations to measurement data for superconductive integrated circuit processes," IEEE Trans. Appl. Supercond., vol.23, no.3, 1301305, June 2013.
[21] A. Fujimaki, M. Tanaka, R. Kasagi, K. Takagi, M. Okada, Y. Hayakawa, K. Takata, H. Akaike, N. Yoshikawa, S. Nagasawa, K.

Takagi, and N. Takagi, "Large-scale integrated circuit design based on a Nb nine-layer structure for reconfigurable data-path processors," IEICE Trans. Electron., vol.E97-C, no.3, pp.157–165, March 2014.

[22] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Thermodynamic study of energy dissipation in adiabatic superconductor logic," Phys. Rev. Appl., vol.4, no.3, p.034007, Sept. 2015.

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