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PAPER Special Section on Analog Circuit Techniques and Related Topics

A Low-Power Current-Reuse LNA for 3D Ultrasound Beamformers

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SUMMARY 3D ultrasound imagers require low-noise amplifier (LNA) with much lower power consumption and smaller chip area than conventional 2D imagers because of the huge amount of transducer channels. This paper presents a low-power small-size LNA with a novel current-reuse circuitry for 3D ultrasound imaging systems. The proposed LNA is composed of a differential common source amplifier and a source-follower driver which share the current without using inductors. The LNA was fabricated in a 0.18-μm CMOS process with only 0.0056 mm^2. The measured results show a gain of 21 dB and a bandwidth of 9 MHz. The proposed LNA achieves an average noise density of 11.3 nV/$\sqrt{\text{Hz}}$, and the 2nd harmonic distortion below −40 dBc with 0.1-Vpp input. The supply current is 85 μA with a 1.8-V power supply, which is competitive with conventional LNAs by finer CMOS process.

key words: *amplifier, current-reuse, driver, ultrasound, LNA*

1. Introduction

Ultrasound imaging systems are widely used for medical diagnosis. A 1D array probe is commonly used to obtain 2D images, but 3D imaging systems with 2D array probes have been used recently to minimize examination time and to make it easier to find a target [1]–[3]. In the conventional 1D probe, a received ultrasound signal is converted into an electrical signal at a transducer array in the handheld probe and usually transmitted to a main unit that has a beam-focusing function as shown in Fig. 1(a). However, for the 2D array probe, this function must be integrated in the probe as shown in Fig. 1(b) to avoid a too heavy transceiver cable to the main unit necessary for accommodating massive channels of the ultrasound transmitter and receiver. Fig. 2 shows an architecture of an ultrasound beamformer IC. The front-end transducer is connected to a low-noise amplifier (LNA) through a transmitter (TX) and receiver (RX) switch (TR-SW) [4]. A received ultrasound signal is converted into an electrical signal, amplified in the LNA stage, and sent to a variable delay stage and a subsequent adder stage. The variable delay stage decides the focus point of the ultrasound image. In such a 2D matrix probe, the power and area budget given to individual channels is significantly limited be-

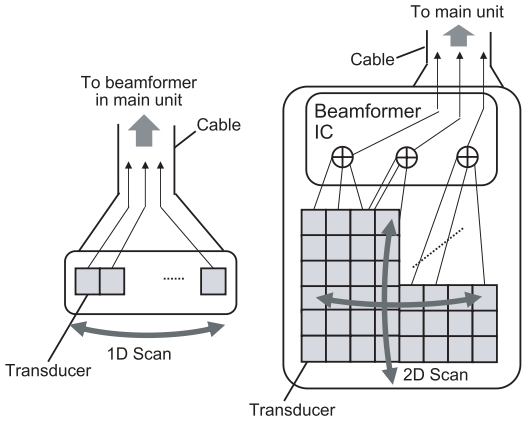

Fig. 1 Probes for ultrasound imagers. (a) 1D array for 2D imager. (b) 2D array for 3D imager.

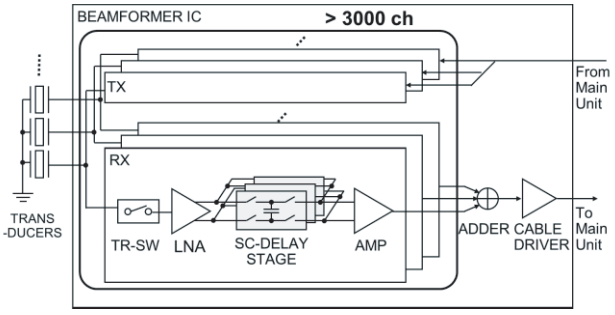

Fig. 2 Architecture of ultrasound beamformer IC.

cause 1,000 to 10,000 channels must be integrated in a small hand-held probe. For example, to achieve a power consumption of 1 W with 3,000 channels, assuming the TX and RX budget to be 1:1, the power consumption of an individual receiver channel must be < 150 μW, which is further divided into each of the stages that constitute the RX channel. Nevertheless, additional noise at the LNA must be sufficiently small so that very weak signal from deep structures in the human body can be captured. Another crucial requirement for the LNA is that it must drive the delay stage, which is composed of a high-speed parallel switched capacitor (SC) circuit. Furthermore, 2nd harmonic distortion (2HD) of the LNA must also be suppressed to a specified level because 2nd harmonic ultrasound signals are used in some of the imaging modes used for diagnostic procedures.

In some low-power LNAs used for RF applications,

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the current-reuse technique is known as an attractive solution that reduces power consumption [5]–[7]. The current-reuse architecture of RF-LNAs usually uses an inductor element to isolate between the functional stages. However, the frequency band of medical ultrasound imagers is usually around 1–10 MHz, which is much lower than that of RF-LNAs. The inductor size becomes prohibitively large to be applied for this frequency band. Some other current-reuse architectures for LNA were also proposed to increase transconductance or reduce power consumption of several receiver channels without using inductors [8]–[10]. However, a current-reuse architecture optimized for driving switched capacitor circuit in 2D array probe has not been proposed.

In this paper, a low-power small-size current-reuse LNA without an inductor is proposed and verified by the prototype measurement for ultrasound beamformer ICs. The proposed current-reuse circuitry enables independent optimization of both a high gain at the amplifier stage and low output impedance at the driver stage with halved power consumption. A differential architecture is employed to suppress 2HD. In addition, both amplifier and driver stages are NMOS-based for even better power and area efficiency. This paper is organized as follows. In Sect. 2, the architecture and operating principle of the circuit are described. The stability is analyzed in Sect. 3. The circuit is verified by measurement in Sect. 4, and a comparison with other low-power LNAs for ultrasound systems is shown. Section 5 concludes the paper.

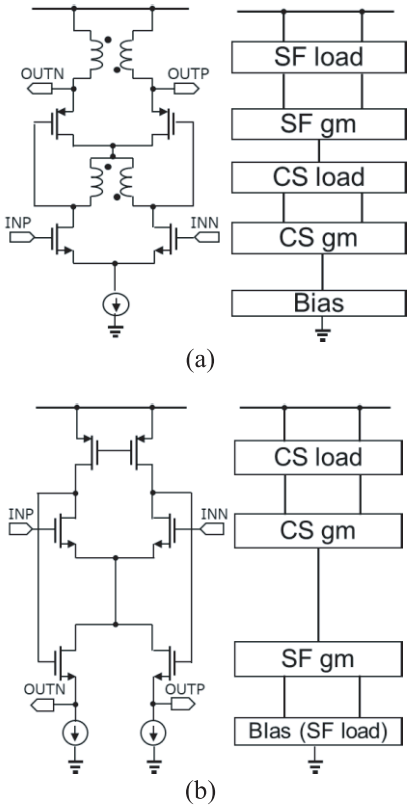

Fig. 3 Architecture of conventional [5] and proposed current-reuse LNA. (a) Conventional LNA. (b) Proposed LNA.

2. Proposed Architecture of LNA

Figure 3(a) shows a conventional current-reuse RF-LNA with a driver stage [5]. This LNA uses two inductors as a load without DC drop and the structure is composed of five-stacked functional elements as described in right-side of Fig. 3(a). The differential architecture is suitable for the cancellation of 2HD required by the ultrasound system. However, inductors for load functions are not suitable for the frequency range of the ultrasound system as mentioned previously. On the other hand, the voltage headroom is sacrificed if inductors are replaced by MOS transistors. Thus, Fig. 3(b) shows a proposed inductor-less current-reuse LNA with a driver stage. A differential common-source (CS) amplifier stage is located on top of a source-follower (SF) driver stage in order to reuse the bias current. The common drain nodes of the transistors in the driver stage and the common source nodes of the transistors in the amplifier stage are connected directly as an AC ground without using an inductor. This structure also reduces the number of stacked elements from five to four, which provides larger voltage headroom while all loads are implemented with MOS transistors. Another significant feature is that NMOS transistors are used for input of the source follower by flipping the PMOS counterpart in [5]. Because a required size of NMOS transistor is smaller than PMOS to obtain same transconductance, the load capacitances of the amplifier stage are reduced. Therefore, the further power saving is attained to achieve the required bandwidth as well as the area saving.

In Fig. 4, a full schematic of the proposed LNA is shown. For the amplifier stage, the driver stage is seen as a high-impedance current source because the current flow through the junction node (P) is kept constant set by the bottom transistors M7 and M8. The impedance of the current source is determined by the channel-length modulation effect of M7 and M8. When the input signal (v_{IN}) is single-ended (as required by ultrasound imagers) and the gate voltage of M2 is a fixed DC bias as shown in Fig. 4, the voltage of junction node P (v_P) follows the same polarity as v_{IN} because the common-mode input component appears at this node. The drain current of M2 is also generated by the swing of v_P. This results in the positive output of the 1st stage (v_{O1P}) having the same polarity as v_{IN} and the negative output having the opposite polarity. At the source-follower stage, the voltage of V_{O1P} and V_{O1N} is shifted by (V_{TH} + V_{OV}) with M3 and M4. Here, V_{TH} and V_{OV} are the threshold voltage and over-drive voltage of the MOS transistors, respectively. The body terminals of M3 and M4 are connected to their source terminals to avoid the body effect. One of the important points of this structure is that it enables a high gain with a low output impedance because the maximum gain is determined by the output impedance of the 1st amplifier stage, and a low output impedance is achieved in the driver stage.

The proposed stacked architecture needs to be care-

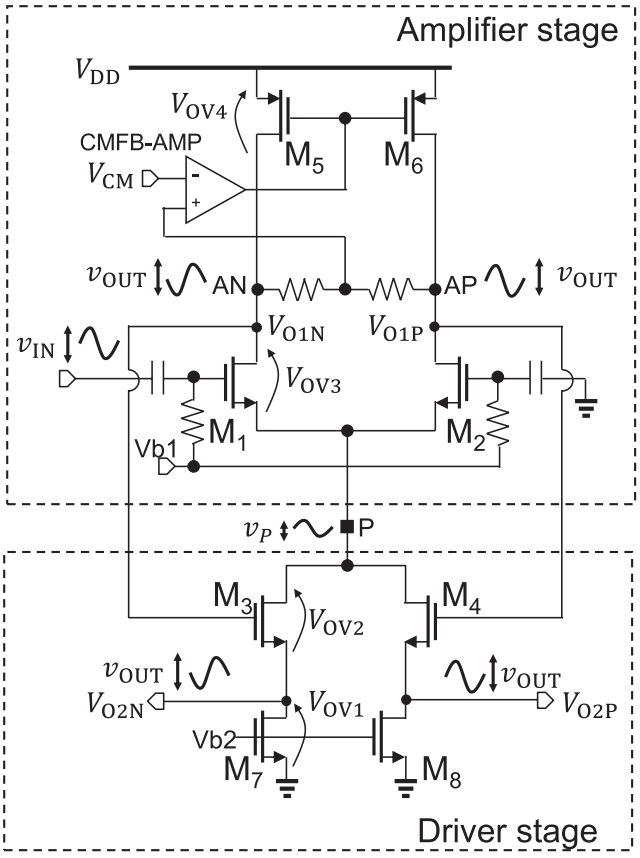

Fig. 4 Schematic of proposed LNA circuit.

fully designed in consideration of the bias point and voltage swing at each node. A simple guideline for the design is given as follows. As previously described, the polarity of the voltage swing at the drain and source is the same for M2 and M4 but opposite for M1 and M3. Therefore, the constraint for operating the transistors in the saturation region for M1 and M3 is more stringent than that for M2 and M4. The condition for operating in the saturation region for M1, M3, and M5 is described as (1) and (2).

$$V_{OV1} + v_{OUT} + V_{OV2} + v_P + V_{OV3} + v_{OUT} + V_{OV4} < V_{DD} \quad (1)$$

$$v_P = \frac{v_{IN}}{2}, \quad v_{OUT} = \frac{G}{2} v_{IN} \quad (2)$$

Here, V_{OVX} (X=1~4) is over-drive voltage of each transistor as denoted in Fig. 4 and v_{OUT}, v_P, and v_{IN} are voltage swing at the output of driver, node P and input of amplifier stage respectively. G is the differential voltage gain of the amplifier. In (1), the voltage gain of the source follower (M3, M4) was approximately regarded as one, which is reasonable when the body terminal is connected to the source terminal. (1) and (2) result in the following Eq. (3).

$$V_{OV1} + \left(G + \frac{1}{2}\right) v_{IN} + V_{OV2} + V_{OV3} + V_{OV4} < V_{DD} \quad (3)$$

When applying $V_{DD} = 1.8$ V, $V_{OVX} = 0.2$ V, and G = 10, (3) results in $v_{IN} < 100$ mV, giving upper limit of the input range. We also need to consider the voltage shift by the source follower as follows.

$$V_{O2} = V_{O1} - V_{TH} - V_{OV2} \quad (4)$$

Due to this relation, the 1st-stage common-mode level (V_{O1}) is determined by the output common-mode level (V_{O2}). Also, the voltage swing at junction node P and the output node is sandwiched by V_{O1} and V_{O2}, which gives Eq. (5) and hence (6) by combining with (4).

$$V_{O2} + \frac{v_{OUT}}{2} + V_{OV2} + v_P < V_{O1} - \frac{v_{OUT}}{2} - V_{OV3} \quad (5)$$

$$v_{OUT} < \frac{V_{TH} - V_{OV3}}{1 + 1/G} \approx V_{TH} - V_{OV3} \quad (6)$$

The Eq. (6) means that the maximum output swing is determined by the threshold voltage of M3 and M4. Thus, to achieve the maximum swing of $v_{OUT} = 0.5$ V, the threshold voltage needs to be equal to or larger than 0.7 V. From these analyses, when $V_{OVX} = 0.2$ V and $V_{TH} = 0.7$ V, the appropriate bias voltage can be decided to be about $V_{O2} = 0.45$ V and $V_{O1} = 1.35$ V. Here, V_{O1} is controlled to be the same voltage as common-mode bias V_{CM} by a common-mode-feedback amplifier (CMFB-AMP) and load PMOS transistors (M5, M6) as shown in Fig. 4. Once V_{O1} is set by V_{CM}, V_{O2} is also biased automatically with the relationships in accordance with Eq. (4).

Next, the effects of process, voltage and temperature variations are discussed. The proposed LNA is affected by variation of the threshold voltage of MOS transistors (due to process or temperature variations) more significantly than by variation of the over-drive voltage (V_{OVX}), as long as the bias circuit is designed to keep the current constant against the variations. As shown in (6), the maximum output swing is determined by the threshold voltage and becomes smaller with the lower threshold voltage. Therefore, the output range and hence the input range of the proposed LNA need to be set by considering the minimum threshold voltage under the variations. In addition, when the power supply voltage decreases, the input range can be reduced based on (3).

It should also be noted that the source follower serves not only as a driver but also as a level shifter. The delay stage includes parallel samplers which are composed of MOS switches and capacitors as shown in Fig. 5(a). A bandwidth of the samplers is determined by an output impedance (R_{OUT}) of the LNA, an on-resistance of the sampling switch (R_{SW}) and a capacitance of the sampling capacitor in each sampler. The low-level voltage (V_{O2}) brought by the level-shift function of the source follower makes it possible to use NMOS switches instead of CMOS switches because the on-resistance of NMOS is lower when the signal stays in low level as shown in Fig. 5(b). This is additional advantage for reducing the area of the ultrasound beamformer IC since there are many sampling switches in the delay stage.

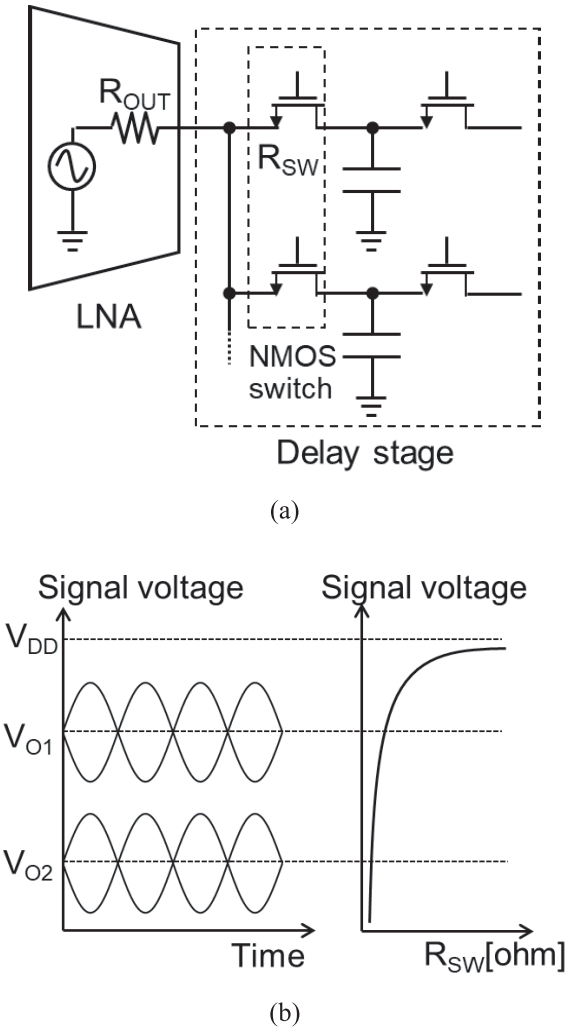

Fig. 5 Level shift function for facilitating the delay stage. (a) Load circuit of LNA. (b) Bias voltage and on-resistance of NMOS sampling switch.

3. Stability Analysis

In this section, the stability of the proposed LNA is described. For differential signal component, the amplifier stage and the driver stage are isolated from each other because node P serves as AC ground. Therefore, the common-mode stability is addressed here. Figure 4 can be simplified as Fig. 6 for common-mode signal component. The common-mode voltage at the node AP (AN) which is output node of the amplifier stage is determined by a local feedback loop of a CMFB-AMP and M5 (M6). An important point is that the voltage variation at node AP (AN) is not fed back by M3 (M4) because the voltage at node BP (BN) which is output node of the driver stage follows to match the voltage for keeping the drain current of M4 (M3). Variation in the common-mode voltage at the input node is also absorbed by voltage change at node P. Therefore, there is no additional sensitive feedback loop in this current-reuse architecture compared with single-stage differential common-source

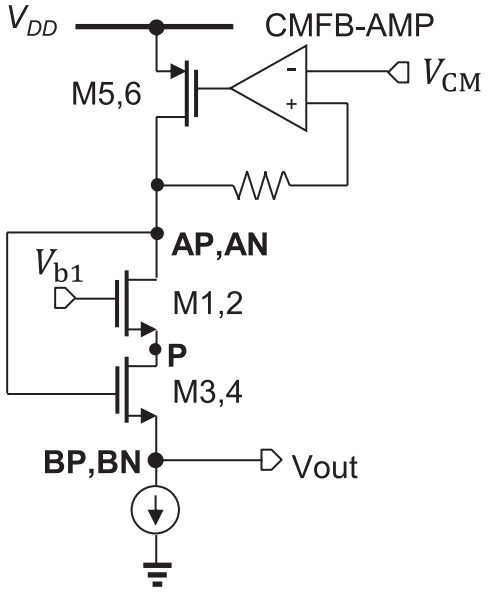

Fig. 6 Simplified schematic for common mode stability analysis.

amplifiers. Therefore, design for stability can be treated in the same manner as an open-loop differential LNA.

4. Measurement Results

The proposed LNA was designed and fabricated in a 0.18-μm SOI CMOS process. Figure 7 shows a photo of the fabricated chip. The core area of a single proposed LNA including the CMFB-AMP is 70 µm × 80 µm. Figure 8 shows a set up for measuring the fabricated LNA. The fabricated chip is packaged in QFP44. The input signal is supplied to the LNA from arbitrary/function generator (Agilent: 33500B) through the on-chip TR-SW [4]. The output signal of the LNA is buffered by an on-chip monitoring buffer (MON-BUFFER) and measured by a differential probe (Agilent: 1141A) and spectrum analyzer (Keysight: N9030B). In the following measured result, input voltage is defined as voltage at an input terminal on the evaluation board. The reason of using MON-BUFFER is to avoid a parasitic capacitance of evaluation board. Because the LNA is designed to drive a switched capacitor in the delay stage, which is usually a few pF or less, the parasitic capacitance of evaluation line is too large to evaluate a performance of the LNA without an on-chip buffer. Figure 9 shows a structure of the MON-BUFFER. The MON-BUFFER is a very simple source-follower circuit composed of 5V-MOSFETs. 5V-MOSFETs are utilized to prevent a linearity of MON-BUFFER from affecting the evaluation results. The equivalent input capacitance of MON-BUFFER is 1.2 pF and −3 dB cutoff frequency with 20 pF load capacitance is 70 MHz, which is enough bandwidth to evaluate the LNA. The gain of MON-BUFFER is −0.07 dB to −0.2 dB in 0.1 MHz–10 MHz, which affects the evaluation of the LNA performance only slightly.

The measured supply current of the LNA circuit was

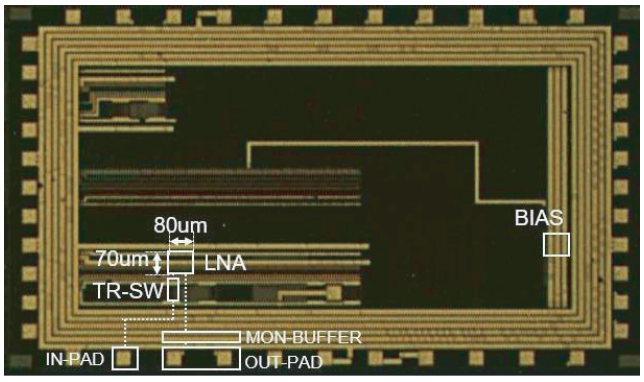

Fig. 7 Die photo of proposed LNA.

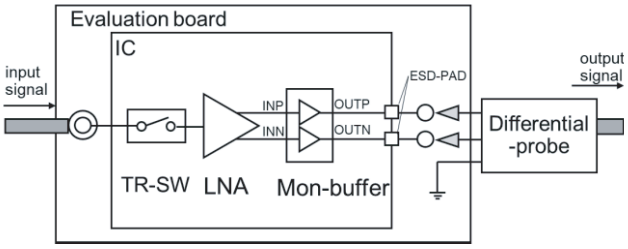

Fig. 8 Measurement setup.

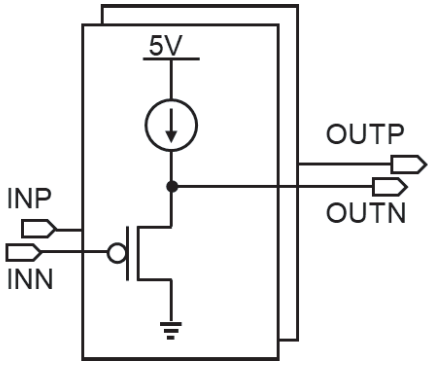

Fig. 9 Implemented MON-buffer for measurement.

85 μA including CMFB-AMP under a supply voltage of 1.8 V. The total power consumption was 153 μW, which is very suitable for ultrasound imaging systems as described in Sect. 1. Figure 10 shows the simulated and measured frequency response of the prototype LNA. The LNA achieved a 10-MHz cutoff at −3 dB from the peak gain of 21.9 dB in measurement results, which is well matched with simulation. In a real ultrasound beamformer, the signal source is the transducer element and their impedance is different from that of signal generator (50 ohm). Regarding the frequency characteristics, the low-frequency side is mainly affected by this difference of impedance. However, since the input impedance of this LNA is high, it can be adjusted to match the impedance of the transducer element by inserting a resistor between the LNA input and the ground. The simulated and measured gain, 2nd and 3rd harmonic distortions versus input voltage swing are presented in Fig. 11. As mentioned in Sect. 2, distortion increases when the input voltage becomes close to 100 mVpp, but the 2HD increases less than the 3HD because of the differential cancellation. The 2HD was kept below −40 dBc at a 0.1-Vpp input in measurement result. A possible reason why the measured 2HD is higher than the simulation result at small input swing is mismatch in the differential architecture due to process variation. The measured input-referred noise density was 11.3 nV/√Hz in average from 1 MHz to 10 MHz (necessary for the ultrasound system), and the noise density of the full bandwidth is plotted in Fig. 12. The performance of the proposed LNA is compared with state-of-the-art works of bandwidth 1 MHz–100 MHz LNA in Table 1. A noise efficiency factor (NEF) [14] is employed to compare the trade-off between power

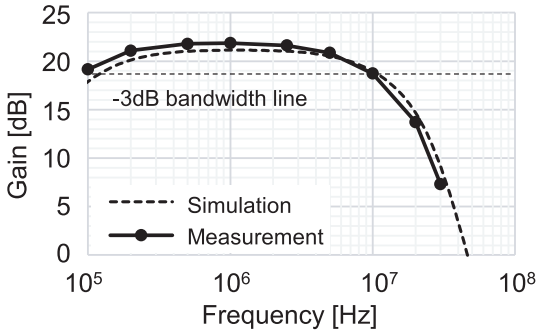

Fig. 10 Simulated and measured frequency response of proposed LNA.

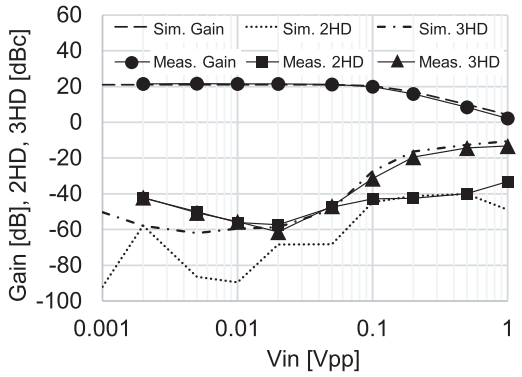

Fig. 11 Simulated and measured performance of gain and 2nd, 3rd harmonic distortion versus input voltage swing.

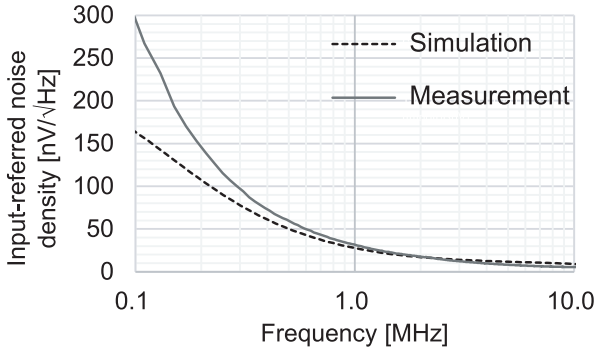

Fig. 12 Simulated and measured input-referred voltage noise density.

Table 1 Benchmark.

Work	[11]	[12]	[13]	This work
Process	0.18 µm	28 nm	65 nm	0.18 µm HV SOI
Supply voltage [V]	1.8	1.0	0.5	1.8
Gain [dB]	19	20	26	21
Bandwidth [MHz]	33	100	40	9
Input-referred voltage noise density [nV/√Hz]	1.01	1.74	7.0	11.3
Total input-referred voltage noise [µV]	5.8	20.8	44.3	34.0
2nd harmonic distortion [dBc]	−53.5	-	−55	−40
Supply current [mA]	9	2	0.108	0.085
Noise efficiency factor	3.7	3.6	2.8	4.0
Core area [mm^2]	0.36	0.0012	0.016	0.0056

consumption and noise performance.

$$NEF = V_{\mathrm{ni,rms}} \sqrt{\frac{2I_{\mathrm{tot}}}{\pi \cdot \mathrm{U_T} \cdot 4\mathrm{kT} \cdot BW}} \tag{7}$$

where $V_{ni,rms}$ is the total in-band input-referred voltage noise, I_{tot} is the supply current, U_T is the thermal voltage, k is the Boltzmann constant, T is the temperature and BW is the bandwidth of LNA, respectively. The attained power and area efficiencies are competitive or even better than prior works with much finer CMOS process.

5. Conclusion

In this paper, a low-power small-size LNA with a novel current-reuse architecture was presented for ultrasound beamformers. The proposed LNA was implemented in only 0.0056 mm^2 chip area with 0.18-µm CMOS process and verified the performance of an input noise density of 11.3 nV/√Hz, a bandwidth of 9 MHz, and a gain of 21 dB with sufficiently low supply current 85 µA, which enables to increase a performance of a next-generation 3D ultrasound imaging system.

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