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An Evaluation of a New Type of High Efficiency Hybrid Gate Drive Circuit for SiC-MOSFET Suitable for Automotive Power Electronics System Applications

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SUMMARY In response to fast charging systems, Silicon Carbide (SiC) power semiconductor devices are of great interest of the automotive power electronics applications as the next generation of fast charging systems require high voltage batteries. For high voltage battery EVs (Electric Vehicles) over 800V, SiC power semiconductor devices are suitable for 3-phase inverters, battery chargers, and isolated DC-DC converters due to their high voltage rating and high efficiency performance. However, SiC-MOSFETs have two characteristics that interfere with high-speed switching and high efficiency performance operations for SiC MOS-FET applications in automotive power electronics systems. One characteristic is the low voltage rating of the gate-source terminal, and the other is the large internal gate-resistance of SiC MOS-FET. The purpose of this work was to evaluate a proposed hybrid gate drive circuit that could ignore the internal gate-resistance and maintain the gate-source terminal stability of the SiC-MOSFET applications. It has been found that the proposed hybrid gate drive circuit can achieve faster and lower loss switching performance than conventional gate drive circuits by using the current source gate drive characteristics. In addition, the proposed gate drive circuit can use the voltage source gate drive characteristics to protect the gate-source terminals despite the low voltage rating of the SiC MOS-FET gate-source terminals.

key words: *SiC-MOSFET, gate-driver, current-source, voltage-source, gate resistance*

1. Introduction

Electric Vehicle (EV) technical trend have been attracted great interest from all over the world because of its growing great market until 2030. Figure 1 shows each automotive company's sales quantity compared between 2019 and 2020. In spite of COVID-19 calamity, it is understood that only TESLA have expanded their sales as in Fig. 1. The reason is long cruising range for one full charging condition in TESLA EV products. In general, the long cruising range performance is decided from total balance between the coefficient of drag (CD) value and heavy weight of EV. Model 3 and Model S of TESLA EV can achieve higher balance performance in each component as compared with Taycan/Porsche as in Fig. 2. From this discussion, it can be seen that the most important performance for automotive applications is high power density performance [1].

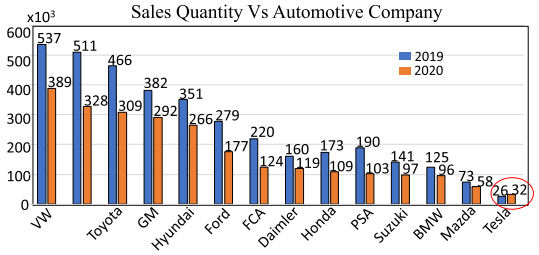

Fig. 1 Automotive manufacturer's sales for year 2019 and 2020.

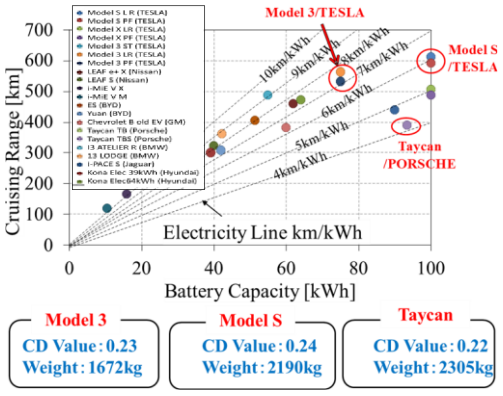

Fig. 2 Relationship between cruising range and battery capacity.

In addition, compared to traditional technologies, next-generation EV applications require additional technology to achieve high power density performance.

The electric system for EV is composed of the on-board charger, the isolated DC-DC converter, main drive inverter and traction motor in general. And each electric components will mount and laminated as shown in Fig. 3. In this case, each electric components must keep low profile performance because the higher automobile hoods influence directly for CD value of EVs.

To achieve the low-profile performance, several technical challenges will be required in next generation EV applications as shown in Fig. 4. Mainly, the necessary technical components can be divided into two parts, which is a high frequency and a high efficiency technology. In case

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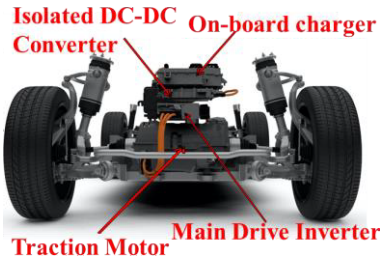


Fig. 3 Electric Components of EV System for Jaguar I-Pace (2020).

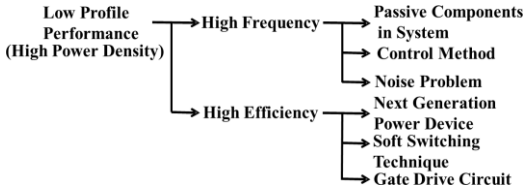


Fig. 4 Technical requirement for low profile performance of EV system.

of high frequency condition, passive components will be achieve high power density and miniaturized performance [2]–[5]. And high frequency system requires higher performance control method in both of analogue and digital feedback systems [6]–[14]. However, high frequency system includes noise problem in DC bus-line for EV. In electric system for EV, there are many numbers of DC-DC converters connected in parallel to DC bus-line, therefore, each DC-DC converter EMI/EMC noise control requires effective measures [15]–[19]. This is because if noise appears on the DC bus line, it will affect the end application of each DC-DC converter over the DC bus line.

The DC bus-line application such as auxiliary battery charger in HEV/EV, is important too and as a solution of preventing noise, isolated DC-DC converter, its combination systems and DC breaker have been reported in recent years [20]–[36].

On the other hand, high efficiency technique contributes to miniaturized cooling systems of power electronics system for EV. Because power electronics components related to power losses is account for half volume of power electronics systems for EV as shown in Fig. 5. Therefore, the reduction of power losses in Power Electronics systems is effective solution for high power density technical hurdle.

Most effective solution to the technical hurdles of high power density is to replace power devices with next generation power semiconductor devices such as Silicon Carbide (SiC), Gallium Nitride (GaN) and Gallium Oxide [37]–[39] due to their high-performance characteristics of low device power loss. However, the cost problem remains for such power device applications. In addition, soft switching techniques can effectively reduce power losses in power electronics systems with traditional silicon devices. On the other hand, soft switching techniques require additional circuitry and control systems for perfect zero voltage switching (ZVS) and zero current switching (ZCS) in switching transient of each power semiconductor devices [40]–[47].

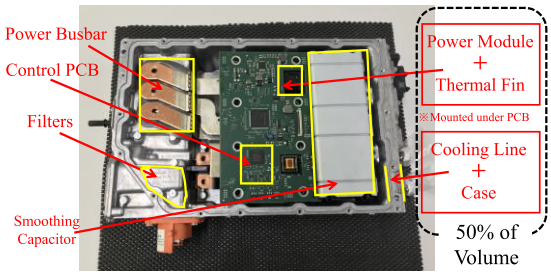


Fig. 5 Power Electronics System for EV (Jaguar I-Pace, 2020).

Therefore, using soft switching technology increases cost and space. Replacing silicon devices with SiC makes GaN a reasonable solution and at a relatively low cost.

In this paper, the combination solution has been selected for high power density performance for power electronics system. That is combination technique between SiC power semiconductor device applications and its gate drive circuit development. Because SiC power device have been already applied in Electric Vehicle, Model 3/TESLA [48]. However, the conventional gate drive circuit has been applied in such EV, but improved gate drive circuit can reduce power losses as compared with conventional gate drive circuit. Our effort is to propose novel gate driver circuit to mitigate the gate driving problem and reduce the power losses.

2. Characteristics of SiC MOSFET and Gate-Driving Problems

SIC-MOSFETs, which are next-generation power semiconductors, have greater advantages over conventional silicon MOSFETs and IGBTs in high voltage switching power supply applications. However, in consideration of the characteristics of SiC-MOSFET from the point of view of the gate drive, it can be seen that the characteristics of SiC-MOSFET have several problems [49], [50].

One of the main points is that the internal gate resistance RG (int) is large as compared with the same specification (device voltage) of silicon MOSFET. Figure 6 is a diagram in which more than 1000 MOSFETs are examined and among them, those in which the internal gate resistance and the input capacitance are described in the data sheet are extracted and the time constant is plotted.

As seen from Fig. 6, the SiC-MOSFET has a large time constant. Compared to silicon MOSFETs, SiC-MOSFETs can achieve lower on-resistance on smaller area chips, reducing gate input capacitance. However, currently, polysilicon is mainly used as the gate electrode material for SiC-MOSFETs fabrication process to get high switching speed, but it has higher resistance and higher gate resistance than the silicide used for silicon MOSFETs. In addition, for modular products consisting of multiple Si or SiC chips, gate waveform disturbance is common and has an undesired effect on switching transients. A damping resistor is inserted in each chip to suppress the disturbance of the waveform. However, the internal gate resistance of SiC is higher than

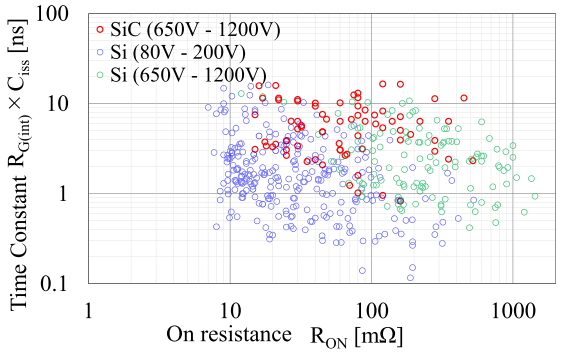


Fig. 6 Comparison of time constant by internal gate resistance and input capacitance of MOSFET.

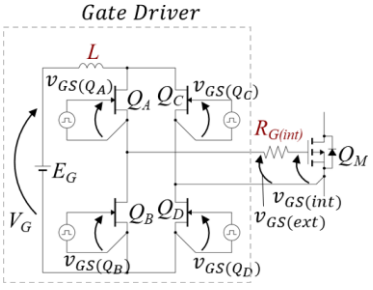


Fig. 7 Current source type gate driver circuit.

that of Si, and the gate resistance of SiC increases with the damping resistance.

Therefore, the time constant of the internal gate resistance is several times that of the silicon MOSFET, and there is a problem that high-speed driving is difficult with a general voltage source type gate drive circuit.

The second point is that the gate withstand voltage is low. In the case of a voltage source type gate drive circuit, there is a way to increase the gate drive voltage in order to overcome the deceleration of the gate drive due to the internal gate resistance. However, since the difference between the rated drive voltage of the gate and the absolute maximum rated voltage of the SiC-MOSFET is small, if the gate drive voltage is easily increased, there is a risk of withstand voltage failure due to ringing. The current source type gate drive circuit can drive the gate at high speed without being affected by the internal gate resistance, but in the case of the driver circuit in Fig. 7, there is an inductor and the gate input capacitance of the SiC-MOSFET. Therefore, the steady-state gate voltage may not be as designed and the gate withstand voltage may be exceeded.

Third point, the transconductance is small, and the ON resistance fluctuates greatly due to fluctuations in the gate voltage. In this respect, a voltage source type gate drive circuit in which the gate drive voltage in a steady state is stable is advantageous. In the current source type gate drive circuit, as in Fig. 7, the gate drive voltage in the steady state gradually decreases due to the gate leak current. Therefore, there is a risk that the loss will increase due to the increase in ON resistance. In addition, due to the low transconductance of SiC-MOSFETs, the ON resistance has a negative coefficient with respect to temperature in the low gate voltage range. Therefore, in a drive circuit such as a current source type gate drive circuit in which the gate drive voltage drops during steady operation, the SiC-MOSFET may risk of thermal runaway.

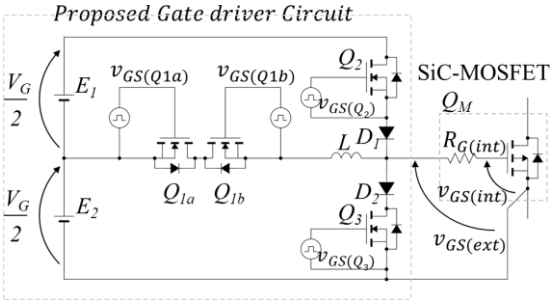


Fig. 8 Proposed hybrid gate driver circuit.

3. Proposed Hybrid Gate Driver System

In the previous section, we explained the problems when using a conventional gate drive circuit for the gate drive of SiC-MOSFET. Therefore, we realized that driving a SiC-MOSFET needs gate driver circuit that allows current to flow through the gate regardless of the internal gate resistance, and the characteristics of a voltage source-type gate drive circuit that stabilizes the gate voltage during steady state operation. Therefore, in this paper, we propose a new gate drive circuit that realizes high-speed and stable gate drive by charging the gate at high-speed using an inductor that acts as a current source at the time of rising and falling, and then shifting to voltage source type drive in order to realize the optimum gate drive of SiC-MOSFET.

3.1 Configuration of Proposed Gate Driver Circuit

The proposed circuit configuration is shown in Fig. 8. The area surrounded by the gray dotted line on the left side is the proposed gate drive circuit, and the Q_M is the targeted SiC-MOSFET. The proposed circuit consists of four switching elements (Q_{1a}, Q_{1b}, Q_2, Q_3), two diodes (D_1, D_2), power supplies (E_1, E_2) with voltage $V_G/2$, and an inductor (L). The gate voltages of Q_{1a}, Q_{1b}, Q_2, and Q_3 are set to $v_{GS(Q\_1a)}$, $v_{G(Q\_1b)}$, $v_{GS(Q\_2)}$, $v_{GS(Q\_3)}$, respectively, and are outside the Q_M. Let the gate voltage seen from above be $v_{GS(ext)}$ and the gate oxide film voltage be $v_{GS(int)}$. The gate voltage when Q_M is on is V_G, which is the rated gate voltage or recommended gate drive voltage described in the data sheet of the SiC-MOSFET used.

3.2 Operating Principle

As shown in Fig. 9, the gate control signal of each switching element that composes the proposed gate driver circuit is generated from the PWM command from the external controller. In the proposed circuit, each MOSFET has a simple

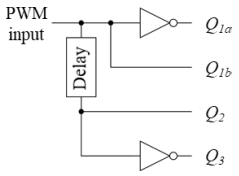


Fig. 9 Gate control signal distribution circuit.

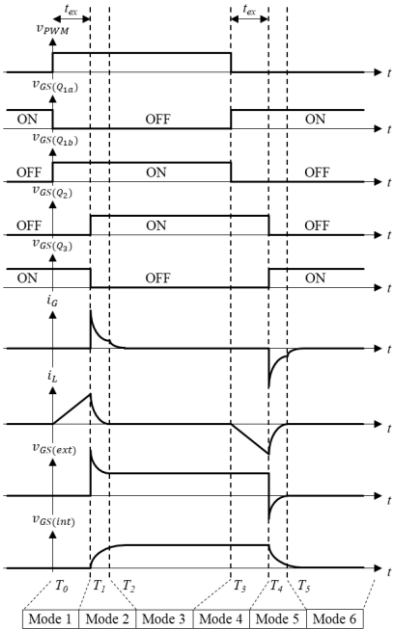


Fig. 10 Key waveforms and operating modes of proposed hybrid gate driver circuit.

operation of turning on and off only once per cycle of the input PWM signal, so it can be operated with such a simple distribution circuit. In an actual circuit, if Q_2 and Q_3 are turned on at the same time, a shoot-through current will flow, so it is necessary to set a dead time at each switching. For Q_{1a} and Q_{1b}, dead time is not required because the switching is performed when the current of the inductors connected in series is zero. Figure 10 shows the key waveforms and operating modes of the proposed gate drive circuit.

3.3 Operating Modes of Proposed Circuit

Figure 11 shows the operating modes of proposed gate driver circuit and each mode of circuit operation is explained in Sect. 3.3.

⟨Mode 1⟩ As shown in Fig. 11(a), Q_{1b} and Q_3 are in the ON state, and Q_{1a} and Q_2 are in the OFF state. This mode is the preparation period for turning on the SiC-MOSFET to be driven. Current flows from the power supply E_2 as shown by the gray solid arrow in Fig. 11(a), and the inductor L is excited. At the time of T_1, Q_2 is turned on and Q_3 is turned off to move to the next mode. Since the current i_L of the inductor L increases linearly, if the exciting time is $t_{ex} = T_1 - T_0 = T_4 - T_3$ and the forward voltage of the body diode of Q_{1a} and D_2 is V_f, the value of iL at T_1 is given by (1). Although V_f is current-dependent, its fluctuation is very smaller than the voltage $V_G/2$ of the power supply E_2 and it can be ignored.

$$i_L(T_1) = \frac{\frac{V_G}{2} - 2V_f}{L} t_{ex} = \frac{V_G - 4V_f}{2L} t_{ex} \quad (1)$$

Table 1 Absolute maximum ratings of SiC-MOSFET (BSM300D12P2E001).

Parameter	Symbol	Limit
Drain-source voltage [V]	V_{DSS}	1200
Gate-source voltage [V]	VG_{GS}	-6 to 22
Drain current [A]	I_D	300
Source current [A]	I_S	300

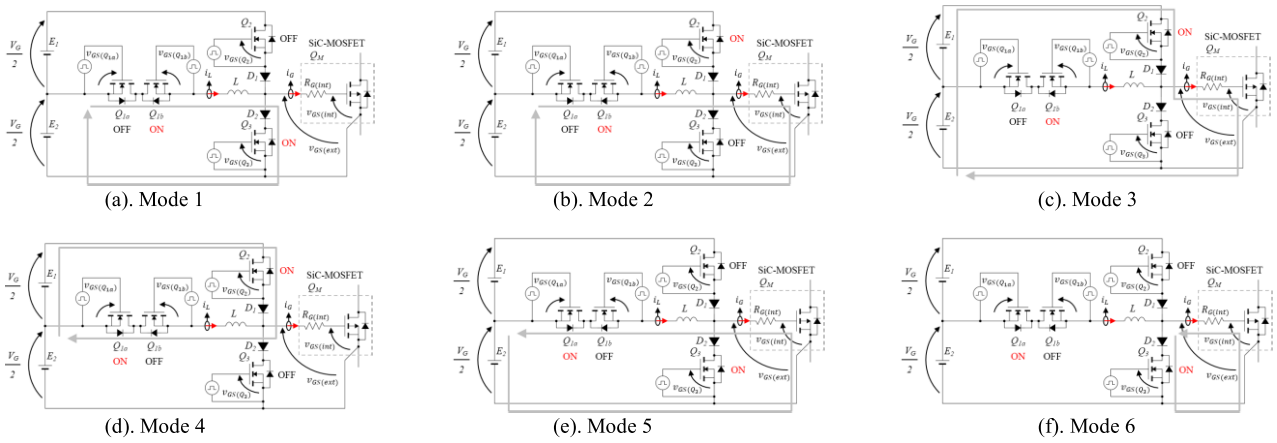
⟨Mode 2⟩ As shown in Fig. 11(b), Q_{1b} and Q_2 are in the ON state, and Q_{1a} and Q_3 are in the OFF state. The SiC-MOSFET turns on when the current of the inductor L excited in Mode 1 passes through the gate of the SiC-MOSFET to be driven. At this time, the inductor L behaves as a current source, so the gate current is not limited to the internal parasitic gate resistance $R_{G(int)}$ of the SiC-MOSFET. In other words, it is a current source type drive, and high-speed gate drive is realized.

⟨Mode 3⟩ As shown in Fig. 11(c), after the gate of the SiC-MOSFET is fully charged by the action of the inductor L, the gate of the SiC-MOSFET is clamped to V_g by Q_2 turned on in Mode 2, and the voltage stabilizes. This mode is voltage source type drive. The transition from Mode 2 to Mode 3 is performed at T_3, but at this time, no command from the external controller is required, and the transition occurs naturally when the current of the inductor L becomes zero.

⟨Mode 4⟩ As shown in Fig. 11(d), Q_{1a} and Q_2 are in the ON state, and Q_{1b} and Q_3 are in the OFF state. This mode is equivalent to Mode 1 except that the direction of the current is opposite, and it is the preparation period for turning off the SiC-MOSFET to be driven. A current flow from the power supply E_1 as shown by the gray solid arrow in Fig. 11(d), and the inductor L is excited. At the time of T_4, Q_2 is turned on and Q_3 is turned off to move to the next mode.

⟨Mode 5⟩ As shown in Fig. 11(e), Q_{1a} and Q_3 are in the ON state, and Q_{1b} and Q_2 are in the OFF state. The SiC-MOSFET turns off when the gate charge of the SiC-MOSFET to be driven is pulled out at once by the inductor L excited in Mode 4. At this time, the inductor L behaves as a current source, so the gate current is not limited to the internal parasitic gate resistance $R_{G(int)}$ of the SiC-MOSFET. In other words, it is a current source type drive, and high-speed gate drive is realized.

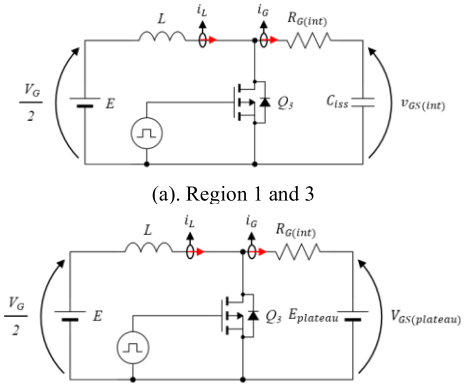
⟨Mode 6⟩ As shown in Fig. 11(f), after the gate of the SiC-MOSFET is fully charged by the action of the inductor L, the gate of the SiC-MOSFET is clamped to 0 V by Q_3 turned on in Mode 5, and the voltage stabilizes. This mode is voltage source type drive. The transition from Mode 5 to Mode 6



(a). Mode 1 (b). Mode 2 (c). Mode 3

(d). Mode 4 (e). Mode 5 (f). Mode 6

Fig. 11 Operating modes of proposed hybrid gate driver circuit.



(a). Region 1 and 3

(b). Region 2

Fig. 12 Simplified circuit of the proposed gate driver in different regions of gate charge.

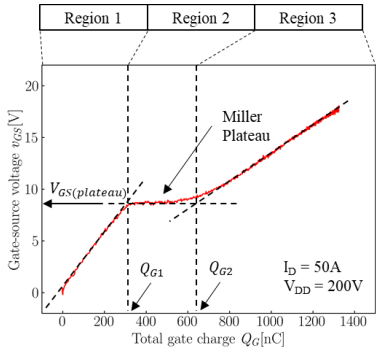


Fig. 13 Actual measurement of Qg–Vgs of SiC-MOSFET (BSM300D12P2E001).

is performed at T_5, but at this time, no command from the external controller is required, and the transition occurs naturally when the current of the inductor L becomes zero.

4. Design of Hybrid Gate Driver Circuit

When driving a MOSFET, it is necessary to design the gate drive circuit so that the gate oxide film voltage does not exceed the absolute maximum rated voltage, but the inductor L that operates as a current source in the proposed circuit also has a large constant and is driven. The gate-source voltage of the target SiC-MOSFET exceeds the absolute maximum rating value, which may cause a malfunction. Conversely, if the inductor constant is too small, the inductor will give less energy to the gate drive of the driving SiC-MOSFET, making it impossible to speed up the gate drive. Therefore, in the proposed circuit, it is important to properly determine the constant of the inductor L that operates as a current source. However, since it is difficult to directly measure the voltage of the gate oxide film, it is necessary to estimate the voltage of the gate oxide film by calculation at both the design stage and the actual machine verification stage. Therefore, focusing on the amount of charge flowing through the gate of the SiC-MOSFET driven from the inductor L, the gate oxide film is based on the relationship of the gate charge amount ($Qg = \int I_G(t)dt$) and gate voltage (V_{gs}).

ROHM's switching device BSM300D12P2E001 [51] is selected as the SiC-MOSFET to be driven in our design. The absolute maximum rating of the SiC-MOSFET is shown in Table 1, and the actual measurement graphs of Q_g and V_{gs} are shown in Fig. 12. As can be read from this graph, Q_g and V_{gs} show a non-linear relationship. In particular, since the feedback capacitance is charged in the mirror plateau region, the slope of the $Q_g - V_{gs}$ graph becomes zero. Here, the analysis is carried out by dividing into three areas as shown in Fig. 12. However, in the proposed circuit, the current drive is performed until the end of the mirror plateau region, so only Region 1 and Region 2 are designed so that the inductor current contributes to the gate drive. Therefore, the regions to be analyzed are only Region 1 and Region 2, and the inductor value and excitation time can be determined by calculating the gate current in this region. As a simpler design method, there is a method of designing using a circuit simulator. The value of the inductor L and the excitation time should be adjusted so that the gate drive current flows through the SiC-MOSFET to be driven even after the current of the inductor L of the proposed gate drive circuit becomes zero. On the contrary, if a current flows from the

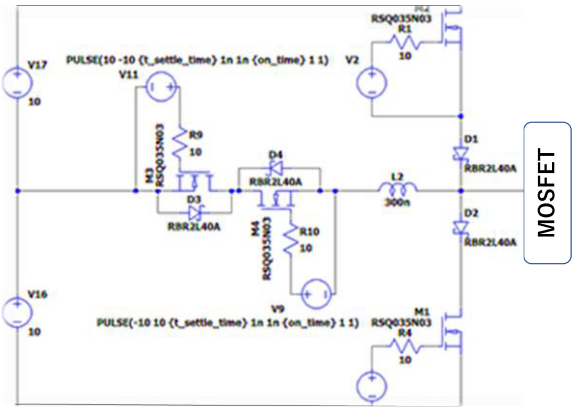


Fig. 14 Proposed gate driver circuit used for simulation.

inductor to the gate of the SiC-MOSFET even after reaching the target gate drive voltage, not only the gate withstand voltage is exceeded, but also the voltage source type drive cannot be shifted, resulting in unstable operation.

⟨Region 1⟩ As shown in Fig. 12, in region 1, the proposed circuit can be simplified as in Fig. 13(a), and gate current can be expressed as (2)

$$L\frac{di_G(t)}{dt} + R_{G(int)}i_G(t) + \frac{1}{C_{iss}}\int i_G(t)dt = \frac{V_G}{2} \tag{2}$$

After number of calculation step gate current (i_G) in region 1 can be derived as (3)

$$i_G(t) = I_0\alpha e^{-\frac{R_{G(int)}}{2L}t}sin(\omega t + \varphi) \tag{3}$$

where

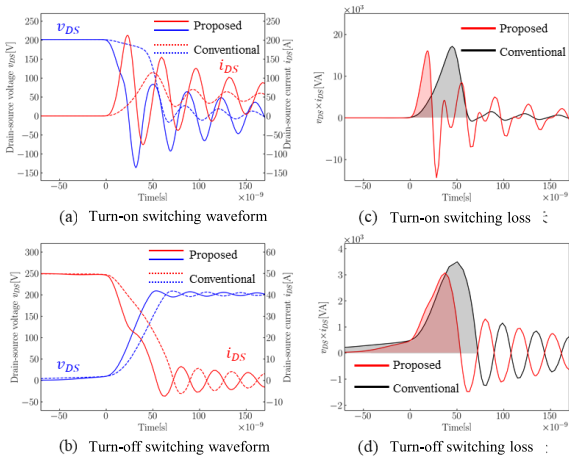
$$\alpha = \sqrt{1 + \left(\frac{V_G - R_{G(int)}I_L}{2\omega L I_0}\right)^2}, \quad \omega = \sqrt{\frac{1}{LC_{iss}} - \left(\frac{R_{G(int)}}{L}\right)^2},$$
$$\varphi = tan^{-1}\left(\frac{2\omega L I_L}{V_G - R_{G(int)}I_L}\right)$$

⟨Region 2⟩ As shown in Fig. 12, region 2 is the mirror plateau region, and since the charge flows from the drain side to the gate side via the feedback capacitance, the slope of the *Qg-Vgs* graph becomes zero. That is, the gate and source of the SiC-MOSFET to be driven behave as a constant voltage source of $V_{gs(plateau)}$. Therefore, the proposed circuit can be simplified as shown in Fig. 13(b). If the inductor current entering this region, is I_L, the gate current can be expressed as (4)

$$i_G(t) = \frac{V_G}{2R_{G(int)}} + \left(I_L - \frac{V_G}{2R_{G(int)}}\right)e^{-\frac{R_{G(int)}}{L}t} \tag{4}$$

5. Simulation

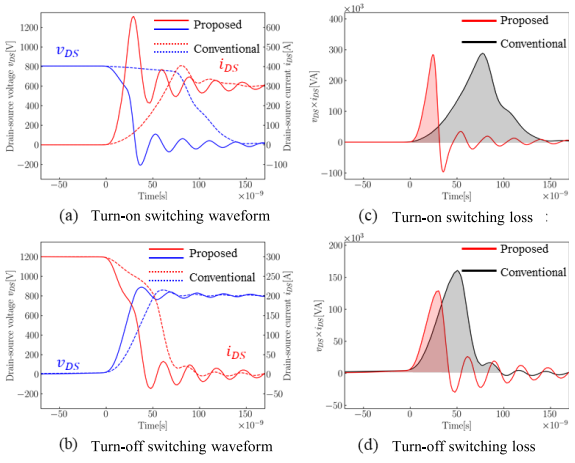
The operation of the proposed gate driver circuit was confirmed by the circuit simulator. The circuit simulator used is LTspice provided by Analog Devices, Inc. The simulation circuit is shown in Fig. 14. In the studies so far, the



(a) Turn-on switching waveform (c) Turn-on switching loss

(b) Turn-off switching waveform (d) Turn-off switching loss

Fig. 15 Simulation results for comparison of switching waveforms of conventional and proposed topologies at 200 V/50 A.



(a) Turn-on switching waveform (c) Turn-on switching loss

(b) Turn-off switching waveform (d) Turn-off switching loss

Fig. 16 Simulation results for comparison of switching waveforms of conventional and proposed topologies at 800 V/300 A.

gate drive voltage of the SiC-MOSFET was 0 V when it was off, but in actual applications, the gate drive voltage when it is off is often set to a negative voltage in order to avoid malfunctions. Therefore, in simulations and experiments, a 2 V constant voltage source was inserted between the Kelvin source terminal of the SiC-MOSFET and the proposed gate drive circuit, and the VG was set to 20 V so that the drive could be from −2 V to 18 V. bottom. The gate drive voltage only shifts as a whole, and the operation of the proposed circuit and the voltage and current of each part are the same as in the previous studies. The SPICE model provided by ROHM was used as the model of the SiC-MOSFET (ROHM BSM300D12P2E001).

Figure 15 shows a comparison of the switching waveforms of conventional voltage source type gate drive circuit and the proposed gate drive circuit is simulate under the conditions of drain-source voltage 200 V and drain-current 50 A. Similarly, Fig. 16 compares the switching waveforms by simulating under the conditions of drain-source voltage 800 V and drain-current 300 A. In each simulation result, the

switching loss at turn-on is shown in red and black area in Fig. 15(c), Fig. 16(c). The turn-off switching loss is shown in red and black area in Fig. 15(d), Fig. 16(d). In any of the conditions, when the SiC-MOSFET was driven by the proposed circuit, the waveform transition is sharper than in the conventional voltage source type gate drive circuit, confirming the effect of increase of switching speed and low switching losses.

6. Experimental Verification

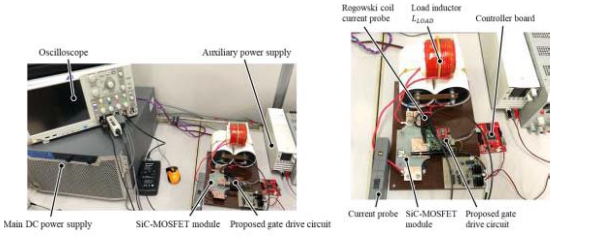
Experimentally driven the SiC-MOSFET using the proposed gate drive circuit and verified the effect of increasing the switching speed in the double pulse test circuit.

6.1 Method and Techniques of Measurements

Figure 17 shows the experimental setup with the enlarged view. Using the Tektronix DPO5204B oscilloscope (frequency band 2 GHz, sampling rate 10 GS/s), waveform of the experimental prototype was measured.

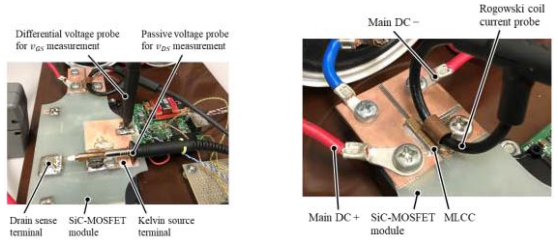
In the double pulse test, various measures are required to measure a waveform that is closer to the true waveform. Especially in the case of high-speed switching devices such as SiC-MOSFETs, the waveform becomes violent due to the parasitic inductance of the circuit. In the case of the SiC-MOSFET module used this time, the parasitic inductance inside the package is large, so it is important to reduce the parasitic inductance of the external circuit.

Figure 18(a) shows the measurement points of the drain-source voltage waveform. A wideband passive probe (Tektronix P5100A) was used to measure the drain-source voltage waveform. Although different passive probes are



(a). Test setup (b). Expanded view of test setup

Fig. 17 Experimental setup for proposed gate driver circuit.



(a). Voltage measurement (b). Current measurement

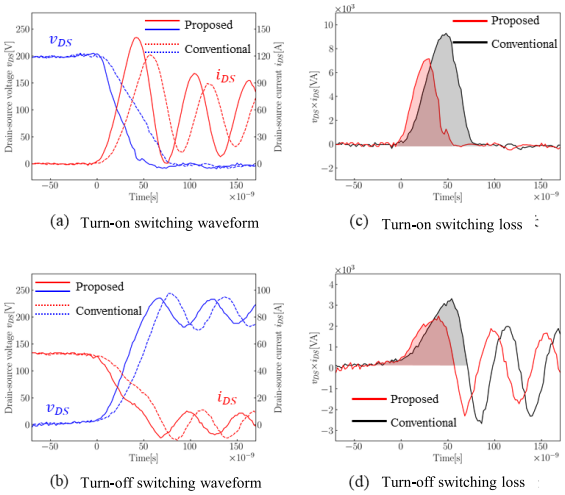
Fig. 18 Points of voltage and current measurement of experimental prototype. Current measured between MLCC array and drain-source.

connected in Fig. 18(a), P5100A was used in the waveform measurement. The waveform measured from the chip of the passive probe to the drain source of the switching device and the inductance of the ground lead of the passive probe is greatly affected. In addition, due to the wiring inductance inside the module, when measurement is performed at the terminal where a large current flows, a waveform that is significantly different from the waveform of the internal SiC-MOSFET chip is observed. Therefore, in the experimental verification, the substrate was placed directly above the SiC-MOSFET module, the passive probe was fixed without using a ground lead as shown in Fig. 18(a), and measurement was performed between the sensing drain terminal and the Kelvin source.

Furthermore, as in Fig. 18(b), the MLCC (Multilayer Ceramic Capacitor) connected between the PN terminals of the MOSFET and the current probe used to measure the drain-source current. A low-impedance MLCC was placed in the immediate vicinity between the PN terminals of the MOSFET, and the current measurement loop was also devised to minimize the ringing of the waveform.

6.2 Experimental Results

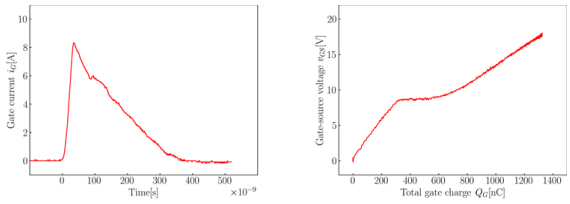
Measured results of the proposed gate driver circuit using the experimental prototype will be described. Figure 19 shows the waveform of the test results with a drain-source voltage of 200 V and a drain-current of 50 A. In both Fig. 19(a) and Fig. 19(b), the solid line is the waveform when the SiC-MOSFET module is driven using the proposed gate drive circuit, and the broken line is the waveform when the conventional voltage source type gate drive circuit is used. The blue line is the drain-source voltage waveform, and the red line is the drain-source current waveform. Furthermore, Fig. 19(c) and Fig. 19(d) show the losses at turn-on and turn-off, respectively. The red area is the loss when the proposed gate drive circuit is measured, and the



(a) Turn-on switching waveform (c) Turn-on switching loss

(b) Turn-off switching waveform (d) Turn-off switching loss

Fig. 19 Experiment results for comparison of switching waveforms of conventional and proposed topologies at 200 V/50 A



(a) Gate Current (b) Q_G-v_{GS}

Fig. 20 Gate current and gate charge Q_G-v_{GS} with proposed gate driver when driving a SiC-MOSFET.

black area is the loss when the conventional voltage source type gate drive circuit is measured. Similar to the simulation study, it was confirmed that the switching speed was increased for both turn-on and turn-off. When the switching loss was calculated, the turn-on loss shown in Fig. 19(c) was 359 μJ for the conventional voltage source type gate drive circuit and 203 μJ when the proposed gate drive circuit was used. 43.5% of turn-on loss reduction is achieved with proposed gate driver circuit. Similarly, regarding the loss at turn-off, 27.7% loss reduction is achieved. 141 μJ when using the conventional voltage source type gate drive circuit and 102 μJ when using the proposed circuit.

Figure 20 shows the measurement results of the gate current at turn-on switching when the SiC-MOSFET is driven with proposed gate driver circuit. When the gate current waveform was integrated, the amount of charge that flowed was 1300 nC. When the gate oxide film voltage is read from Fig. 20(b), it is found to be 18 V. Therefore, it was confirmed that the current drive was shifted to the voltage drive as designed in the middle of the gate drive, and that safe drive was possible without exceeding the gate withstand voltage.

7. Conclusions

In this paper, we have explained the problems from the viewpoint of gate drive of SiC-MOSFET as compared with silicon MOSFET. High internal gate resistance and low transconductance can slow down switching speeds and fluctuate gate drive voltages, which can lead to high SiC-MOSFET losses. In addition, since the margin of the gate withstand voltage is smaller than the recommended gate drive voltage, the method of increasing the gate drive voltage for high-speed switching cannot be adopted, and stable gate drive is required. Therefore, in order to mitigate the above gate drive problem, a hybrid gate driver is proposed, confirmed by Lt-spice simulation, and experimentally verified. Significant results were achieved with a 43.5% reduction in turn-on switching loss and a 27.7% reduction in turn-off switching loss.

References

[1] M. Yamamoto, T. Kakisaka, and J. Imaoka, "Technical trend of power electronics systems for automotive applications," Jpn. J. Appl. Phys., vol.59, pp.0805-1–0805-13, 2020.

[2] F. Kurokawa, M. Sasaki, S. Hiura, and H. Matsuo, "1 MHz high-speed digitally controlled DC-DC converter," IEICE Trans. Commun., vol.E87-B, no.12, pp.3437–3442, Dec. 2004.

[3] T. Suetsugu, X. Wei, and M.K. Kazimierczuk, "Analysis of dynamic and transient response of frequency modulated class E amplifier," IEICE Trans. Commun., vol.E97-B, no.8, pp.1630–1637, Aug. 2014.

[4] M. Matsuo, T. Suetsugu, S. Mori, and I. Sasase, "Resonant DC/DC converter with class DE tuned power oscillator," IEICE Trans. Commun. (Japanese edition), vol.J82-B, no.10, pp.1830–1837, Oct. 1999.

[5] T. Fujita and K. Wada, "Considering of frequency splitting phenomena of magnetic resonance WPT systems and investigation of maximum power tracking circuit using PLL," IEICE Trans. Commun. (Japanese edition), vol.J102-B no.6, pp.459–472, June 2019.

[6] S. Hong and B. Choi, "Average model for pulse width modulatorin voltage-mode-controlled PWM converters," IEICE Trans. Commun., vol.E85-B, no.7, pp.1415–1417, July 2002.

[7] Y. Murakawa, Y. Sadanda, and T. Hikihara, "Parallelization of boost and buck type DC-DC converters by individual passivity-based control," IEICE Trans. Fundamentals, vol.E103-A, no.3, pp.589–595, March 2020.

[8] H. Matsuo, F. Kurokawa, and H. Eto, "Novel digital controller with static model reference for switching DC-DC power converters," IEICE Trans. Commun., vol.E88-B, no.11, pp.4346–4352, Nov. 2005.

[9] M. Sasaki, H. Matsuo, F. Kurokawa, and Y. Mimura, "Static characteristics of the digital PWM and/or PFM controlled switching DC-DC converters," IEICE Trans. Commun., vol.E90-B, no.3, pp.645–650, March 2007.

[10] F. Kurokawa and M. Okamatsu, "Static and dynamic characteristics of DC-DC converter using a digital filter," IEICE Trans. Commun., vol.E92-B, no.3, pp.998–1003, March 2009.

[11] T. Kohama, S. Tokimatsu, and A. Inoue, "Magnetic saturation due to fast dynamic response and its eliminating method in bridge-type DC-DC converter," IEICE Trans. Commun., vol.E93-B, no.8, pp.2165–2170, Aug. 2010.

[12] T. Hirose and Y. Nakazawa, "Design of switched-capacitor voltage boost converter for low-voltage and low-power energy harvesting systems," IEICE Trans. Electron., vol.E103-C, no.10, pp.446–457, Oct. 2020.

[13] K. Fujiwara, R. Ute, J. Imaoka, and M. Oyama, "Limit operating frequency of peak current Mode Control DC-DC converter considering turn-off delay time," IEICE Trans. Commun. (Japanese edition), vol.J101-B, no.11, pp.950–957, Nov. 2018.

[14] M. Nakamura, K. Takeno, and M. Shoyama, "Electric load leveling control of lithium-ion battery in green base stations," IEICE Trans. Commun. (Japanese edition), vol.J104-B, no.6, pp.520–526, June 2021.

[15] G.M. Dousoky, M. Shoyama, and T. Ninomiya, "A comparative investigation of several frequency modulation profiles for programmed switching controllers targeted conducted-noise reduction in DC-DC converters," IEICE Trans. Commun., vol.E93-B, no.9, pp.2265–2272, Sept. 2010.

[16] H. Hasegawa, K. Harada, Y. Ishihara, and T. Todaka, "An examination of radiation noise characteristics in DC-DC converters," IEICE Trans. Commun. (Japanese edition), vol.J84-B, no.4, pp.801–808, April 2001.

[17] K. Hayashi, T. Funaki, and T. Ibuchi, "Common mode voltage compensation method in transient floating voltage measurement for high side arm of half bridge circuit," IEICE Trans. Commun. (Japanese edition), vol.J103-B, no.1, pp.11–21, Jan. 2020.

[18] T. Nishimoto, M. Yamaoka, T. Yamada, T. Matsushima, and O. Wada, "Common-mode noise reduction on asymmetric switching power supply circuits with impedance balance method," IEICE Trans. Commun. (Japanese edition), vol.J102-B, no.3, pp.184–193, March 2019.

[19] Y. Saito, T. Ibuchi, T. Funaki, K. Kawai, and T. Tsuda, "Equivalent circuit modeling of EMI noise source for CMOS-based DC-DC buck converter," IEICE Trans. Commun. (Japanese edition), vol.J104-B, no.6, pp.461–470, June 2021.
[20] W. Lint, H. Matsuo, F. Kurokawa, and Y. Ishizuka, "Control strategies of the multiple-input DC-DC converter," IEICE Trans. Commun., vol.E85-B, no.9, pp.1824–1831, Sept. 2002.
[21] J. Zhang, X. Xie, D. Jiao, and Z. Qian, "A high efficiency adapter with novel current driven synchronous rectifier," IEICE Trans. Commun., vol.E87-B, no.12, pp.3471–3477, Dec. 2004.
[22] T. Hosotani, K. Harada, Y. Ishihara, and T. Todaka, "A novel self-excited ZVS half-bridge converter with energy stored transformer and capacitor," IEICE Trans. Commun., vol.E87-B, no.12, pp.3531–3538, Dec. 2004.
[23] S. Moiseev, K. Soshin, and M. Nakaoka, "High-frequency isolated soft-switching phase-shift PWM DC-DC power converter using tapped inductor filter," IEICE Trans. Commun., vol.E87-B, no.12, pp.3561–3567, Dec. 2004.
[24] O. Matsuo, H. Matsuo, Y. Shizuka, and H. Ota, "Analysis of a multi-oscillated current resonant type DC-DC converter," IEICE Trans. Commun., vol.E91-B, no.10, pp.3307–3312, Oct. 2008.
[25] T. Kohama, S. Tokimatsu, and A. Inoue, "Magnetic saturation due to fast dynamic response and its eliminating method in bridge-type DC-DC converter," IEICE Trans. Commun., vol.E93-B, no.8, pp.2165–2170, Aug. 2010.
[26] H. Terashi and T. Ninomiya, "Analysis of leakage-inductance effect on characteristics of flyback DC-DC converter using time keeping control," IEICE Trans. Commun. (Japanese edition), vol.J87-B, no.11, pp.1959–1969, Nov. 2004.
[27] K. Fukushima, I. Norigoe, T. Ninomiya, M. Shoyama, Y. Harada, and K. Tsukakoshi, "Characteristics of a pulse-link DC-AC converter for fuel cells," IEICE Trans. Commun. (Japanese edition), vol.J92-B, no.1, pp.345–352, Jan. 2009.
[28] S. Tomioka, T. Ninomiya, and M. Shoyama, "Analysis of boost-input type full bridge converter with leakage inductance," IEICE Trans. Commun. (Japanese edition), vol.J93-B, no.11, pp.1512–1521, Nov. 2010.
[29] K. Nishijima, M. Lin, and S. Tomioka, "The basic characteristics of tapped-inductor buck converter," IEICE Trans. Commun. (Japanese edition), vol.J101-B, no.1, pp.41–50, Jan. 2018.
[30] K. Nishijima, "A two-phase four-parallel coupled-inductor converter with voltage dividing capacitors," IEICE Trans. Commun. (Japanese edition), vol.J101-B, no.2, pp.179–186, Feb. 2018.
[31] K. Hirose and F. Kurokawa, "380 Vdc power supply and distribution system," IEICE Trans. Commun. (Japanese edition), vol.J101-B, no.11, pp.902–918, Nov. 2018.
[32] M. Oku and T. Tanaka, "On steady-state analysis of current-resonant half-wave push-pull converter," IEICE Trans. Commun. (Japanese edition), vol.J103-B, no.1, pp.11–21, Jan. 2020.
[33] E. Firmansyah, S. Tomioka, S. Abe, M. Shoyama, and T. Ninomiya, "Totem-pole power-factor-correction converter under critical-conduction-mode interleaved operation," IEICE Trans. Commun., vol.E93-B, no.9, pp.2250–2256, Sept. 2010.
[34] S. Abe, S. Yang, M. Shoyama, T. Ninomiya, A. Matsumoto, and A. Fukui, "Malfunction issue of SiC-SIT based DC circuit breaker in 400 VDC power distribution systems for data centers," IEICE Trans. Commun., vol.E95-B, no.6, pp.1990–1996, June 2012.
[35] M. Uno and A. Kukita, "Two-switch voltage equalizer using a series-resonant voltage multiplier operating in frequency-multiplied discontinuous conduction mode for series-connected supercapacitors," IEICE Trans. Commun., vol.E98-B, no.5, pp.842–853, May 2015.
[36] Y. Ishikura, T. Hosotani, and M. Yamamoto, "Bidirectional converter using multi-stage FET driving technique," IEICE Trans. Commun. (Japanese edition), vol.J103-B, no.4, pp.154–161, April 2020.
[37] H. Ohashita, I. Omura, S. Matsumoto, Y. Sato, H. Tadano, and I. Ishii, "Power electronics innovation with next generation advanced power devices," IEICE Trans. Commun., vol.E87-B, no.12, pp.3422–3429, Dec. 2004.
[38] M. Higashiwaki, A. Kuramata, H. Murakami, and Y. Kumagai, "Current status of development on gallium oxide power devices," IEICE Trans. Electron. (Japanese edition), vol.J99-C, no.9, pp.448–455, Sept. 2016.
[39] T. Kachi, "Next generation power devices for automobile applications — Challenge of GaN power devices —," IEICE Trans. Electron. (Japanese edition), vol.J103-C, no.7, pp.331–340, July 2020.
[40] T. Mizoguchi, T. Ninomiya, T. Ohgai, and M. Shoyama, "A family of single-switch ZVS-CV DC-to-DC converters," IEICE Trans. Commun., vol.E79-B, no.6, pp.849–856, June 1996.
[41] E. Hiraki, Y. Hirota, M. Nakaoka, T. Horiuchi, and Y. Sugawara, "Power loss estimation analysis based on experimental power switching device data for three-phase ARCP assisted soft-switching inverter," IEICE Trans. Commun., vol.E87-B, no.5, pp.1366–1372, May 2004.
[42] Y. Lee, Y. Chiu, M. Cheng, Y. Ko, and S. Hsiao, "Inverting quasi-resonant switched-capacitor bidirectional converter and its application to battery equalization," IEICE Trans. Commun., vol.E92-B, no.4, pp.1326–1336, April 2009.
[43] Y. Lee, Y. Chiu, M. Cheng, Y. Ko, and S. Hsiao, "Inverting quasi-resonant switched-capacitor bidirectional converter and its application to battery equalization," IEICE Trans. Commun., vol.E92-B, no.4, pp.1326–1336, April 2009.
[44] M. Ochiai and H. Matsuo, "High power factor current resonant type converter," IEICE Trans. Commun. (Japanese edition), vol.J85-B no.9, pp.1652–1660, Sept. 2002.
[45] C. Kang, K. Harada, H. Sakamoto, and H. Kim, "Soft switching of half-bridge converter using core saturation," IEICE Trans. Commun. (Japanese edition), vol.J86-B, no.3, pp.552–559, March 2003.
[46] M. Yoshida, Y. Hirota, E. Hiraki, and M. Nakaoka, "Comparative electromagnetic noise evaluations of ZVZCS resonant snubber and ZVS resonant snubber-assisted soft-switching PWM inverters," IEICE Trans. Commun. (Japanese edition), vol.J87-B, no.5, pp.726–732, May 2004.
[47] S. Abe, T. Zaitsu, J. Yamamoto, S. Ueda, and T. Ninomiya, "Synchronous rectifier driving technique for LLC current resonant converter without signal sensing," IEICE Trans. Commun. (Japanese edition), vol.J97-B, no.5, pp.375–382, May 2014.
[48] M. Yamamoto, "Discussion of SiC/GaN power semiconductor devices technical and market trends for next generation automotive applications from model 3 (Tesla) disassembled analysis," IS09 Next Steps for Transportation Electronics Technologies, APEC 2021.
[49] On Semiconductor, "SiC MOSFETs: Gate Drive Optimization," 2018. (online), https://www.onsemi.jp/pub/collateral/TND6237-D.PDF
[50] ROHM Co. Ltd, "Application example of SiC power devices," 2016, [Online], https://www.rohm.com/application-examples/sic
[51] ROHM Co. Ltd, "SiC Power Module BSM300D12P2E001 Data sheet," 2, 2018. [Online], https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/power_module/bsm300d12p2e001-e.pdf

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