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FOREWORD

Special Section on VLSI Design and CAD Algorithms

On behalf of the Guest Editors, I am pleased to present this special section on VLSI design and CAD algorithms. From 2021, every industry in world-wide has been suffered from supply shortage of semiconductor devices. The importance of VLSI is well accepted and the improvement in VLSI design and CAD area is requested. These special sections aim to provide new VLSI design methodology and CAD algorithms to produce coming semiconductor VLSIs. These special sections help researchers to have the opportunity to get state-of-the-art of work on VLSI design and CAD algorithms.

In this special section, we have received 9 papers. We made thorough reviews, had online paper selection meetings of all editorial committee members, and finally selected 8 papers. These papers are categorized into 4 topics: 1) Hardware Implementations and Design Examples, 2) Verification and Test, 3) Low Power, and 4) EDA, PDK, and IP. They cover a wide variety of research areas.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on judging the quality of papers. I should thank Professor Toshiki Kanamoto from Hirosaki University and Professor Takashi Matsumoto from University of Tokyo for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

Toshihiro Hattori, Guest Editor-in-Chief

Toshihiro Hattori *(Member)* received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Japan, in 1983 and 1985, respectively. He received the Ph.D in informatics from Kyoto University, Japan, in 2006. He joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, in 1985. From 1992 to 1993 he was a Visiting Researcher at the University of California Berkeley, with a particular interest in CAD. He joined the Semiconductor Integrated Circuits Division in Hitachi Ltd. in 1995. He moved to Renesas Technology Corp. in 2003. He was belonging to SuperH (Japan), Ltd. from 2001 to 2004. He moved to Renesas Electronics Corp. in 2010. He moved to Renesas Mobile Corp. as VP of SoC design in 2010. He is currently working with Renesas Electronics Corp. as Senior Director, Digital Products Business, Automotive Solution Business Unit. He is a member of IEEE, ACM, IEICE, and IPSJ.