PAPER

# Analytical Model of Maximum Operating Frequency of Class-D ZVS Inverter with Linearized Parasitic Capacitance and any Duty Ratio

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**SUMMARY** This paper proposes an analytical model of maximum operating frequency of class-D zero-voltage-switching (ZVS) inverter. The model includes linearized drain-source parasitic capacitance and any duty ratio. The nonlinear drain-source parasitic capacitance is equally linearized through a charge-related equation. The model expresses the relationship among frequency, shunt capacitance, duty ratio, load impedance, output current phase, and DC input voltage under the ZVS condition. The analytical result shows that the maximum operating frequency under the ZVS condition can be obtained when the duty ratio, the output current phase, and the DC input voltage are set to optimal values. A 650 V/30 A SiC-MOSFET is utilized for both simulated and experimental verification, resulting in good consistency.

***key words:*** *class-D ZVS inverter, maximum operating frequency, nonlinear drain-source parasitic capacitance, any duty ratio*

## 1. Introduction

The class-D inverter [1]–[16] is a classical circuit to convert DC power to AC power. The main advantage of the class-D inverter is the low switch voltage stress. Hence, it is widely applied as DC-DC resonant converters [17]–[19], induction heating [4], wireless power transmission [20]–[26], induction lamp [27], and radio transmitter [28]. With the help of wide band-gap power device, the class-D inverter can operate in high-frequency of megahertz (MHz) [24]–[26]. Although the high-frequency operation can realize high-power density, therewith increased switching loss and noise becomes a problem. By adopting zero-voltage-switching (ZVS) [29]–[41] technology, the problem of high switching loss and noise can be improved. And if the frequency limitation under the ZVS condition could be found, it is possible for the class-D inverter to operate at the maximum frequency under the ZVS condition, achieving the highest power density with relative low switching loss and noise. In addition, the frequency design of the class-D ZVS inverter could be more convenient if the frequency limitation is known. Totally, it is meaningful to analyze the maximum operating frequency of the class-D ZVS inverter.

As there are a lot of parameters related to the ZVS condition, it is necessary to combine all these parameters to build an analytical model to analyze the optimal parameters for achieving the maximum operating frequency under the ZVS condition. According to [37], the shunt capacitance is a key parameter to determine the frequency under the ZVS condition. Normally, the shunt capacitance is formed by the sum of both the linear external capacitor and the nonlinear parasitic capacitance. In low-frequency analysis, the required linear external capacitor is much larger than the nonlinear parasitic capacitance, so the nonlinear parasitic capacitance can be neglected. But in high-frequency analysis, the external linear capacitor becomes much smaller, and the nonlinear parasitic capacitance takes up a certain proportion of the total shunt capacitance. Therefore, the nonlinear parasitic capacitance cannot be neglected in the high-frequency analysis. Otherwise, the analyzed parameters may not accurately satisfy the ZVS condition when operating at high operating frequency.

According to [38], the duty ratio is another key parameter to determine the operating frequency under the ZVS condition. If the analysis model is built with a fixed duty ratio, the obtained maximum operating frequency by the model is only applicable to the assumed duty. Therefore, it is necessary to build the model with any duty ratio so that the obtained maximum operating frequency is applicable to all the duty ratios. Furthermore, as the duty is also related to the output voltage [39], it is possible to reconcile the power analysis under ZVS condition with the proposed model.

There are some previous researches about the analytical model of maximum operating frequency of class-D ZVS inverter. In [36], the model was mathematically built within the assumption of duty $D = 0.25$, and the neglect of the nonlinear parasitic capacitance. Thus, the frequency under the ZVS condition cannot be analyzed by other duty ratios, and the designed parameter of shunt capacitance may not satisfy the ZVS condition accurately especially when operating at a high frequency. In [37], the model was built within the nonlinear parasitic capacitance and assumption of $D = 0.25$. Thus, the shunt capacitance can be designed accurately to satisfy the ZVS condition, but the frequency still cannot be analyzed for other duty ratios. In [38], the model was built within the any duty ratio and neglect of nonlinear parasitic capacitance. Thus, it remained the same problem as [36]. In [40], both the nonlinear parasitic capacitance and the any duty ratio were considered to build the model based on [38]. However, when the two varieties were included in the cir-

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cuit formulas simultaneously, the derivation for the model becomes too complicated to conduct. Therefore, there was no analytical model built in [40]. Furthermore, for all the models above, there was no simulated and experimental verification for the frequency analysis. Totally, as there is still no analytical model built within both the nonlinear parasitic capacitance and any duty ratio, it is not reliable and convenient for circuit designers to design the shunt capacitance accurately and the duty ratio freely under the ZVS condition especially in high frequency operation.

Based on the researched models, this paper proposes a new analytical model built with both the nonlinear parasitic capacitance and any duty ratio within simulated and experimental verification. As it is difficult to derive the model when both the nonlinear parasitic capacitance and any duty ratio are directly contained in the equations, the parasitic capacitance is first linearized through the charge-related equation, resulting in a monotone decreasing function of the DC input voltage. With the same derivation method in [38], all the parameters related to the ZVS condition are combined into two frequency-related equations according to ZVS condition and the fundamental frequency component approximation. The frequency analysis model under the ZVS condition is solved by combining the equations. The analytical result shows that when the load impedance and DC input voltage are fixed, the maximum operating frequency under the ZVS condition can always be obtained at 0° output current phase and 0.25 duty ratio. Upon the condition of fixed load impedance, 0° output current phase and 0.25 duty ratio. Furthermore, if the DC input voltage is undetermined, it is analyzed that higher maximum operating frequency can be obtained with higher DC input voltage under the ZVS condition, and it is limited by the highest DC input voltage. As for verification, a 650 V/30 A SiC-MOSFET is utilized to frame the class-D ZVS inverter circuit. The nonlinear parasitic capacitance of the SiC-MOSFET is accurately modeled and linearized for verification. The ZVS operation is verified by simulation within comparing to the conventional model and is further verified by experiment with little error. The maximum frequency is verified with various DC input voltage of 400 V, 300 V, 200 V by simulation and with that of 300 V, 200 V by experiment. The results show that in condition of 0° output current phase and 0.25 duty ratio, the maximum operating frequency for 300 V DC input can be obtained higher than that of 200 V. And the highest maximum operating frequency is obtained by the highest DC input voltage of 400 V. Both results show good consistency with analysis.

## 2. Class-D ZVS Inverter

### 2.1 Circuit

A typical circuit of the class-D ZVS series-resonant inverter is shown in Fig. 1. The inverter is composed of a DC voltage source $V_I$, two identical switching MOSFETs $M_1$ and $M_2$ which are connected in half-bridge, a series-resonant tank $L_r$–$C_r$, and a load resistance R. Each switch contains

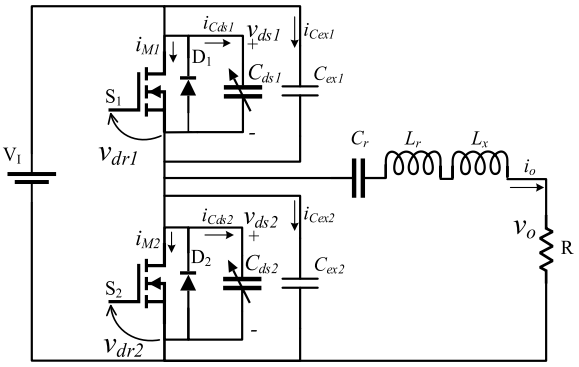


**Fig. 1** Typical class-D inverter topology.

a nonlinear parasitic capacitance $C_{ds}$ and a parasitic body-diode, and there is an extra linear capacitor connected in parallel with the drain-source. For ZVS operation, the shunt capacitance and inductive load are necessary. The shunt capacitance is formed by the nonlinear parasitic capacitance and the extra linear capacitor. And the extra inductor $L_x$ makes the load impedance inductive.

### 2.2 ZVS Operation

Figure 2 shows the nominal waveforms of the class-D ZVS inverter. The $\omega = 2\pi f$ expresses the angular frequency and $\theta = \omega t$ expresses the angular time. The switch is assumed to be ideal. The switches are driven by a set of pluses $v_{\mathrm{dr1}}$ and $v_{\mathrm{dr2}}$ with duty ratio $D$ at frequency $f$ respectively. The output current's phase angle lags behind that of the output voltage by $\varphi$. During the deadtime $t_{\mathrm{d}}$, both switches are off, and the output current charges one shunt capacitance and discharge the other. When the low-side switch's voltage $v_{ds2}$ is discharged to zero, the current begins to flow through the body diode. If the turn-on voltage comes during the time interval $\pi$ to $\pi + \varphi$, the ZVS can be conducted.

## 3. Nonlinear Parasitic Capacitance Linearization

### 3.1 $C_{ds}$ Modeling

The typical definition equation of the nonlinear parasitic capacitance $C_{\mathrm{ds}}$ can be expressed by (1), where $C_{\mathrm{j0}}$ is the capacitance of $C_{ds}$ at $v_{ds} = 0$ V, $V_{\mathrm{bi}}$ is the built-in potential determined by the material of the switch, and m is the grading coefficient and it is typically to be 0.5.

$$C_{ds}\left(v_{ds}\right) = \frac{C_{j0}}{\left(1 + \frac{v_{ds}}{V_{bi}}\right)^{m}} \tag{1}$$

According to [40], the expression (1) can be mathematically transformed into (2), where $C_{\mathrm{DS}}(V_{\mathrm{DS}})$ is a specific value of capacitance at a specific drain-source voltage $V_{\mathrm{DS}}$. For a specific switch, the value of $C_{\mathrm{DS}}(V_{\mathrm{DS}})$ usually can be read from the datasheet.

$$C_{ds}\left(v_{ds}\right) = C_{DS}\left(V_{DS}\right)\sqrt{\frac{V_{DS} + V_{bi}}{v_{ds} + V_{bi}}} \tag{2}$$

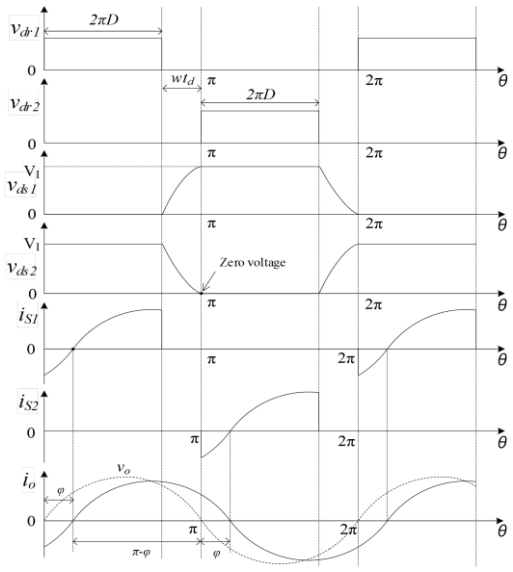


**Fig. 2** Nominal waveforms of class-D ZVS inverter.

### 3.2 $C_{ds}$ Linearization

As it is difficult to directly utilize the nonlinear parasitic capacitance to derivation, the nonlinear $C_{\rm ds}$ is proposed to be linearly transformed through the charge-related equation. When the $C_{\rm ds}$ is charged to $V_I$, the charge stored in the $C_{\rm ds}$ can be expressed as:

$$Q_{ds}(V_I) = \int_{-V_{bi}}^{V_I} C_{ds}(v_{ds})\, dv_{ds} \tag{3}$$

If there is a linear capacitance $C_{dseq}$ existed and satisfied the condition that when it is charged to $V_I$, the charge is the same as (3), thus the charge can be expressed by

$$Q_{ds}(V_I) = C_{dseq} V_I \tag{4}$$

Combine (4) with (3) and (2), the nonlinear $C_{ds}$ can be transformed into an equal linear capacitance shown by (5). As $V_{\rm bi}$, $C_{\rm DS}(V_{\rm DS})$, $V_{\rm DS}$ are constants in the function, it is obvious that the dependent variable $C_{dseq}$ is a monotone decreasing function of the independent variable $V_I$, which means with the increase of $V_I$, the $C_{dseq}$ decreases.

$$\begin{aligned} C_{dseq}(V_I) &= \frac{1}{V_I}\int_{-V_{bi}}^{V_I} C_{ds}(v_{ds})\, dv_{ds} \\ &= \frac{2C_{DS}(V_{DS})}{V_I}\sqrt{V_{DS}+V_{bi}}\sqrt{V_I+V_{bi}} \end{aligned} \tag{5}$$

### 3.3 Influence on Phase of Waveform by Linearization

In [37], the waveforms of low-side switch's drains-source voltage $v_{\rm ds2}$ under the ZVS condition was modeled by both nonlinear capacitance and linear capacitance. The result has proved that the linearities or nonlinearities never affect the phase angle of the drain-source voltage as well as that of the output current under the ZVS condition.

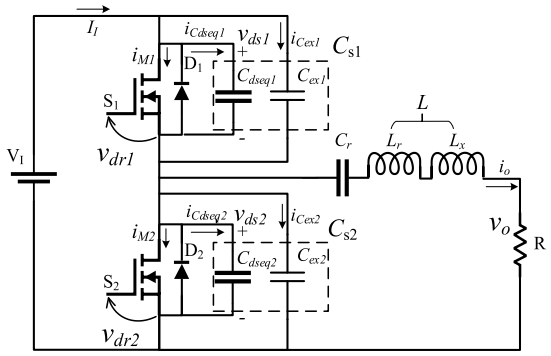


**Fig. 3** Equivalent circuit for analysis.

## 4. Circuit Modeling

### 4.1 Assumptions

In this section, the frequency-related parameters' relationship of the class-D ZVS inverter is given by mathematical equations. The equivalent circuit including the linearized parasitic capacitance for analysis is shown in Fig. 3 and it is based on the following assumptions:

*1)* The shunt capacitance is formed by both the linearized parasitic capacitance and the linear external capacitor.

*2)* The switch is assumed ideal in this circuit, meaning zero-switching time, zero on-resistances, and infinite off-resistances.

*3)* The gate-driving voltages are ideal symmetric square waveforms, and their duty ratios range by $0 \le D \le 0.5$.

*4)* The loaded quality factor $Q_{\rm L}$, which is defined as

$$Q_L = \frac{\omega L}{R} \tag{6}$$

expresses the ratio of reactive power for resonant tank to the true power for load [39]. Here it is assumed to be sufficiently high so that the resonant can be ideal and the output current can be regarded as a sinusoidal wave as

$$i_o = \frac{V_m}{R}\sin(\omega t - \varphi) = I_m \sin(\omega t - \varphi) \tag{7}$$

where $V_m$ and $I_m$ are the amplitudes and the $\varphi$ is the phase difference compared to the output voltage.

*5)* Only the fundamental frequency component remains from the resonant filter. It is well known that the resonant filter should be inductive for achieving the ZVS condition. Therefore, the resonant inductance $L$ is divided into $L_r$ and $L_x$ virtually, namely

$$L = L_r + L_x \tag{8}$$

The resonant filter $Lr$–$C_r$ is an ideal filter at the operating frequency $f$, that is, $f = 1/2\pi\sqrt{L_r C_r}$. Additionally, $L_x$ yields a phase shift of the output current.

*6)* All the components have no parasitic components, and both high-side and low-side are identical.

*7)* The switches' voltages satisfy the ZVS condition that

$$v_{ds1}(2\pi) = 0 \quad and \quad v_{ds2}(2\pi) = V_I \tag{9}$$

$$v_{ds1}(\pi) = V_I \quad and \quad v_{ds2}(\pi) = 0 \tag{10}$$

### 4.2 Waveform Equation Derivation

According to assumptions 3), 4), and the waveform of output current shown in Fig. 2, by KCL, the basic equation can be expressed as

$$\begin{aligned} &i_{M1} + (i_{Cdseq1} + i_{Cex1}) - \left[i_{M2} + \left(i_{Cdseq2} + i_{Cex2}\right)\right] \\ &= i_o = I_m \sin(\theta - \varphi) \end{aligned} \tag{11}$$

For $0 \le \theta \le 2\pi D$, switch $S_1$ is on state, and switch $S_2$ is off state, so the switch voltages are given as

$$v_{ds1} = 0, \quad v_{ds2} = V_I \tag{12}$$

As there is no current flowing through the switch $S_2$, and no current charged or discharged through the shunt capacitance $C_{s1}$ and $C_{s2}$, thus the currents become

$$i_{M2} = i_{Cdseq1} = i_{Cdseq2} = i_{Cex1} = i_{Cex2} = 0 \tag{13}$$

Substituting (13) into (11), it can be obtained that

$$i_{M1} = i_o = I_m \sin(\theta - \varphi) \tag{14}$$

For $2\pi D \le \theta \le \pi$, which is the dead time interval, both $S_1$ and $S_2$ are off. Therefore, the switches' currents are

$$i_{M1} = i_{M2} = 0 \tag{15}$$

Additionally, the voltage relationship between the two switches is

$$v_{ds1} = V_I - v_{ds2} \tag{16}$$

From (11) and (15), it can be obtained that

$$i_{Cdseq1} + i_{Cex1} - (i_{Cdseq2} + i_{Cex2}) = i_o = I_m \sin(\theta - \varphi) \tag{17}$$

According to the definition of the capacitance current, it can be obtained from (17) that

$$\begin{aligned} &\omega \left(C_{dseq1} + C_{ex1}\right) \frac{dv_{ds1}}{d\theta} - \omega \left(C_{dseq2} + C_{ex2}\right) \frac{dv_{ds2}}{d\theta} \\ &= I_m \sin(\theta - \varphi) \end{aligned} \tag{18}$$

By rearranging (18) by using (16), it can be obtained that

$$\omega \left(C_{dseq1} + C_{ex1} + C_{dseq2} + C_{ex1}\right) \frac{dv_{ds2}}{d\theta} = I_m \sin(\theta - \varphi) \tag{19}$$

Define the total sum of the shunt capacitance as

$$C_{st} = C_{s1} + C_{s2} = C_{dseq1} + C_{ex1} + C_{dseq2} + C_{ex2} \tag{20}$$

Hence

$$\omega C_{st} dv_{ds2} = I_m \sin(\theta - \varphi) d\theta \tag{21}$$

Because of $v_{ds2}(2\pi D) = V_I$, it can be obtained by solving indefinite integral for both sides.

$$\omega C_{st} \int_{V_I}^{v_{ds2}} dv_{ds2} = \int_{2\pi D}^{\theta} I_m \sin(\theta - \varphi) d\theta \tag{22}$$

Yields,

$$\begin{aligned} v_{ds2} &= V_I + \frac{I_m}{\omega C_{st}} [\cos(\theta - \varphi) - \cos(2\pi D - \varphi)] \\ &= V_I + \frac{V_m}{\omega C_{st} R} [\cos(\theta - \varphi) - \cos(2\pi D - \varphi)] \end{aligned} \tag{23}$$

For $\pi \le \theta \le \pi + 2\pi D$, switch $S_1$ is off state, and switch $S_2$ is on state, so the switch voltages are given as

$$v_{ds1} = V_I, \quad v_{ds2} = 0 \tag{24}$$

Similar with (13), the currents are

$$i_{M1} = i_{Cdseq1} = i_{Cdseq2} = i_{Cex1} = i_{Cex2} = 0 \tag{25}$$

Therefore, the current relationship is expressed as

$$i_{M2} = -i_o = -I_m \sin(\theta - \varphi) \tag{26}$$

For $\pi + 2\pi D \le \theta \le 2\pi$, which is the dead time interval, both $S_1$ and $S_2$ are off. The relationship between switches' currents and voltages are the same as (15)–(19). As $v_{ds2}(\pi + 2\pi D) = 0$, it can be obtained by following the similar procedure of the time interval $2\pi D < \theta \le \pi$ that

$$\omega C_{st} \int_{0}^{v_{ds2}} dv_{s2} = -I_m \int_{\pi + 2\pi D}^{\theta} \sin(\theta - \varphi) d\theta \tag{27}$$

Yields,

$$\begin{aligned} v_{ds2} &= \frac{I_m}{\omega C_{st}} [\cos(\theta - \varphi) + \cos(2\pi D - \varphi)] \\ &= \frac{V_m}{\omega C_{st} R} [\cos(\theta - \varphi) + \cos(2\pi D - \varphi)] \end{aligned} \tag{28}$$

### 4.3 ZVS Condition

According to (10), substituting the ZVS condition $v_{ds2}(\pi) = 0$ to (23), we have

$$V_m = \frac{\omega C_{st} R}{2 \cos(\pi D - \varphi) \cos \pi D} V_I \tag{29}$$

(29) expresses the relationship between the output voltage amplitude and DC input voltage, under the ZVS condition. For $2\pi D \le \theta \le \pi$, $v_{ds2}$ decreases from $V_I$ by the discharging of $C_{s2}$, therefore, the derivative of $v_{ds2}$ should be minus or zero [38]. When the derivative is just equal to zero at $\theta = \pi$, not only ZVS condition but also the class-DE

zero-derivative-switching (ZDS) condition is satisfied. The derivative can be expressed as

$$\alpha = \left.\frac{dv_{ds2}(\theta)}{d\theta}\right|_{\theta=\pi} = -\frac{V_m}{\omega C_{st} R}\sin\varphi \tag{30}$$

Substituting (29) into (30), we have

$$\alpha = -\frac{\sin\varphi}{2\cos(\pi D-\varphi)\cos\pi D} V_I \tag{31}$$

As discussed above, the derivative should be

$$\alpha \le 0 \tag{32}$$

## 5. Fourier Analysis

The Fourier expansion is utilized to derive another equation base on (29), so that the two equations can be combined to provide a further equation for frequency analysis. Besides, the relationship between the phase shift inductance $L_x$ and other parameters can also be figured out, providing the precondition for designing the $L_x$ for ZVS condition.

The output voltage across the load resistance R and the phase shift inductance $L_x$ can be expressed as

$$v_o = Ri_o = RI_m\sin(\theta-\varphi) = V_m\sin(\theta-\varphi) \tag{33}$$

$$v_{Lx} = \omega L_x\frac{di_o}{d\theta} = \omega L_x I_m\cos(\theta-\varphi) = V_{Lx}\cos(\theta-\varphi) \tag{34}$$

From assumption 5), the voltage across the phase shift inductor $L_x$ and the load resistance R just constitute the fundamental-frequency component of the low-side switch voltage $v_{ds2}(\theta)$ for $0 \le \theta \le 2\pi$, where the voltage across $L_x$ is the cosine function part and the voltage across R is the sine function part. According to the principle of the Fourier series expansion, the sine function amplitude $V_m$ and the cosine function amplitude $V_{Lx}$ can be calculated by integrating the product of $v_{ds2}(\theta)$ and $\sin(\theta-\varphi)$ or $\cos(\theta-\varphi)$ in the time interval $0 \le \theta \le 2\pi$. Therefore, from (23), (28), it can be obtained that

$$\begin{aligned} V_m = RI_m &= \frac{1}{\pi}\int_0^{2\pi} v_{ds2}(\theta)\sin(\theta-\varphi)d\theta \\ &= \frac{1}{\pi}\left\{\int_0^{2\pi D} V_I\sin(\theta-\varphi)d\theta \right. \\ &\quad + \int_{2\pi D}^{\pi}\left\{V_I + \frac{V_m}{\omega C_{st}R}[\cos(\theta-\varphi)-\cos(2\pi D-\varphi)]\right\}\sin(\theta-\varphi)\,d\theta \\ &\quad \left. + \int_{\pi+2\pi D}^{2\pi}\frac{V_m}{\omega C_{st}R}[\cos(\theta-\varphi)+\cos(2\pi D-\varphi)]\sin(\theta-\varphi)d\theta\right\} \end{aligned} \tag{35}$$

$$\begin{aligned} V_{Lx} = wL_xI_m &= \frac{1}{\pi}\int_0^{2\pi} v_{s2}(\theta)\cos(\theta-\varphi)d\theta \\ &= \frac{1}{\pi}\left\{\int_0^{2\pi D} V_I\cos(\theta-\varphi)d\theta \right. \\ &\quad + \int_{2\pi D}^{\pi}\left\{V_I + \frac{V_m}{\omega C_{st}R}[\cos(\theta-\varphi)-\cos(2\pi D-\varphi)]\right\}\cos(\theta-\varphi)d\theta \\ &\quad \left. + \int_{\pi+2\pi D}^{2\pi}\left(\frac{V_m}{\omega C_{st}R}[\cos(\theta-\varphi)+\cos(2\pi D-\varphi)]\right)\cos(\theta-\varphi)d\theta\right\}V_I \end{aligned} \tag{36}$$

The solution of $V_m$ and $V_{Lx}$

$$\begin{aligned} V_m = 2V_I\cos\varphi\left\{\pi + \frac{1}{\omega C_{st}R}\left[\frac{1}{2}\cos 2\varphi + \frac{1}{2}\cos(4\pi D-2\varphi)\right.\right. \\ \left.\left. + \cos(2\pi D-2\varphi) + \cos 2\pi D + 1\right]\right\}^{-1} \end{aligned} \tag{37}$$

$$\begin{aligned} V_{Lx} = \omega L_x I_m = \frac{V_I}{\pi}\left\{2\sin\varphi + \left[\pi - 2\pi D - \frac{1}{2}\sin(4\pi D-2\varphi)\right.\right. \\ \left.\left. + \sin(2\pi D-2\varphi) - \sin 2\pi D\right][2\cos\pi D\cos(\pi D-\varphi)]^{-1}\right\} \end{aligned} \tag{38}$$

Combine (37) with (29), a new equation within the angle frequency, total sum of shunt capacitance, duty, phase angle and the load impedance can be obtained that

$$\omega C_{st}R = \frac{\sin(2\pi D-2\varphi)\sin 2\pi D}{\pi} \tag{39}$$

It can be inferred that $\omega C_{st}R$ can be a function of $\varphi$ when $D$ is fixed. For the range of $\varphi$, according to $\alpha$ in (30), and $\omega C_{st}R$ in (39), the with the condition $\alpha \le 0$, and $\omega C_R \ge 0$, the range of $\varphi$ can be limited to

$$0 \le \varphi \le \pi D \tag{40}$$

## 6. Maximum Operating Frequency Analysis

Figure 4 shows the plotted the graph of the function $\omega C_{st}R$ when $\varphi$ is the variable and $D$ is the stepped constant. The value of $\omega C_{st}R$ can be obtained with varies conditions of $\varphi$ and $D$. When $\varphi = 0°$ and $D = 0.25$, the $\omega C_{st}R$ reaches its maximum value of 0.318 (which is circled by red). Additionally, when $\varphi = 0°$, the $\omega C_{st}R$ increases from $D = 0.05$ to 0.25 and decreases from $D = 0.25$ to 0.45. This is an important characteristic for frequency design with various duty ratios. For $\omega = 2\pi f$, the maximum value of $\omega C_{st}R$ obtained at $\varphi = 0°$ and $D = 0.25$ can be expressed by (41).

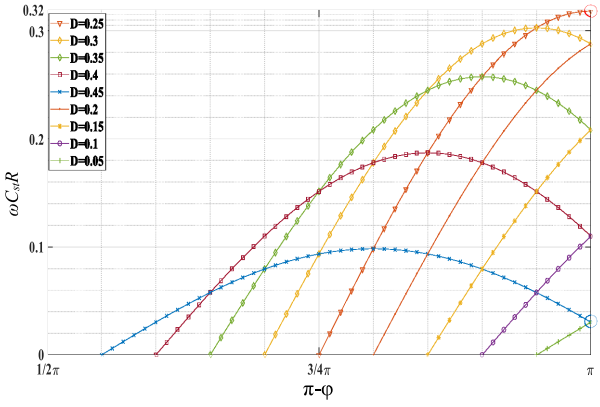


**Fig. 4** $\omega C_{st}R$ as a function of $\varphi$ and $D$.

$$(2\pi f C_{st} R)_{\max} = 0.318 \tag{41}$$

There are two steps for analysis of (41). From (5), when the DC input voltage $V_I$ is determined, the linearized parasitic capacitance $C_{dseq}$ is determined. As the external capacitance $C_{ex}$ is initially constant, the sum of shunt capacitance $C_{st}$ can be determined. For R is usually 50 Ω in high frequency system, it can also be regarded constant. Thus, (41) can be rewritten to (42), meaning that with any determined $V_I$ and $C_{st}$, the condition to obtain the maximum operating frequency $f_{max}$ at any $\varphi$ and $D$ is that $\varphi = 0°$ and $D = 0.25$.

$$f_{\max} = \frac{0.318}{2\pi R C_{st}} \tag{42}$$

Furthermore, when the DC input voltage $V_I$ is undetermined, the $C_{dseq}$ becomes a variate, so do the $C_{st}$. Thus, (42) can be furtherly rewritten to (43). It means that upon the condition of $\varphi = 0°$ and $D = 0.25$, for undetermined $V_I$ and $C_{st}$, the maximum frequency $f_{max}$ will increase with the decrease of $C_{st}$, and it will reach its highest value as $f'_{\max}$ when the $C_{st}$ reaches its minimum as $C_{st\text{-}min}$.

$$f'_{\max} = \frac{0.318}{2\pi R C_{st\text{-}\min}} \tag{43}$$

To obtain the $C_{st\text{-}min}$, both the external capacitor and linearized parasitic capacitance should be minimum. As the external capacitors $C_{ex1}$, $C_{ex2}$ can be removed from the circuit, they can be zero. Therefore, solving the $C_{st\text{-}min}$ becomes a case of solving the minimum value of the sum of $C_{dseq1}$ and $C_{dseq2}$, which is

$$\begin{aligned} C_{st-\min} &= C_{dseq1-\min} + C_{ex1-\min} + C_{dseq2-\min} + C_{ex2-\min} \\ &= 2C_{dseq-\min} \end{aligned} \tag{44}$$

According to the monotone decreasing property of (5), the minimum of linearized parasitic $C_{dseq\text{-}min}$ can be obtained when $V_I$ is determined to its maximum value, thus

$$\begin{aligned} C_{st-\min} &= 2C_{dseq-\min} = 2C_{dseq}(V_{I-\max}) \\ &= \frac{4C_{DS}(V_{DS})}{V_{I-\max}} \sqrt{V_{DS} + V_{bi}} \sqrt{V_{I-\max} + V_{bi}} \end{aligned} \tag{45}$$

Substitute (45) into (43), the relationship between the maximum frequency $f'_{max}$ and the maximum DC input voltage $V_{I\text{-}max}$ can be expressed as (46), where $V_{DS}$, $C_{DS}(V_{DS})$, $V_{bi}$ and R are constant.

$$f'_{\max} = \frac{0.318 V_{I-\max}}{8\pi C_{DS}(V_{DS}) R \sqrt{V_{DS} + V_{bi}} \sqrt{V_{I-\max} + V_{bi}}} \tag{46}$$

(46) indicates that under the condition of $\varphi = 0°$ and $D = 0.25$, the operating frequency $f_{max}$ under the ZVS condition is a monotone increasing function of the DC input voltage $V_I$, and the highest maximum operating frequency $f'_{max}$ under the ZVS condition can be obtained at the highest DC input voltage $V_{I\text{-}max}$. Totally, the optimal condition for the class-D inverter achieving its maximum operating frequency under the ZVS condition is $\varphi = 0°$, $D = 0.25$ and the highest DC input voltage.

## 7. Design Equation

From the expressions analyzed above, the design equations of the resonant components such as resonant capacitor $C_r$, resonant inductor $L_r$, phase shift inductor $L_x$ for the high-frequency class-D inverter under the ZVS condition can be obtained as below:

From (38), $L_x$ can be solved as

$$\begin{aligned} L_x = \frac{1}{\pi\omega^2 C_{st}} \Big[ &\pi - 2\pi D + 4\sin\varphi \cos\pi D \cos(\pi D - \varphi) \\ &- \frac{1}{2}\sin\varphi + \frac{1}{2}\sin(4\pi D - 2\varphi) + \sin(2\pi D - 2\varphi) - \sin 2\pi D \Big] \end{aligned} \tag{47}$$

Therefore, from (6) and (8), we have

$$L_r = L - L_x = \frac{Q_L R}{\omega} - L_x \tag{48}$$

Therefore, $C_r$ can be solved as

$$C_r = \frac{1}{(2\pi f)^2 L_r} \tag{49}$$

## 8. Verification

### 8.1 $C_{ds}$ Modeling of a 650 V/30 A SiC-MOSFET

According to the datasheet of the 650 V/30 A SiC-MOSFET [41], the value of $C_{DS}(V_{DS})$ at $V_{DS}$ = 500 V can be calculated to 20 pF, for $C_{DS}(500\,\text{V}) = C_{OSS}(500\,\text{V}) - C_{RSS}(500\,\text{V})$. The built-in potential $V_{bi}$ can be calculated according to the definition formulas and parameters in [42] and the value for SiC-MOSFET at room temperature is calculated as $V_{bi}$ = 2.996 V. As shown in Fig. 5, The model of the $C_{ds}$ with the two initially valued parameters is plotted and compared with the reference points extracted from the datasheet. As there is a large gap, the two parameters are fitted step by step and finally optimized as $C_{DS}(500\,\text{V})$ = 32 pF, $V_{bi}$ = 2 V. Thus, the final model of $C_{ds}$ of the 650 V/30 A SiC-MOSFET.

$$C_{ds}(v_{ds}) = 32 \times 10^{-12} \times \sqrt{\frac{502}{v_{ds} + 2}} \tag{50}$$

And the model of linearized capacitance is

$$C_{dseq(M)}(V_I) = \frac{64 \times 10^{-12}}{V_I} \sqrt{502} \sqrt{V_I + 2} \tag{51}$$

Figure 6 illustrates the function of $C_{dseq(M)}$ given by (51). The function is monotone decreasing which proves the analysis in (5). Note that Fig. 6 is not the physical characteristics of the $C_{dseq(M)}$, it is just a calculated result.

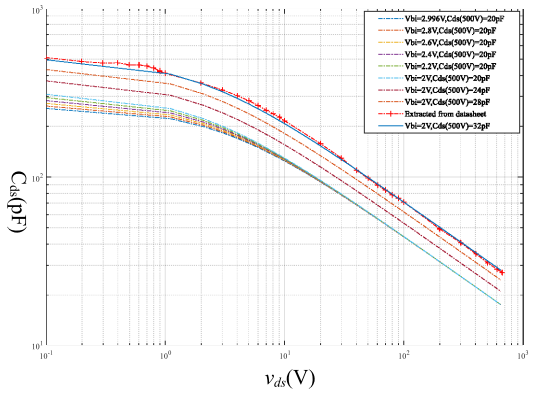


**Fig. 5** Graph plotting of $C_{ds}$ model with fitted $C_{DS}(V_{DS})$ and $V_{bi}$.

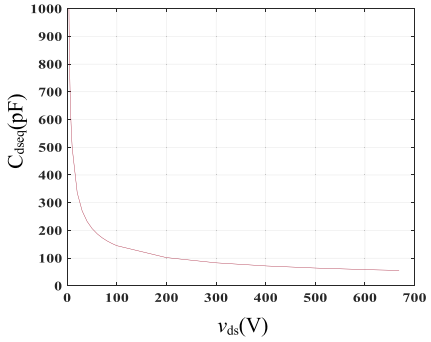


**Fig. 6** Plotted graph of the $C_{dseq}$.

**Table 1** Maximum operating frequency of each DC input voltage.

| Input voltage | Maximum frequency |
|---|---|
| 400V | 7.041MHz |
| 350V | 6.584MHz |
| 300V | 6.094MHz |
| 250V | 5.558MHz |
| 200V | 4.967MHz |
| 150V | 4.294MHz |
| 100V | 3.495MHz |
| 50V | 2.447MHz |

Typically, the maximum input voltage of a switch is about 60% of its break-down voltage due to the high voltage surge occurred in the high-frequency system. For the 650 V/30 A SiC-MOSFET, 400 V can be considered as a proper maximum input voltage. Thus, according to (51), assuming R is fixed at 50 Ω, the maximum operating frequency of the class-D ZVS inverter with the 650 V/30 A SiC-MOSFET can be calculated as (52). For other DC input voltages, the corresponding maximum frequency of each voltage under ZVS condition can be calculated respectively shown as Table 1. It is seen that higher input DC voltage can obtain higher maximum operating frequency under the ZVS condition.

$$f_{\max(M)} = 7.041\,MHz \tag{52}$$

## 8.2 ZVS Operation Verification

In Fig. 4, the relationship among $\omega C_{st}R$, $\varphi$ and $D$ under the ZVS condition is plotted by graph. As the parasitic parameters like ESL and ESR may produce large error in experiment in megahertz frequency, here we just pick up the operation point in kilohertz frequency at $\varphi = 0°$, $D = 0.45$, which is circled by blue in Fig. 4 to verify the ZVS operation within small error. The value of $\omega C_{st}R$ at the $\varphi = 0°$, $D = 0.45$ can be read from the tool which is $\omega C_{st}R = 0.0304$. According to (51), when $V_I = 200$ V, the equal linearized capacitance of the 650 V/30 A MOSFET can be calculated as

$$C_{dseq(M)200\,V} \approx 101.901\,pF \tag{53}$$

According to (44), to obtain the maximum operating frequency at the point of $\varphi = 0°$, $D = 0.45$, we just use the switch's parasitic capacitance to form the shunt capacitance by minimum. Thus, the total shunt capacitance is just the sum of the linearized parasitic capacitance of both high-side and low-side, which is

$$C_{stmin} = 2C_{dseq(M)200\,V} = 203.802\,pF \tag{54}$$

As $\varphi = 0°$, $D = 0.45$, $\omega C_{st}R = 0.0304$, $\omega = 2\pi f$, assuming R = 50 Ω, the frequency under minimum shunt capacitance $C_{stmin}$ can be calculated as

$$f = \frac{0.0304}{2\pi C_{stmin}R} \approx 474.804\,kHz \tag{55}$$

Substituting the determined values of $\omega = 2\pi f$, $C_{st}$, $\varphi$, $D$ to (47), the phase shift inductance can be calculated as

$$L_x \approx 3.554\,uH \tag{56}$$

From assumption 4), it is supposed that the loaded quality factor $Q_L$ should be set sufficiently high. In [39], $Q_L$ is supposed to larger than 2.5. In [38], $Q_L$ is set to 3. Here we set it enough high by 5. Thereupon, with the determined frequency $f$, the total inductance can be calculated as

$$L = \frac{Q_L R}{2\pi f} \approx 83.766\,uH \tag{57}$$

Thus, the resonant inductance can be calculated as

$$L_r = L - L_x = 80.211\,uH \tag{58}$$

And capacitor can be calculated as

$$C_r = \frac{1}{(2\pi f)^2 L_r} \approx 1.400\,nF \tag{59}$$

On the other hand, to demonstrate the influence on ZVS operation when the nonlinear parasitic capacitance is neglected. Here, the corresponding parameters are designed again through the conventional model in [38] with the same condition of $\varphi = 0°$, $D = 0.45$, $\omega C_{st}R = 0.0304$, $f =$

**Table 2** Parameters of conventional and proposed model.

| Parameter | Symbol | Conventional | Proposed |
|---|---|---|---|
| Duty | $D$ | 0.45 | 0.45 |
| Input voltage | $V_I$ | 200V | 200V |
| Switching frequency | $f$ | 474.8KHz | 474.8KHz |
| External capacitor | $C_{ex}$ | 101.901pF | 0pF |
| Parasitic capacitance | $C_{ds}$ | (Neglected) | 101.901pF (Linearized) |
| Loaded quality factor | $Q_L$ | 5 | 5 |
| Total inductor | $L$ | 83.766uH | 83.766uH |
| Resonant capacitor | $C_r$ | 1.400nF | 1.400nF |
| Load resistance | R | 50Ω | 50Ω |

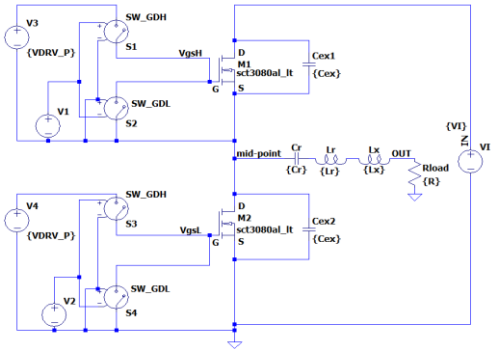


**Fig. 7** Simulation schematic.

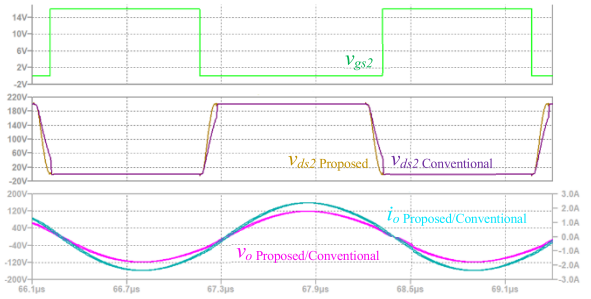


**Fig. 8** Simulated waveforms.

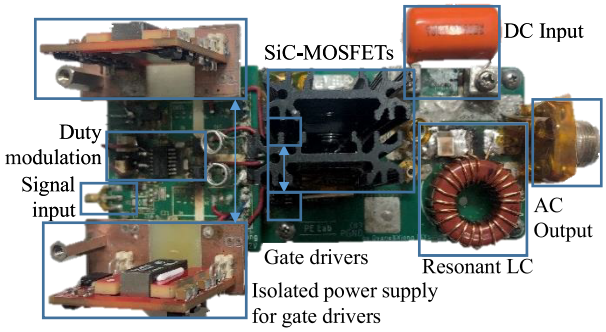


**Fig. 9** PCB prototype for experimental verification.

474.804 KHz, R = 50 Ω as above. Thus, the required total sum of capacitance can be calculated as

$$C_{st(con)} = \frac{0.0304}{2\pi f R} \approx 203.802\,pF \tag{60}$$

As the nonlinear parasitic capacitance are neglected in [38], they become zero. Thus, the shunt capacitance is all composed by the external capacitor. Therefore,

$$C_{ext(con)} = C_{st(con)} = 203.802\,pF \tag{61}$$

Thus, the required external capacitor of each side is

$$C_{ex(con)} = \frac{1}{2}C_{ext(con)} = 101.901\,pF \tag{62}$$

The design of other parameters in [38] are same with the proposed model, and the calculated results are listed by Table 2. As the parasitic capacitance is considered in the proposed model, it forms required the shunt capacitance with linearized capacitance so that the external capacitor is not needed. On the other hand, the parasitic capacitance in the conventional model is neglected so that the required shunt capacitance needs to be formed all by the external capacitor.

The verification is conducted by spice simulation. The simulation schematic within the 650 V/30 A SiC-MOSFET spice model is shown by Fig. 7. Both switches are driven by a gate-driving voltage of 16 V. The ESR and ESL of wire are not set in the circuit to match the ideal condition assumed for the analytical model.

Figure 8 shows the waveforms of low-side gate driving voltage $v_{gs2}$, low-side drain-source voltage $v_{ds2}$, output current $i_o$ and output voltage $v_o$ are simulated by both conventional and proposed model. The result of proposed model shows that the turn-on edge of $v_{gs2}$ comes just directly after the $v_{ds2}$ (proposed) decreases to zero, meaning that the ZVS operation is successfully conducted. However, as for the result of conventional model, the $v_{ds2}$ (conventional) is still far from zero when the turn-on edge has come, meaning that the ZVS operation failed. Due to the neglect of the parasitic capacitance, the designed parameter of external capacitor by conventional model does not satisfy the ZVS condition accurately.

For experimental verification, Fig. 9 shows the prototype of the class-D ZVS inverter is made for the experimental verification. The switch of the 650 V/30 A SiC-MOSFET is utilized to the board. The resonant inductor is hand-made by a toroidal core with enameled copper wire. The resonant capacitors are used by the high-voltage multilayer ceramic capacitors (MLCC). The parameters of the components are precisely adjusted to match the simulation conditions. The load is used by a standard 50 Ω dummy load. The signal is generated by a 200 MHz low-noise function generator. The duty is adjustable via an RC integral circuit. The gate drivers are fed by the isolated DC-DC converters and provide a 16.2 V gate-driving voltage. Both SiC-MOSFETs are attached with the heatsinks and there are no external capacitors are paralleled with the drain-source.

Table 3 listed both simulated and experimental parameters. And Fig. 10 shows the experimental waveform in success of ZVS operation as well as simulation. Affected by the inevitable differences in the real components and the ESL, ESR in the PCB circuit, the measured condition to achieve

**Table 3** Conditions for ZVS operation verification.

| Parameter | Simulated | Measured |
|---|---|---|
| Duty | 0.45 | 0.44 |
| Gate voltage | 16V | 16.2V |
| Load resistance | 50Ω | 49.96Ω |
| $R_{dson}$+ESR | 0.1Ω+0Ω | 0.3Ω+2.6Ω |
| Input voltage | 200V | 200V |
| Switching frequency | 474.8KHz | 474.8KHz |
| Total inductor | 83.766uH | 88.919uH |
| Resonant capacitor | 1.400nF | 1.397nF |

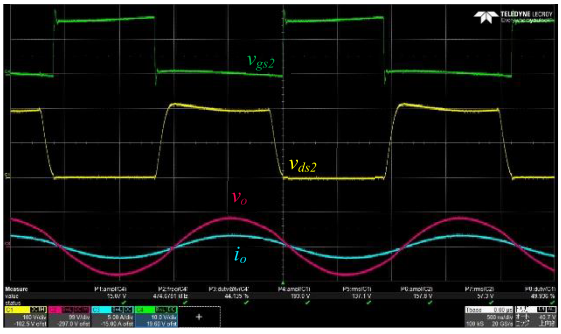


**Fig. 10** Measured waveforms.

the ZVS operation deviated with a little error from simulation.

### 8.3 Frequency Verification

This section is to verify three analytical results inferred from the Sect. 6. First, to verify that at any fixed DC input voltage $V_I$, which results in a fixed $C_{st}$, the maximum operating frequency under the ZVS condition can always be obtained at $\varphi = 0°$, $D = 0.25$. Second, to verify that at $\varphi = 0°$, $D = 0.25$, higher DC input voltage $V_I$, which results in a lower $C_{st}$, can obtain a higher maximum operating frequency f under the ZVS condition. Third, to verify that at $\varphi = 0°$, $D = 0.25$, if the DC input voltage and the corresponding maximum operating frequency are not matched with each other, the operation cannot satisfy the ZVS condition.

Table 4 shows the three conditions of simulation and experiment for verification 1&2. Each DC input voltage is set with its corresponding maximum operating frequency. The duty is set from 0.1 to 0.4. In simulation, the junction temperature of the switch is set to a proper temperature. While in the experiment, the data is measured when the case temperature reaches the same. Concerning the danger of overheating and breakdown of the switch, only 200 V and 300 V input DC voltage are tested in the experiment this time.

The results of verification 1&2 are shown by Fig. 11. As for the simulation result, for each input DC voltage, when operating at its corresponding maximum operating frequency, the highest efficiency is always obtained at $\varphi = 0°$, duty=0.25, which are 78.0% for 200 V at 4.967 MHz, 77.4% for 300 V at 6.094 MHz, 75.8% for 400 V at 7.041 MHz, respectively. As the ZVS is the optimal operation mode for

**Table 4** Conditions for verification 1&2.

| Parameter | Simulated | Measured |
|---|---|---|
| Duty | 0.1~0.4 | 0.1~0.4 |
| Gate voltage | 16V | 16.2V |
| Load resistance | 50Ω | 40.96Ω |
| | Condition A | |
| Input voltage | 200V | 200V |
| Switching frequency | 4.967MHz | 4.967 MHz |
| Total inductor | 8.011uH | 8.010uH |
| Resonant capacitor | 128.164pF | 129.068pF |
| Temperature on test | 50°C(junction) | 50°C(case) |
| | Condition B | |
| Input voltage | 300V | 300V |
| Switching frequency | 6.094MHz | 6.094MHz |
| Total inductor | 6.529uH | 6.508uH |
| Resonant capacitor | 104.694pF | 104.796pF |
| Temperature on test | 75°C(junction) | 75°C(case) |
| | Condition C | |
| Input voltage | 400V | |
| Switching frequency | 7.041MHz | |
| Total inductor | 5.654uH | |
| Resonant capacitor | 90.416pF | |
| Temperature on test | 100°C(junction) | |

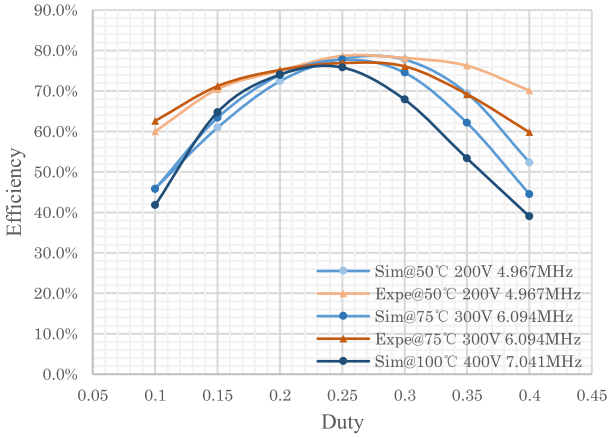


**Fig. 11** Results for verification 1&2.

efficiency, it can be inferred that all the operations at $\varphi = 0°$, $D = 0.25$ are satisfying the ZVS condition. Among these three ZVS operation points, 300 V can achieve 6.094 MHz while 200 V can only achieve 4.967 MHz. And the highest frequency of 7.041 MHz is achieved by the highest DC input voltage of 400 V. If $\varphi = 0°$, $D \neq 0.25$, the analyzed ZVS condition is not satisfied so that the efficiency decreases. Thus, the first and second analytical results are verified. As the simulation is conducted by the switch in SPICE model, the contained on-resistance and input capacitance leads to the inescapable conduction loss and switching loss. Thus, for each operation, even if the ZVS condition is satisfied, the obtained efficiency cannot be very high at such a high frequency of megahertz. Furthermore, as the degree of Miller's effect occurred by the input capacitance varies from different frequencies, there are few differences among the obtained highest efficiencies under the ZVS condition. On the other hand, the experimentally obtained curves by both operation conditions keep the same characteristics as those of simula-

**Table 5** Conditions for verification 3.

| Parameter | Simulated | Measured |
|---|---|---|
| Duty | 0.25 | 0.25 |
| Gate voltage | 16V | 16.2V |
| Load resistance | 50Ω | 40.96Ω |
| | Condition A | |
| Input voltage | 50V~200V | 50V~200V |
| Switching frequency | 4.967MHz | 4.967 MHz |
| Total inductor | 8.011uH | 8.010uH |
| Resonant capacitor | 128.164pF | 129.068pF |
| Temperature on test | 50℃(junction) | 50℃(case) |
| | Condition B | |
| Input voltage | 50~300V | 50~300V |
| Switching frequency | 6.094MHz | 6.094MHz |
| Total inductor | 6.529uH | 6.508uH |
| Resonant capacitor | 104.694pF | 104.796pF |
| Temperature on test | 75℃(junction) | 75℃(case) |
| | Condition C | |
| Input voltage | 50V~400V | |
| Switching frequency | 7.041MHz | |
| Total inductor | 5.654uH | |
| Resonant capacitor | 90.416pF | |
| Temperature on test | 100℃(junction) | |

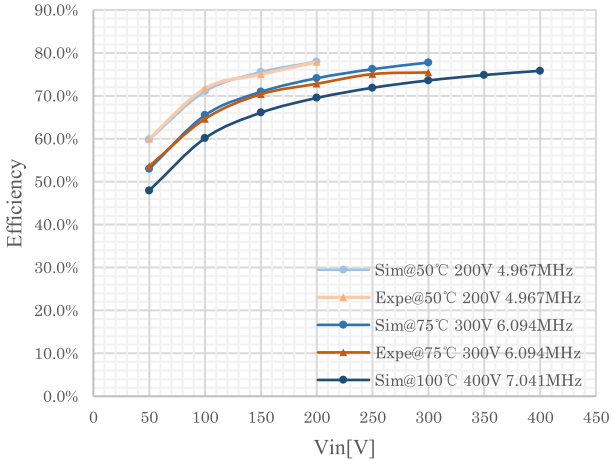


**Fig. 12** Simulation result for verification 3.

tion. The obtained efficiencies under the ZVS condition at $\varphi = 0°$, $D = 0.25$ are consistent with the simulated result.

Table 5 shows the conditions of simulation and experiment for verification 3. The duty is fixed at 0.25 with the precondition of $\varphi = 0°$. According to Table 1, the frequencies are set to the corresponding maximum operating frequencies under the ZVS condition of 400 V, 300 V and 200 V DC input, respectively. For each frequency, the DC input voltages are set from 50 V to 400 V, 300 V and 200 V, respectively. Figure 12 shows the simulation results. For each operation, the highest efficiency can only be obtained when the input DC voltage and its corresponding maximum operating frequency under the ZVS condition are matched with each other, which are 75.8% for 7.041 MHz at 400 V, 77.4% for 6.094 MHz at 300 V, 78.0% for 4.096 MHz at 200 V. For each operating frequency, if the DC input voltage deviated from the matched value, the ZVS condition is not satisfied and the efficiency decreases. For example, when operating at 7.041 MHz, the matched DC input voltage under ZVS condition should 400 V. If the voltage deviates to 300 V, the corresponding maximum operating frequency under the ZVS condition of 300 V becomes 6.094 MHz. As 7.041 MHz > 6.094 MHz, the frequency limitation under the ZVS condition of 300 V is exceeded. Thus, the ZVS condition is not satisfied by 300 V at 7.041 MHz and the efficiency decreases. On the other hand, at the DC input voltage of 200 V, the highest efficiency is only obtained at 4.967 MHz, which is the corresponding maximum operating frequency under the ZVS condition. If the frequency deviated higher, like 6.094 MHz or 7.041 MHz, the frequency limitation under the ZVS condition of 200 V is exceeded, thus the ZVS condition is not satisfied by 200 V at 6.094 MHz or 7.041 MHz and the efficiency decreases. As for experimental result, the data are all obtained by the experiment under the precondition of $\varphi = 0°$, $D = 0.25$. The obtained curves keep good agreement with those of the simulation.

## 9. Conclusion

This paper proposes an analytical model of maximum operating frequency of class-D ZVS inverter. The proposed model includes the linearized parasitic capacitance and the any duty ratio. The model is built based on the expressions derived from the class-D inverter operation principle and the Fourier expansion under the ZVS condition. And the design equations for circuit parameters are also built. The result of frequency analysis shows that the maximum operating frequency under the ZVS condition can be obtained in condition of 0.25 duty and 0° output current phase angle and the highest DC input voltage. The verification is conducted by a self-designed class-D inverter within a 650 V/30 A SiC-MOSFET. The ZVS operation and analyzed frequency characteristics are successfully verified by both simulation and experiment in good agreement.

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