PAPER

A Multi-Channel Biomedical Sensor System with System-Level Chopping and Stochastic A/D Conversion

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SUMMARY This paper presents a multi-channel biomedical sensor system with system-level chopping and stochastic analog-to-digital (A/D) conversion techniques. The system-level chopping technique extends the input-signal bandwidth and reduces the interchannel crosstalk caused by multiplexing. The system-level chopping can replace an analog low-pass filter (LPF) with a digital filter and can reduce its area occupation. The stochastic A/D conversion technique realizes power-efficient resolution enhancement. A novel auto-calibration technique is also proposed for the stochastic A/D conversion technique. The proposed system includes a prototype analog front-end (AFE) IC fabricated using a 130 nm CMOS process. The fabricated AFE IC improved its interchannel crosstalk by 40 dB compared with the conventional analog chopping architecture. The AFE IC achieved SNDR of 62.9 dB at a sampling rate of 31.25 kSps while consuming 9.6 μW from a 1.2 V power supply. The proposed resolution enhancement technique improved the measured SNDR by 4.5 dB.

key words: *biomedical sensor, ECG, chopper stabilization, SAR-ADC, stochastic A/D conversion*

1. Introduction

In recent years, biomedical sensors have been required due to the increasing demand for healthcare applications. These devices operate with batteries such as coin cells. Therefore, a low-voltage and low-power analog front-end (AFE) IC is becoming one of the key components. An AFE IC typically consists of a low-noise amplifier (LNA), analog-to-digital converter (ADC), digital signal processor (DSP), and digital interface (Digital I/F). The area, power, and speed of digital circuits can be improved by the CMOS process scaling. However, the design of analog and mixed-signal circuits such as amplifiers and ADC becomes more difficult in a fine CMOS process because of the increasing mismatch and decreasing supply voltage headroom. Therefore, digitally assisted technologies are becoming more important for improving the performance of sensor devices [1]. The power consumption of analog circuits involves trade-offs between accuracy and operating speed [2]. In particular, LNAs and ADCs dominate in terms of power consumption and accuracy.

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Chopper-stabilized LNAs are used to decrease the influence of 1/f noise and low-frequency offset [3]. However, they require an analog post-low-pass filter (LPF) to eliminate the modulation noise [4]. The post-LPF occupies a large occupation area to attenuate modulation noise. In this paper, a chopping technique using a digital demodulator is proposed as a system-level chopping technique. The proposed technique relaxes the requirements of the post-LPF.

For an ADC, a successive approximation register ADC (SAR-ADC) is selected owing to its high power efficiency [5], [6]. The SAR-ADC consists of a digital-to-analog converter (DAC), comparator, and SAR logic. Usually, the DAC block of the SAR-ADC is implemented using a binary-weighted capacitor DAC (CDAC). The resolution of the SAR-ADC is limited by various factors, such as incomplete settling, capacitor mismatch of the CDAC, and thermal noise. In particular, capacitor mismatch and thermal noise are dominant in low-speed, medium-resolution SAR-ADCs used in biomedical sensors [7], [8]. Many capacitance-mismatch calibration techniques have been proposed. However, most of them require additional analog circuits [9]. Thermal noise can be suppressed by oversampling and filtering (analog scaling), which requires four times as much power to improve the effective number of bits (ENOB) by one bit. However, its efficiency degrades for resolution over 10 bits [7]. This study presents a novel resolution-enhancement technique using noise statistics. The proposed technique converts the CDAC output residue using repetitive comparisons and statistical processing.

This paper is organized as follows. The system architecture of the AFE IC is described in Sect. 2. In Sect. 3, the proposed system-level chopping technique is described. In Sect. 4, a resolution enhancement technique using stochastic A/D conversion is proposed. In Sect. 5, the circuit implementation is detailed for the AFE IC, including the proposed techniques, while in Sect. 6, the measurement results are reported. Finally, the conclusions are provided in Sect. 7.

2. System Architecture

The architecture of the proposed biomedical sensor system, including the AFE IC, is shown in Fig. 1. The AFE IC consists mainly of four-channel LNAs, analog LPFs, a four-channel multiplexer (MUX), ADC, de-multiplexer (DEMUX), digital LPFs, and serial peripheral interface (SPI). The AFE IC also integrates an internal bias, regulators, ADC

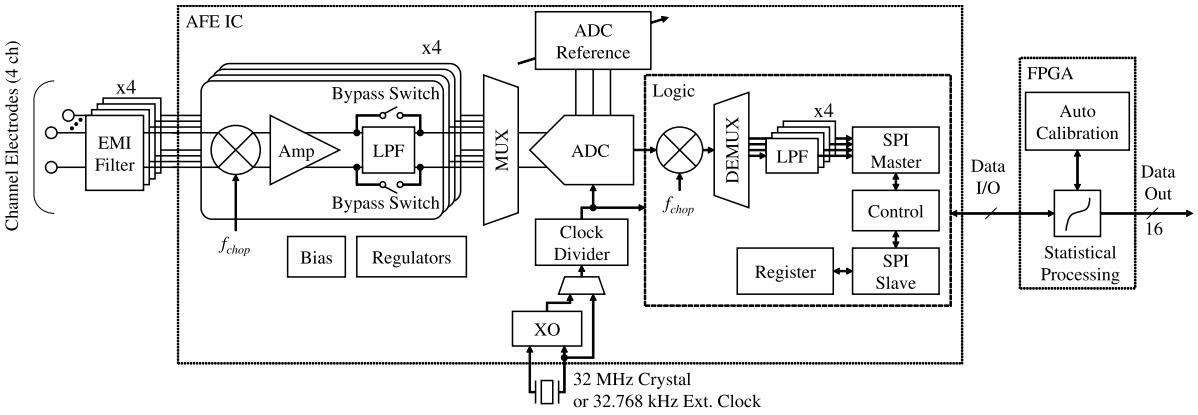

Fig. 1 Block diagram of the proposed biomedical sensor system.

reference drivers, and clock generation circuits (crystal oscillator (XO) and clock divider). The internal regulator generates a supply voltage of 1.0 V for the LNAs, MUX, and buffer.

The proposed AFE IC integrates both conventional analog and system-level chopping configurations, and these configurations can be set with registers via an SPI. The LPF can be bypassed for the system-level chopping configuration.

The AFE IC integrates a stochastic SAR-ADC [7]. The ADC full-scale range can be selected from 0.5 V, 1.0 V, and 1.5 V by configuring the ADC reference output voltage via the SPI. The variable full-scale range realizes optimal gain and noise performance for variable-range applications. The dynamic range can be enhanced by stochastic A/D conversion, even when a lower full-scale range (0.5 V) is selected. The ADC sampling rate can be configured from 256 Sps to 1.024 kSps with an external clock of 32.768 kHz. The sampling rate can be extended to 500 kSps with an internal XO or an external 32 MHz clock. The statistical processing and auto-calibration logic circuits for the stochastic SAR-ADC are implemented using an off-chip field-programmable gate array (FPGA).

The AFE IC realizes multi-channel data acquisition by time-division multiplexing with four-channel amplifiers, a MUX, and ADC. The SPI implements both slave and master modes. The configuration registers are set in the SPI slave mode. The acquired data (ADC output) is transferred in the SPI master mode for high-speed data transmission. The SPI clock can be set up to 32 MHz with the internal XO or external 32 MHz clock.

3. System-Level Chopping for Multi-Channel AFE

The block diagrams of system-level chopping techniques for multi-channel AFE and their principles are shown in Fig. 2. The system-level chopping configuration consists of an analog modulator, ADC, digital demodulator, and digital LPF (decimation filter). A delay-controlling circuit is inserted between the analog modulator and digital demodulator to adjust the chopper clock phase by the latency of the ADC. As shown in Fig. 2(b), the output data is delayed by one period

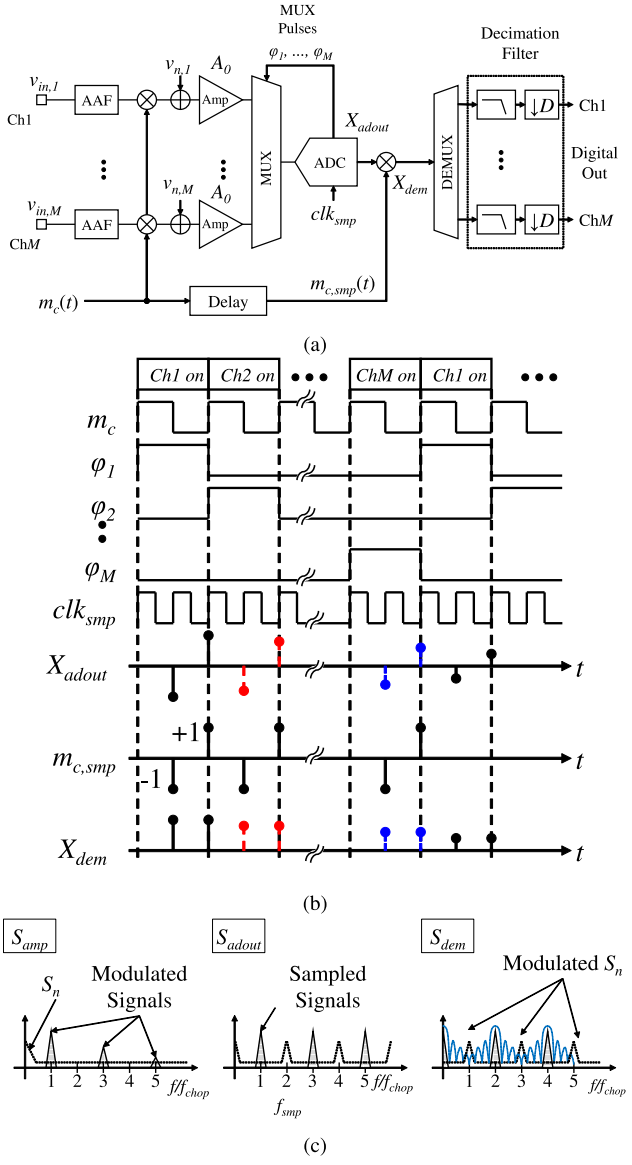

Fig. 2 (a) Block diagram of the multi-channel AFE with system-level chopping technique and (b) timing diagram of control pulses (c) their principles in the frequency domain (a blue line shows the gain of a digital filter).

of clk_{smp}. Therefore, the chopper clock of the demodulator is also delayed by the same amount. The system-level chopping architecture was proposed for a transducer ADC with a delta-sigma modulator to reduce offset drift [10] and adopted in some studies with delta-sigma ADCs [11]–[14]. Delta-sigma ADCs are not suitable for multi-channel AFEs having fast scan rates because an output code does not correspond to a single point of analog input. In this paper, the system-level chopping technique is applied for a time-division multiplexing system with a SAR-ADC.

In the system-level chopping architecture, the ADC directly converts the modulated signal, and the digital demodulator demodulates converted data in the digital domain. The digital LPF attenuates the modulated noise originating from the low-frequency noise (mainly 1/f noise).

As with the conventional analog chopping technique, the 1/f noise added between the modulator and demodulator is suppressed by the analog LPF. On the other hand, the system-level chopping technique does not require an analog LPF with high attenuation at f_{chop}. Therefore, the system-level chopping technique can reduce the area occupation of the analog LPF in exchange for the fast sampling of the ADC. The CMOS process scaling can improve ADC sampling speed [2], while the analog LPF cannot be reduced by process scaling. The cost of implementing analog filters increases with advanced processes due to higher costs per area.

As with the system-level chopping technique, the power spectrum of each amplifier output $S_{amp}(f)$ is given by [15]

$$S_{amp}(f) = \left(\frac{2A_0}{\pi}\right)^2 \sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2} S_{in}\left(f - k f_{chop}\right) + A_0^2 S_n(f), \tag{1}$$

where $S_{in}(f)$ and $S_n(f)$ are the power spectra of v_{in} and v_n, respectively. The power spectrum of the ADC output $X_{adout}(t)$ for a single channel input, $S_{adout}(f)$, is given by

$$S_{adout}(f) = \sum_{n=-\infty}^{\infty} S_{adin}(f - n f_{smp}), \tag{2}$$

where f_{smp} is a sampling frequency. For simplicity, the digital-demodulation signal $m_{c,smp}(t)$ is expressed as a pulse series of which sign changes every $1/2$ period of the chopper clock as follows:

$$m_{c,smp}(t) = \frac{T_c}{2} \sum_{m=-\infty}^{\infty} (-1)^m \delta\left(t - \frac{mT_c}{2}\right) = \sum_{\substack{m=-\infty \\ m\ odd}}^{\infty} e^{j2\pi m f_{chop} t}, \tag{3}$$

where $T_c = 1/f_{chop} = 2/f_{smp}$ and $\delta(t)$ denotes Dirac's delta. The demodulator output is a multiplication of $m_{c,smp}(t)$ and ADC output $X_{adout}(t)$. Therefore, the demodulator output spectrum $S_{dem}(f)$ can be expressed as follows:

$$S_{dem}(f) = \sum_{\substack{m=-\infty \\ m\ odd}}^{\infty} S_{adout}(f - m f_{chop}). \tag{4}$$

Finally, the noise spectrum is shifted by mf_{chop} at the demodulator output and can be given by

$$A_0^2 \sum_{\substack{m=-\infty \\ m\ odd}}^{\infty} \sum_{n=-\infty}^{\infty} S_n(f - m f_{chop} - n f_{smp}), \tag{5}$$

and the signal term is given by

$$\left(\frac{2A_0}{\pi}\right)^2 \sum_{\substack{m=-\infty \\ m\ odd}}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{\substack{k=-\infty \\ k\ odd}}^{\infty} \frac{1}{k^2} S_{in}\left(f_{k,m,n}\right), \tag{6}$$

where $f_{k,m,n} = f - (k+m) f_{chop} - n f_{smp}$. When $f_{chop} = f_{smp}$, the noise spectrum is aliased around DC. Therefore, the sampling frequency must be at least twice the chopper frequency ($f_{smp} \geq 2 f_{chop}$) to avoid aliasing the modulated input signal and noise together. In the proposed system, an anti-aliasing filter (AAF) is implemented as an off-chip filter denoted as the EMI filter in Fig. 1. The wideband (white) noise of the amplifier is aliased by sampling. In the proposed system, sampling is performed at a frequency higher than the signal bandwidth, and a digital filter reduces the effect of thermal noise. In addition, the aliasing of the thermal noise of an amplifier is not critical because the 1/f noise is dominant in biomedical sensor systems.

In the proposed system, the system-level chopping technique is applied to a multi-channel AFE. The DEMUX picks two points from the multiplexed data and distributes them to M channels. The demultiplexed data are filtered with a decimation rate of D. The transfer function in z domain $H(z)$ of the decimation filter can be expressed as follows:

$$H(z) = \frac{1}{2}\left(1 + z^{-1}\right) \cdot \frac{2}{D} \sum_{i=0}^{\frac{D}{2}-1} z^{-2Mi}, \tag{7}$$

where z^{-1} corresponds to a unit delay of $1/f_{smp}$. The output data rate of each channel $f_{DR,ch}$ is $f_{smp}/(M \cdot D)$. The sampling points will be unequally spaced. However, averaging will produce an output that is representative of averaging interval.

The system-level chopping technique can also suppress the interchannel crosstalk of a multi-channel AFE. The interchannel crosstalk is mainly caused by capacitance coupling, reference and power supply coupling, and incomplete settling of a MUX. The capacitance coupling and reference/supply coupling can be suppressed by physical layouts such as wiring shielding and supply decoupling. However, the crosstalk caused by incomplete settling cannot be suppressed by these techniques. The incomplete settling of MUXs can be mitigated by the appropriate design of on-resistance and amplifier drivability [16]. For low-power operation, the LPF should be implemented as a passive-RC filter. However, the drivability seen from the MUX input

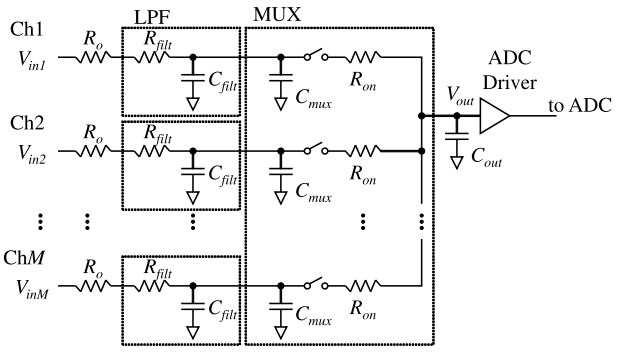

Fig. 3 MUX and driving circuits (LPFs are simplified for conceptual explanation).

is the series resistance of the LNA output and LPF. In this paper, the crosstalk is suppressed by bypassing the analog LPFs in the system-level chopping configuration.

Figure 3 shows the M-channel MUX and driving circuits. In Fig. 3, R_o is the output resistance of the amplifier, R_{filt} is the resistance of the LPF, R_{on} is the on-resistance of the MUX, C_{mux} is the MUX input capacitance, C_{out} is the MUX output capacitance including input capacitance of the ADC driver, and C_{filt} is the capacitance of the LPF. When the ADC input is multiplexed from Ch1 to Ch2, the MUX output voltage V_{out} will change [16]. When $R_{on} \ll R_{filt}$, V_{out} changes instantaneously by charge sharing between C_{filt} and C_{out}. The voltage change at the MUX output $\Delta V_{in2} = V_{out} - V_{in2}$ by this charge sharing is expressed as follows:

$$\Delta V_{in2} = \frac{C_{out}}{C_{filt} + C_{mux} + C_{out}} (V_{in2} - V_{in1}), \tag{8}$$

where V_{in1} and V_{in2} are the equivalent outputs of LNAs in Ch1 and Ch2, respectively. Then the remaining charge is supplied from the amplifier through R_o, R_{filt}, and R_{on}. The settling error voltage $V_{err,2}$ after acquisition time t can be expressed by first-order approximation as follows:

$$V_{err,2}(t) \approx \Delta V_{in2} \exp\left(-\frac{t}{\tau}\right), \tag{9}$$

where τ is the settling time constant and can be expressed as follows:

$$\tau = (R_o + R_{filt} + R_{on})C_{out} + (R_o + R_{filt})(C_{mux} + C_{filt}). \tag{10}$$

The settling error voltage $V_{err,2}$ depends on τ and previous channel voltage V_{in1}. When the number of channels increases and faster multiplexing is required, buffers should be inserted between the passive LPF of each channel and the MUX. This leads to increased power consumption, area, and nonlinearity. As for system-level chopping architecture, R_{filt} is bypassed and C_{filt} is disconnected. Therefore τ can be expressed as follows:

$$\tau = (R_o + R_{on})C_{out} + R_o C_{mux}. \tag{11}$$

When $R_o = 100\,\Omega$, $R_{filt} = 1.25\,\mathrm{M}\Omega$, $R_{on} = 1\,\mathrm{k}\Omega$, $C_{filt} = 120\,\mathrm{pF}$, $C_{mux} = 100\,\mathrm{fF}$ and $C_{out} = 1\,\mathrm{pF}$, τ becomes 151 μs. On the other hand, when the LPF is bypassed, τ becomes 1.11 ns. The bypass of the LPF in the system-level chopping technique can reduce crosstalk caused by incomplete settling of multiplexing.

4. Stochastic SAR-ADC

The SAR-ADC architecture is suitable for low-power applications [17]. A typical SAR-ADC requires a binary-weighted capacitor array as an internal CDAC. It occupies a large occupation area as the resolution increases. The split capacitor architecture used to reduce the area occupation [18], [19], introduces some nonlinearity errors due to parasitic capacitance. The thermal noises also degrade A/D conversion accuracy. For a SAR-ADC with a resolution of around 12 bits, the comparator noise is dominant [7]. The noise can be reduced by oversampling. However, it requires four times oversampling to improve an ENOB by one bit.

Recently, stochastic A/D conversion techniques utilizing the statistics of device mismatch are proposed [20], [21]. These studies utilize offsets of many comparators as a flash ADC. As for SAR-ADCs with high resolution, a successive-stochastic-approximation ADC (SSA-ADC) is proposed [22], [23]. This architecture utilizes the stochastic flash ADC (SF-ADC) to enhance resolution by using ensemble statistics of the offsets of 511 comparators.

On the other hand, stochastic SAR-ADCs which utilize comparator noise statistics are proposed [7], [24], [25]. These stochastic SAR-ADCs enhance their resolution by repetitive comparison and residue estimation. One comparator and 17 times comparisons realize 17 comparator decisions in [7]. Sixteen parallel comparators and four times comparisons realize 64 comparator decisions in [24]. This configuration requires comparator offset calibration so that the offset does not affect the noise statistics.

There is a trade-off between comparator counts and repetitive comparison counts for the SSA-ADC or stochastic SAR-ADC. For high-speed applications, it is preferable to adopt the SSA-ADC [23] or stochastic SAR-ADC with multiple comparators [24]. For low-power applications, stochastic SAR-ADC with a single comparator is suitable. In this paper, the stochastic SAR-ADC with only one comparator is used for design simplicity and performance optimization focusing on electrocardiogram (ECG) monitoring applications. Furthermore, the number of repetitions is variable between 7 and 255 for configurable resolution and power dissipation.

The block diagram of the stochastic SAR-ADC is shown in Fig. 4. The stochastic SAR-ADC consists of a conventional CDAC, comparator, SAR logic, and timing generator. The timing generator adopts a self-timing technique used in [17]. The self-timing technique is suitable for a wide range of sampling rates. As the stochastic SAR-ADC quantizes CDAC residue by repetitive comparison, the self-timing technique also has an advantage in this respect.

The stochastic ADC used in this paper consists of one

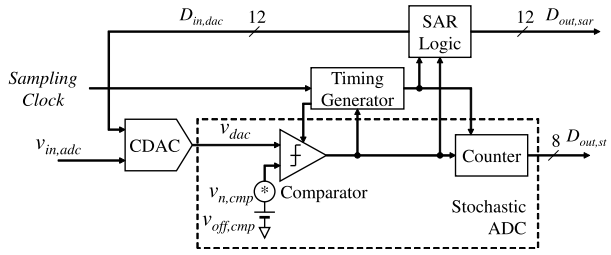

Fig. 4 Block diagram of the stochastic SAR-ADC.

comparator and counter (accumulator) as shown in Fig. 4. The comparator repeats the comparison with noise and offsets during the conversion period and the counter accumulates comparator "1" output. The output $D_{out,st}$ is the counter output and corresponds to the total number of "1" during the conversion cycle.

The stochastic ADC utilizes stochastic resonance [26] with comparator noise. The resolution of the stochastic ADC is determined by the repetitive comparison counts n_{rep}. The comparator noise level (standard deviation) σ_n no longer limits the resolution. The comparator noise level determines the input range.

The stochastic ADC carries out A/D conversion as the following principle. It is assumed that the comparator noise $v_{n,cmp}$ is white noise and follows Gaussian distribution [21]. When comparator input is $v_{in,cmp}$, the probability $P(v_{in,cmp})$ that the comparator outputs "1" can be written as follows:

$$P(v_{in,cmp}) = \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\frac{v_{in,cmp}}{\sqrt{2}\,\sigma_n}\right) \approx \frac{D_{out,st}}{n_{rep}}, \tag{12}$$

where $\mathrm{erf}(x)$ is the error function, and the average of $v_{n,cmp}$ is assumed to be zero.

The SAR-ADC error can be defined as a difference between SAR-ADC output and SAR-ADC input V_{in}. The SAR-ADC error consists of a sampling error ΔV_{smp} and conversion residue ΔV_{dac}, and can be written as follows:

$$D_{out,sar}V_{lsb,sar} - V_{in} = \Delta V_{smp} + \Delta V_{dac}, \tag{13}$$

where $D_{out,sar}$ is the SAR-ADC output code and $V_{lsb,sar}$ is the LSB of the SAR-ADC. For SAR-ADCs, the sampling errors are caused by incomplete settling and kT/C noise. The incomplete settling can be suppressed by the appropriate design of sampling switches and capacitors. The kT/C noise is also suppressed by selecting an appropriate input capacitance against the target resolution.

When ΔV_{dac} can be obtained, the ADC conversion error can be suppressed by subtracting ΔV_{dac} from $D_{out}V_{lsb,sar}$. The stochastic SAR-ADC estimates ΔV_{dac} by repetitive comparison of the CDAC residue after SAR-ADC operation. By substituting ΔV_{dac} in Eq. (12), ΔV_{dac} can be estimated as follows:

$$\Delta V_{dac} \approx \sqrt{2}\sigma_n \mathrm{erf}^{-1}\left(2\left(\frac{D_{out,st}}{n_{rep}} - \frac{1}{2}\right)\right). \tag{14}$$

where $\mathrm{erf}^{-1}(x)$ is the inverse error function. The residue ΔV_{dac} can be estimated by stochastic ADC output $D_{out,st}$, total comparison counts n_{rep}, and the standard deviation of comparator noise σ_n. In previous studies, σ_n is estimated by transient noise simulations [7] or offline calibration [24]. However, σ_n changes by PVT variations. For robustness, it is preferable to determine σ_n automatically after fabrication. The estimation of σ_n is discussed as code combination and scaling for SAR and stochastic ADC output codes [23]. In the previous study [23], the code scaling is determined by off-chip foreground calibration with machine learning.

In this paper, the inverse error function is implemented as a look-up table (LUT) and the code scaling is determined by foreground calibration. The LUT output w_k for $D_{out,st} = k (k = 0, 1, \ldots, n_{rep})$ is determined in the following procedure. First, the ADC input is set to 0 and raw SAR-ADC outputs $D_{out,sar}$ and stochastic ADC outputs $D_{out,st}$ are obtained. Then, the average of the corresponding $D_{out,sar}$ code for the specified $D_{out,st}$ is calculated. The average code is loaded to the LUT as w_k, and can be expressed as follows:

$$w_k = \frac{1}{N_{ave}} \sum_{i=0}^{N_{ave}-1} D^{(k)}_{out,sar,i}, \tag{15}$$

where $D^{(k)}_{out,sar,i}$ is i-th SAR-ADC output of which corresponding $D_{out,st} = k$, N_{ave} is averaging counts for the calibration. The same operations are carried out for $k = 0, 1, \ldots, n_{rep}$ (all $D_{out,st}$ code patterns).

After calibration, $D_{out,st}$ is input to the LUT as an address. The LUT output $w_{D_{out,st}}$ is subtracted from $D_{out,sar}$. The stochastic SAR-ADC output $D_{out,stsar}$ is given by

$$D_{out,stsar} = D_{out,sar} - w_k \quad (k = D_{out,st}). \tag{16}$$

Figure 5(a) shows the hardware implementation of the proposed calibration and statistical processing. The auto-calibration logic block consists of an averaging logic circuit, averaging and sweep counters. When $D_{out,st}$ matches to the sweep counter output k, an enable flag (EN) is asserted and input to the averaging logic and counter. The averaging counter counts up averaging count for the specified $D_{out,st}$. A write-enable flag (WE) for the LUT is asserted when averaging counter output reaches $N_{ave} - 1$. The LUT uses $D_{out,st}$ as a write-address, and averaged $D_{out,sar}$ is written as w_k. The write-enable flag is also used as a sweep counter enable input. The sweep counter counts up k from 0 to n_{rep}.

In the proposed system, w_k is the 16-bit fixed point number as shown in Fig. 5(b). The integer word length $N_{lut,int} = 10$ and the fractional word length $N_{lut,frac} = 6$. The determination of $N_{lut,int}$ is carried out not to be overflowed by the offset of $D_{out,sar}$. The fractional word length $N_{lut,frac}$ is determined by N_{ave}. The output code $D_{out,stsar}$ consists of 16-bit data by truncating LSB 2-bits which do not contribute much to the overall performance.

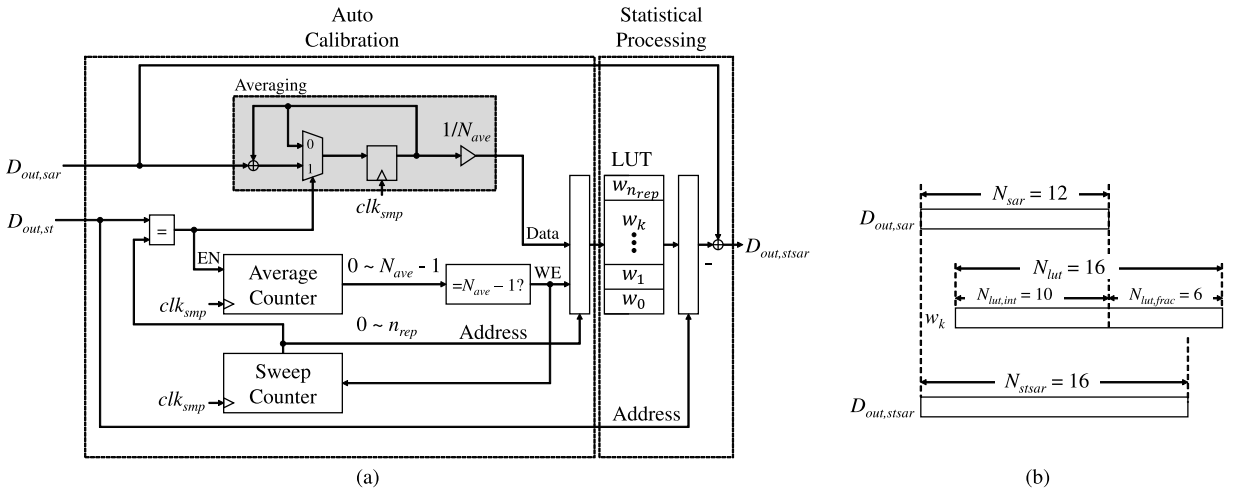

Fig. 5 (a) The stochastic SAR-ADC auto-calibration logic block and (b) bit configuration of the stochastic SAR-ADC.

5. Circuit Implementation

5.1 Low-Noise Amplifier

The schematic of the LNA is shown in Fig. 6. The LNA consists of a fully differential op-amp with chopper stabilization. The analog demodulator can be disabled, which is implemented for performance comparison of analog and system-level chopping configurations. The 33 dB gain is realized by the ratio of AC-coupled capacitors C_{IN} and feedback capacitors C_F. As DC-feedback resistors, pseudo-resistors by diode-connected p-ch FETs are used. The midpoint is connected to the output common-mode voltage V_{CM} of the amplifier via a diode-connected p-ch FET. The pseudo resistors R_1, R_2, and R_3 form a T-feedback network. Using the star-delta transformation, the equivalent feedback resistor $R_{F,EFF}$ can be expressed as follows:

$$R_{F,EFF} = R_1 + R_2 + \frac{R_1 R_2}{R_3}. \tag{17}$$

A high value of $R_{F,EFF}$ can be realized with smaller values of R_1, R_2, and R_3. Therefore, the DC offset due to the leakage currents of parasitic diodes can be suppressed compared with conventional pseudo resistors [27].

The supply voltage of the LNA is 1.0 V which is generated from a 1.2 V supply by an internal voltage regulator to stabilize the supply for analog circuits. The common mode voltage V_{CM} is 0.5 V and is also generated by an internal regulator. The voltage swing of the chopper clock is 0.5 V to reduce clock feed-through [23]. The chopper clock frequency f_{chop} can be selected from 4.096 kHz to 32.768 kHz with an external 32.768 kHz clock (3.90625 kHz to 31.25 kHz with an internal 32 MHz clock). Note that the sampling frequency of the ADC is controlled so that $f_{smp} = 2f_{chop}$. The analog LPF in the latter stage consists of a 6th-order passive RC filter to sufficiently attenuate modulated 1/f noise in the analog chopping configuration.

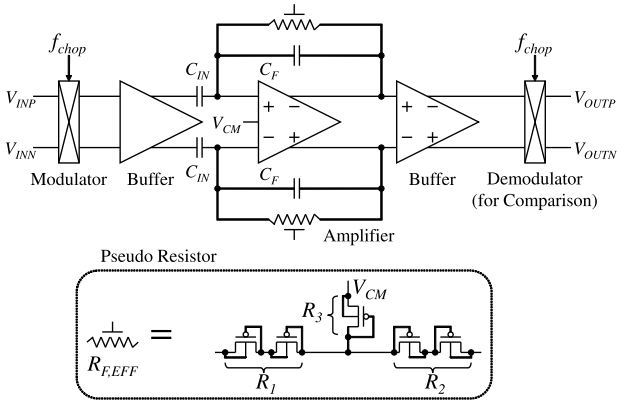

Fig. 6 The schematic of the LNA.

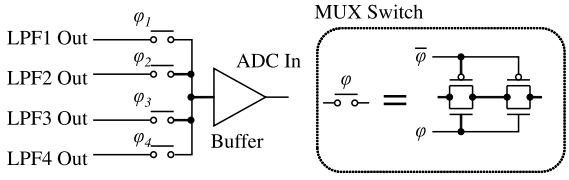

Fig. 7 Four-channel input MUX.

5.2 Multiplexer

Figure 7 shows the MUX between LNA channels and ADC. The MUX consists of four switches and an output buffer. Each switch consists of CMOS switches which are connected in series to reduce capacitance coupling between each channel. The multiplexed signal is buffered to drive the ADC input capacitance and improve settling speed. The MUX is switched by four-phase non-overlapping pulses to avoid interchannel crosstalk due to simultaneous switching.

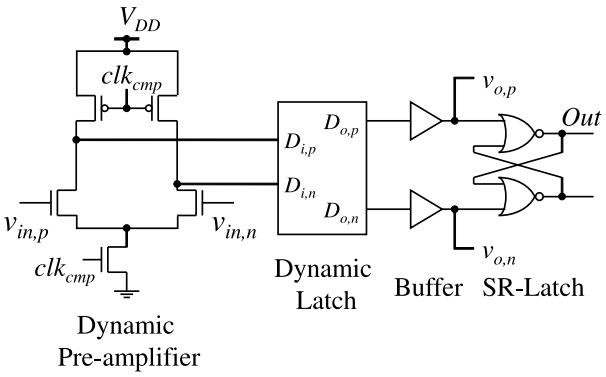

Fig. 8 Schematic of the dynamic latched comparator.

5.3 Comparator

In this design, a dynamic latched comparator as shown in Fig. 8 is used. The dynamic latched comparator is suitable for low-power operation because there is no static current dissipation except for leakage current. The comparator consists of a dynamic pre-amplifier, dynamic latch, buffer, and SR-latch [23]. The buffer is inserted before the SR-latch to avoid hysteresis caused by input capacitance variation depending on SR-latch states. The SR-latch is used to hold comparator output during the reset phase (clk_{cmp} = "0"). Since only one comparator is used in this study, kickback noise is less dominant than in our previous work [23] which uses 511 comparators. Therefore, a static pre-amplifier is not used.

The simulated comparator noise σ_n is 0.29 $\mathrm{mV_{rms}}$ and current dissipation is 10 μA at 100 MHz clock when comparator output toggles every clock cycle.

5.4 Stochastic SAR-ADC Control Logic

The block diagrams of the stochastic SAR-ADC control logic and its timing diagram are shown in Fig. 9. It uses an asynchronous self-timing scheme [17] to realize configurable repeat counts for the stochastic ADC operation without a high-frequency reference clock. The ADC is in the sampling phase while the sampling clock clk_{smp} is high. In the sampling phase, clk_{cmp} = 0, and the dynamic latch outputs of the comparator $v_{o,p}, v_{o,n}$ = 0. When clk_{smp} falls, the ADC enters the conversion phase. The delay of t_{d1} is inserted to relax the settling time for MSB comparison. In the loop of clk_{cmp} including the delay of t_{d2}, the oscillation is performed until the end flag goes high. In the conversion phase, the internally generated clocks are used as the timing control clock for the CDAC clk_{self} and comparator clock clk_{cmp}. The first 12 cycles of clk_{self} are used for the SAR-ADC normal operation, and 0 to 255 cycles are used for the stochastic ADC operation. The estimation and calibration logic is implemented as shown in Fig. 5 by using an off-chip FPGA with n_{rep} = 31, and N_{ave} = 64.

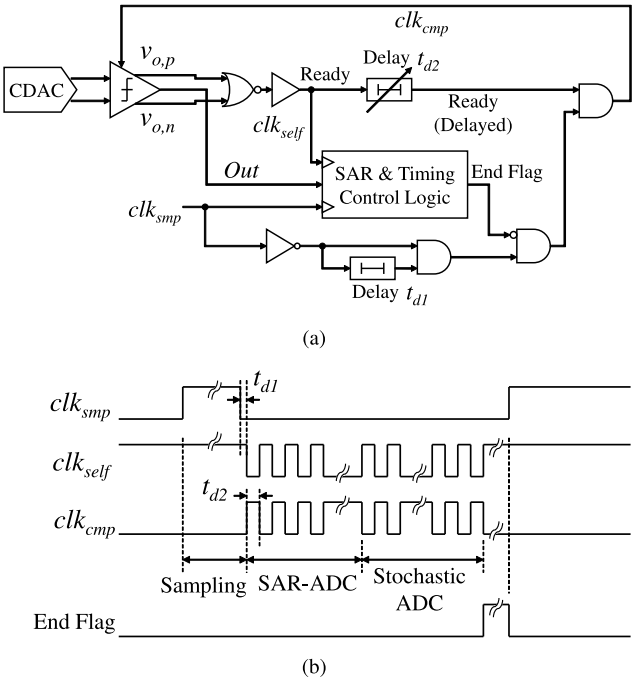

Fig. 9 Asynchronous control logic for the proposed stochastic SAR-ADC: (a) schematic, (b) timing diagram.

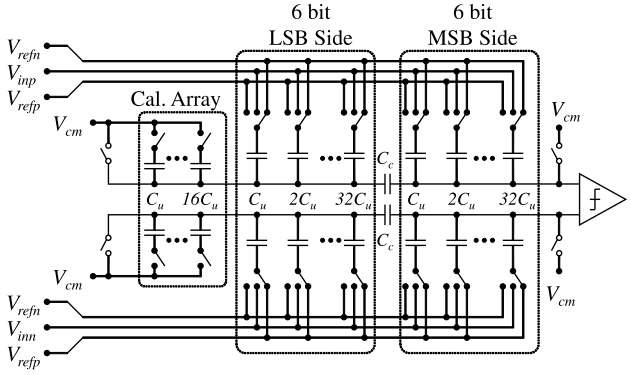

Fig. 10 Charge redistribution CDAC.

5.5 Capacitor DAC

In this design, a CDAC shown in Fig. 10 is used as the DAC of the SAR-ADC. The CDAC consists of a binary-weighted capacitor array and switches. The capacitor array is split into the MSB and LSB arrays to reduce area occupation [19]. The LSB array is scaled by the split capacitor C_c. This SAR-ADC architecture is appropriate for 10-bit and more resolution because of area efficiency and linearity. The unit capacitance C_u is determined so that the kT/C noise does not become the dominant noise. The unit capacitor C_u is 70 fF and the total sampling capacitance is 4.48 pF (64 C_u). The kT/C noise is 30.4 $\mu\mathrm{V_{rms}}$. The split capacitor C_c is equal to 1.25 C_u for compensation of the non-linearity error caused by the parasitic capacitance on the top plate of the LSB side array. The calibration capacitor array is added to

adjust the weight of the LSB side array. This is adjusted manually via the SPI, and the default setting is determined by post-layout simulations.

6. Experimental Results

The designed multi-channel AFE IC was fabricated in a 130 nm CMOS process. The total die area is 2.0 mm × 2.0 mm and the die micrograph is shown in Fig. 11. The chips were packaged into 32-pin BGA packages and measured on the evaluation board shown in Fig. 12. The total power consumption from a 1.2 V external supply is approximately 757 μW when all channels are activated at f_{chop} = 16.384 kHz and the output data rate is 256 Sps/channel with an external 32.768 kHz clock. Figure 13 shows four-channel ECG signals with 60 beats per minute (BPM) which are captured by the prototype AFE IC.

The interchannel crosstalk measurement result is shown in Fig. 14. The crosstalk is measured as the ratio of output amplitude of channel-2 and channel-1 when 9.0 mV_{pp}, 50.5 Hz sinusoidal input is applied to channel-1. The ADC input is multiplexed every two clock cycles (f_{chop} = $f_{smp}/2$). The system-level chopping technique can suppress crosstalk by approximately 40 dB with a sampling rate of 32.768 kSps compared with the analog chopping technique.

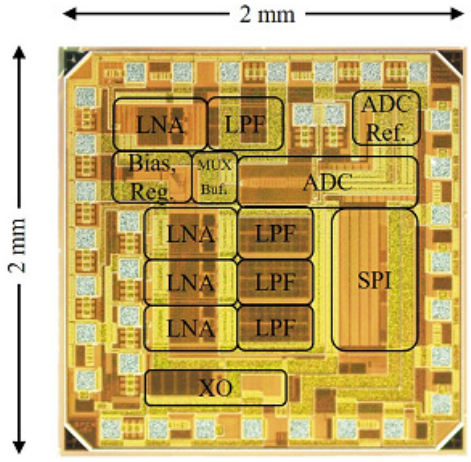

Fig. 11 Chip micrograph of the multi-channel AFE IC.

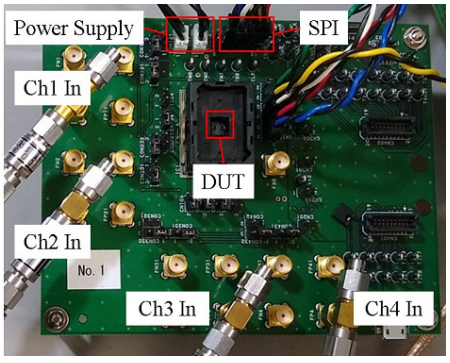

Fig. 12 Photo of the evaluation board.

The proposed system-level chopping technique can achieve crosstalk of less than −80 dB.

Figure 15 shows the gain-frequency characteristics of the AFE channel-1 with the analog chopping and system-

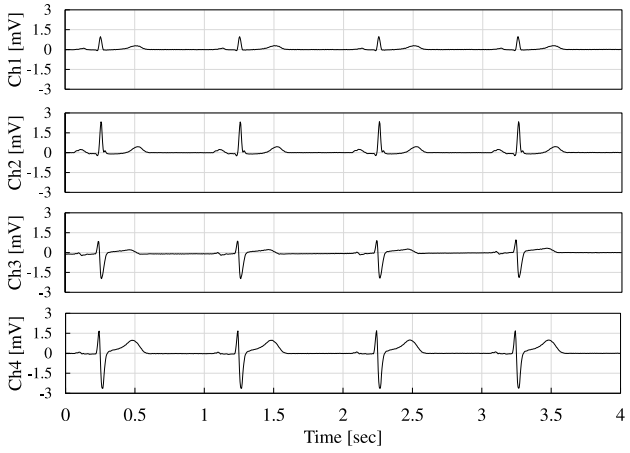

Fig. 13 Four-channel ECG signals with 60 BPM which are captured by the proposed AFE IC (256 Sps/channel with 32.768 kHz external clock).

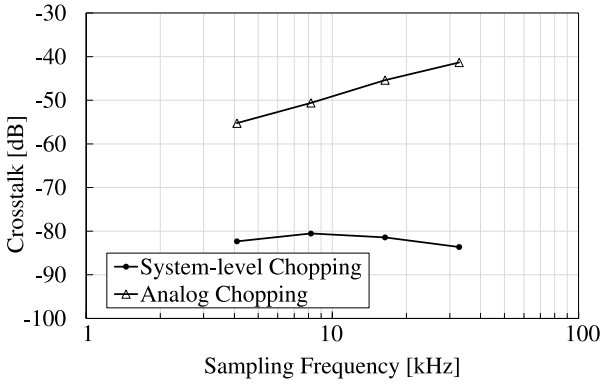

Fig. 14 AFE interchannel crosstalk vs sampling frequency with system-level and analog chopping configurations (f_{chop} = $f_{smp}/2$).

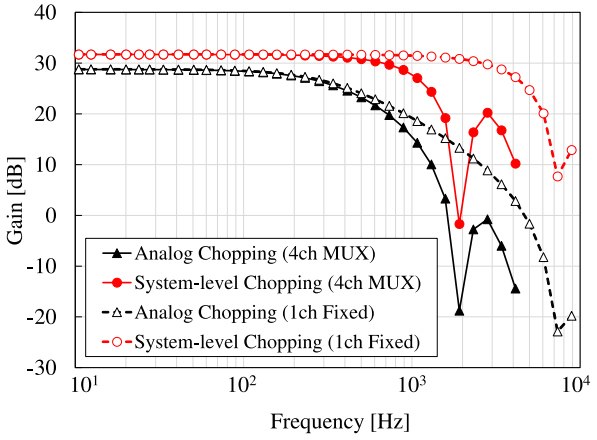

Fig. 15 Gain frequency characteristics of the analog and system-level chopping configurations (f_{chop} = 31.25 kHz from 32 MHz oscillator clock).

Table 1 Comparison with state-of-the-art multi-channel AFEs.

Parameter	[28]	[29]	[30]	[31]	[32]	This Work
Technology [nm]	180	180	180	65	-	130
No. of Channels	16	16	15	4	5	4
Supply [V]	1.8	1	1.2	1.2	3.3	1.2
Power [μW]	25.92	24	29.55	3.456	27000	540
Gain [dB]	40	54/60	40 - 56	40.5 - 56	12.5	31.7
IR Noise [μV]	0.9	0.63	3.43	2.68	1.13	1.89
Crosstalk [dB]	-56	-74.5	-51.5	-63.3	-80	-81

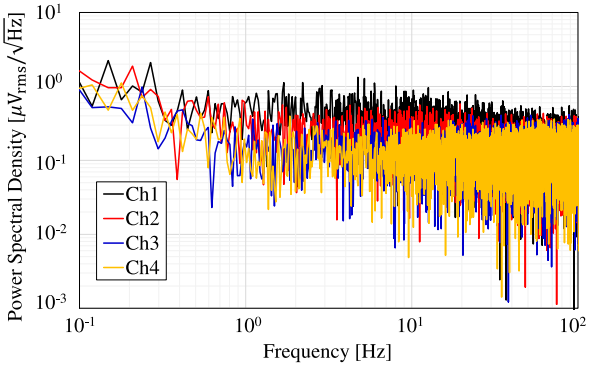

Fig. 16 Measured PSD of IR noise with system-level chopping configuration (f_{chop} = 31.25 kHz from 32 MHz oscillator clock, 2^{16} points FFT).

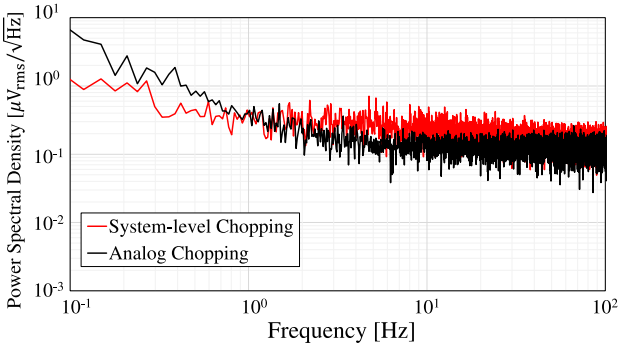

Fig. 17 Measured PSD of IR noise with analog and system-level chopping configurations (average of four channels, f_{chop} = 31.25 kHz from 32 MHz oscillator clock, 2^{16} points FFT).

level chopping configurations. The solid and dashed lines show the frequency characteristics for 4ch MUX operations and 1ch fixed operations, respectively. Note that the notches are attributed to the digital decimation filter. The typical AFE gain is 31.7 dB for system-level chopping configuration. The power consumption of the AFE is 540 μW for all channels except for the XO and regulators. The analog chopping configuration has a cutoff frequency of 370 Hz, while the system-level chopping configuration has a cutoff frequency of 870 Hz for the 4ch MUX operation and 3.38 kHz for the 1ch fixed operation. The system-level chopping allows the bandwidth to be expanded according to applications since the analog filter requirements are independent of the chopping operation. For system-level chopping configuration, the bandwidth is determined by the decimation rate and the number of channels.

Figure 16 shows the power spectral density (PSD) of input-referred (IR) noise for four channels with system-level chopping configuration. The noises were measured simultaneously with a 4ch MUX operation. The 1/f noise is suppressed and the average IR noise of four channels is 1.89 μV_{rms} with a signal bandwidth of 0.5–100 Hz. Figure 17 shows IR noise PSDs with analog and system-level chopping configurations. The noises were measured simultaneously with a 4ch MUX operation and averaged for four channels in each configuration. The PSD of white noise over 1.0 Hz is slightly increased compared with the analog chopping configuration. This is due to the aliasing of white noise in the LNA. On the other hand, 1/f noise is suppressed more compared with analog chopping because of the steep attenuation of a digital decimation filter.

Table 1 summarizes the performance of the proposed

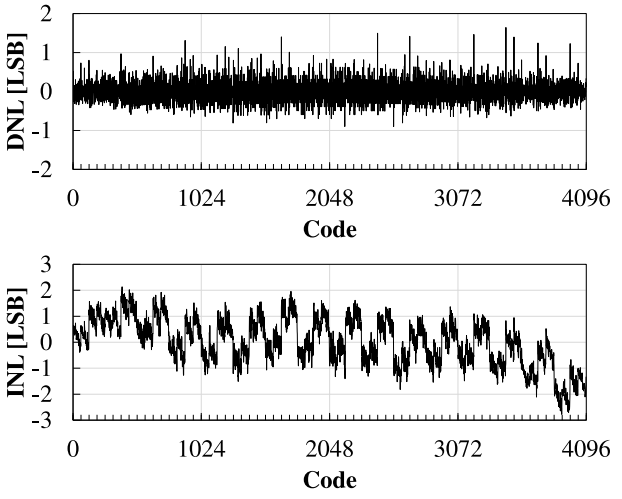

Fig. 18 Measured DNL and INL.

biomedical sensor AFE compared to previous works of multi-channel ECG and electroencephalogram (EEG) circuits. The proposed AFE can achieve better crosstalk performance with the system-level chopping technique and consumes less power than a product-level chip.

To verify the proposed stochastic SAR-ADC technique, the same chips were packaged into 24-pin QFN packages to input ADC test signals directly. Figure 18 shows the measured differential non-linearity (DNL) and integral non-linearity (INL). The minimum and maximum DNL and INL are −0.90/1.64 LSB and −2.77/2.14 LSB, respectively.

Figure 19 shows the noise distribution of the ADC with or without stochastic ADC at V_{in} = 0. The markers denote

Table 2 ADC performance comparison with state-of-the-art stochastic SAR-ADCs.

Parameter	[24]	[23]	[7]	[33]	[34]	This Work
Technology [nm]	40	130	65	65	180	130
Supply Voltage [V]	1.1	1.2	0.7	1.0	1.8	1.2
Full Scale Range [Vppd]	1.6	0.53	-	2.0	-	1.0
Resolution [bit]	12	18	11	10	10	12
Area [mm^2]	0.056	-	0.03	0.12	0.1	0.2068
Sampling Rate [MSps]	35	0.25	0.1	1.28	0.32	0.03125
No. of Comparators	16	511	1	1	1	1
No. of LSB Comparisons	4	16	16	18	16	31
Power [μW]	420	5230	0.6	9	47.9	9.6
Noise [LSB]	-	26.7	0.33	0.21	-	0.58
SNDR [dB]	>60	88.2	64.5	63.5	60.2	62.9
FoM_W [fJ/conv. step]	<15	967.7	4.5	5.6	180	268

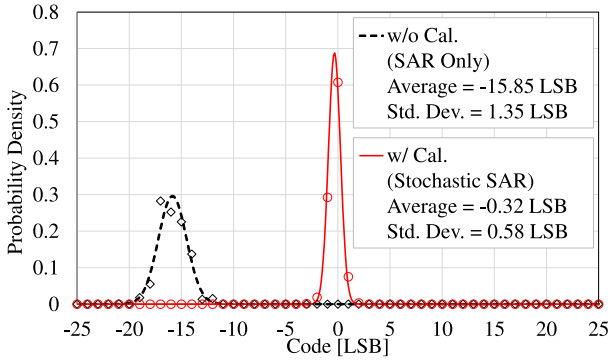

Fig. 19 Measured ADC code distribution with or without stochastic ADC (31.25 kSps with 32 MHz external clock, full-scale is 1.0 V, 2^{15} points).

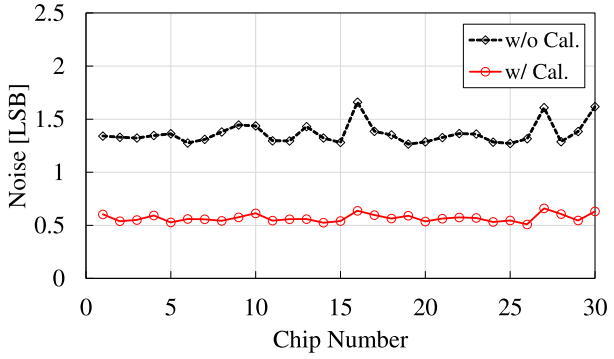

Fig. 20 Measured ADC noise with or without stochastic ADC for 30 chips (31.25 kSps with 32 MHz external clock, full-scale is 1.0 V).

measured code histogram and lines are fitted normal distributions. Without the stochastic ADC, the average and standard deviation of the output code are −15.85 and 1.35 LSB. With the stochastic ADC, they are suppressed to −0.32 and 0.58 LSB, respectively. Note that the histogram count is calculated for 12-bit LSB (truncated LSB four-bits for the result with stochastic ADC). The offset is canceled and noise is reduced by 7.3 dB with the proposed stochastic ADC and its calibration circuit. Figure 20 shows the noise of the ADC with or without stochastic ADC with 30 chips. The noises are reduced by more than 6 dB on all chips. The average noise is 1.36 LSB without stochastic ADC, and 0.57 LSB with stochastic ADC.

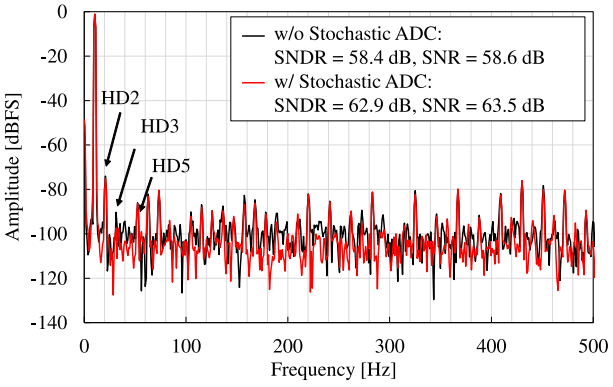

Fig. 21 Measured ADC spectrum without/with stochastic ADC (31.25 kSps with 32 MHz oscillator clock, f_{in} = 10.49 Hz, full-scale is 1.0 V, 2^{15} points FFT).

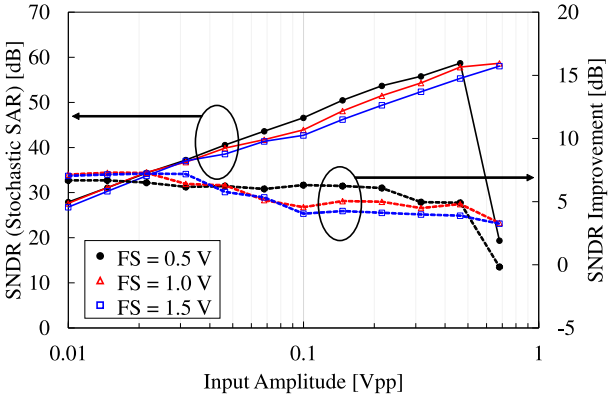

Fig. 22 I/O characteristics of the stochastic SAR-ADC for each full-scale configuration.

The measured spectrum of the ADC is shown in Fig. 21. The input frequency f_{in} is 10.49 Hz and the input amplitude is −1 dBFS. The sampling rate is 31.25 kSps. The SNDRs without and with the stochastic ADC are 58.4 dB and 62.9 dB, respectively. The SNDR was improved by 4.5 dB compared with that of the SAR-ADC raw output.

Figure 22 shows the ADC I/O characteristics for different full-scale (0.5 V, 1.0 V, and 1.5 V) settings, and they were changed by reference driver setting. The input frequency f_{in} is 10.49 Hz and sampling rate is 31.25 kSps. The SNDRs

are improved by the stochastic ADC even when full-scale ranges are changed because the LUTs are optimized by the proposed calibration circuit.

Table 2 summarizes the performance of the proposed stochastic SAR-ADC compared to previous works. Note that $\mathrm{FoM_w}$ is the Walden figure-of-merit defined as follows:

$$\mathrm{FoM_w} = \frac{(\mathrm{Power})}{2^{\mathrm{ENOB}} \times (\mathrm{Sampling\ Frequency})}. \quad (18)$$

The noise performance is better than previous studies considering the full-scale range and resolution.

7. Conclusion

This paper presented a multi-channel AFE IC integrating the system-level chopping technique and stochastic SAR-ADC. The system-level chopping technique can reduce interchannel crosstalk by removing the analog demodulator and LPF in the LNA. This technique can also reduce the area occupation and chip cost. The resolution enhancement technique by a stochastic ADC was also proposed. The stochastic ADC estimates SAR-ADC conversion errors by repetitive comparisons with a noisy, low-power comparator. The AFE IC was fabricated in a 130 nm CMOS process. The interchannel crosstalk was improved by approximately 40 dB by using the system-level chopping technique. The system-level chopping technique also enables expanding the bandwidth of the AFE up to around 3.38 kHz. This leads to the AFE IC being available for multi-application such as ECG, EEG, and electromyogram (EMG). The ADC achieved 62.9 dB SNDR at a sampling frequency of 31.25 kSps with 10.49 Hz, −1.0 dBFS sinusoidal input. The SNDR was improved by 4.5 dB compared with the raw SAR-ADC output. The proposed AFE IC can be used for multiple biomedical applications due to its wide range of bandwidth and resolution configurability.

Acknowledgments

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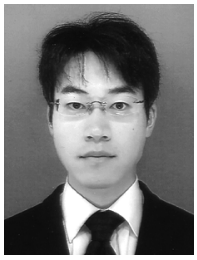

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