PAPER

A Combination Method for Impedance Extraction of SMD Electronic Components Based on Full-Wave Simulation and De-Embedding Technique

Yang XIAO[†], **Zhongyuan ZHOU**[†a)], **Mingjie SHENG**[†], ***and*** **Qi ZHOU**[†], ***Nonmembers***

SUMMARY The method of extracting impedance parameters of surface mounted (SMD) electronic components by test is suitable for components with unknown model or material information, but requires consideration of errors caused by non-coaxial and measurement fixtures. In this paper, a fixture for impedance measurement is designed according to the characteristics of passive devices, and the fixture de-embedding method is used to eliminate errors and improve the test accuracy. The method of obtaining *S* parameters of fixture based on full wave simulation proposed in this paper can provide a thought for obtaining *S* parameters in de-embedding. Taking a certain patch capacitor as an example, the *S* parameters for de-embedding were obtained using methods based on full wave simulation, 2×Thru, and ADS simulation, and de-embedding tests were conducted. The results indicate that obtaining the *S* parameter of the testing fixture based on full wave simulation and conducting de-embedding testing compared to ADS simulation can accurately extract the impedance parameters of SMD electronic components, which provides a reference for the study of electromagnetic interference (EMI) coupling mechanism.

key words: *full-wave simulation, de-embedding, SMD, electronic components, impedance, measuring method*

1. Introduction

The printed circuit board (PCB) is composed of micro-strip lines, discrete components, integrated circuit (IC) chips, etc. Among them, resistors, capacitors, inductors and wires are passive elements [1], [2]. For electromagnetic sensitivity prediction, the lumped parameter model of passive components is not enough to describe the high-frequency characteristics of them [3]. From the perspective of interference, the normal operation of digital control circuit may be affected by electromagnetic interference in the environment. The EMI intentionally or unintentionally harass the IC chip and are coupled by conductor (conducted EMI) or space (radiated EMI) [3]–[5]. The coupling mechanism of EMI to PCB is that when the circuit operates at a high frequency, there are parasitic parameters in the wires of PCB and component leads. These parasitic parameters provide a path for EMI and it would greatly affect the electromagnetic immunity of the equipment. Therefore, the research on the EMI coupling mechanism needs to model the EMI path, Firstly, it is necessary to accurately extract the impedance parameters of the device and establish its high-frequency model [6].

In order to reduce the parasitic parameters of the lead wires, the components of the circuit in current technology are generally SMD components, and the smaller the package size, the smaller the parasitic parameters. The methods of extracting the impedance parameters of SMD electronic components can be divided into analytical method, numerical calculation method and measurement method.

With the trend of miniaturization of SMD electronic components, it is necessary to develop more complex techniques to test them in the field of measurement technology [7]–[10]. In order to accurately obtain the impedance parameters of SMD electronic components, they can also be obtained directly by measuring [11], [12]. However, due to the small size, leadless and non-coaxial structure of SMD components, the ports of vector network analyzer (VNA), test cable and calibration parts generally adopt coaxial structure, which cannot directly measure the components. It is necessary to design a test fixture for SMD electronic components to convert the non-coaxial transmission structure of the components into coaxial transmission structure, but the fixture will bring measurement errors [13]–[15].

De-embedding method is an important fixture removal method [16]. Short-open-load-through (SOLT) calibration method and transmission reflection line (TRL) calibration method are both traditional de-embedding methods. However, SOLT calibration requires strict test standards, coaxial structure calibration kits or special impedance probe workbench and sheet calibration kits [17], [18]. TRL calibration methods should be specifically designed for different measurements. The automatic removal method of single port and double port fixture is also a de-embedding method [19]–[21]. The time domain reflectometry (TDR) method is used to measure the *S* parameters to reduce the number of measurements. However, due to the limitation of frequency band and the numerical error in the transformation process from frequency domain to time domain, their accuracy is reduced. There is a conflict between the accuracy and efficiency of all de-embedding methods. Designers need to balance the simplicity, accuracy and efficiency of de-embedding methods [15], [22].

There are two traditional measurement methods for the impedance measurement of SMD electronic components: fixture measurement based on port extension compensation and fixture de-embedding measurement. The former is a

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[†]Research Center of Electromagnetic Environment Effect, Southeast University, NanJing, 211102 P. R. China.
a) E-mail: zyzhou@seu.edu.cn (Corresponding author)

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simple method, the advantage is simple operation, easy to implement; The disadvantage is that the accuracy is low, and the fixture used is required to have a smooth frequency response, the method cannot correct the mismatch error introduced by the fixture, and can be used in some occasions with low precision requirements.

Fixture de-embedding test method is to use the coaxial calibration data of the VNA and the S parameter file of fixture to achieve fixture de-embedding function and correct the test data. After the network analyzer is calibrated, the S parameter file (.s2p) of the fixture is introduced to obtain the S parameter or Z parameter of the DUT (device under test) through calculation. The advantage of this method is that the precision is very high, but its limitation and difficulty is how to obtain the S parameter of the test fixture.

Although the test concept of de-embedding is indeed widely used, there are several ways to obtain the source of S parameters used for de-embedding. The method of obtaining S parameter can be analytic method, test method or simulation method.

One way to eliminate the measurement error of the fixture is to use the impedance probe table and calibration kits in the process of measurement [17], [18], [24]. With the calibration reference planes located at the front and end of the probes, the impedance of SMD electronic components can be obtained by direct testing. However, the impedance probe bench and its calibration kits are often expensive and not widely available [23].

The innovation point and the main core of this paper is to solve the difficult problem of S parameter acquisition in de-embedding test, a method of S parameter acquisition by full wave simulation is proposed, and impedance extraction of the electronic components of the patch is carried out by using de-embedding technology. The model of full-wave simulation is highly consistent with the model of actual test, and the method of obtaining S parameter in full-wave simulation is close to the test, so the method is more acceptable to readers. Using the test method proposed in this paper, it has better simplicity, accuracy, universality and high efficiency in the studied frequency band. This method does not need to rely on expensive probe impedance test platform and calibration sheet, and can obtain impedance parameters by using common VNA.

2. The Specific Method of Extracting Impedance of SMD Electronic Components by Simulation and Testing

In order to obtain the impedance parameters of SMD electronic components, the method of combining simulation and test is adopted to study the impedance parameter extraction of SMD electronic components. The characteristics of left and right fixture can be obtained from the method by full-wave simulation. The impedance of the components can be obtained finally.

The specific steps are shown in Fig. 1.

1) Design of fixture for impedance test of SMD electronic components.

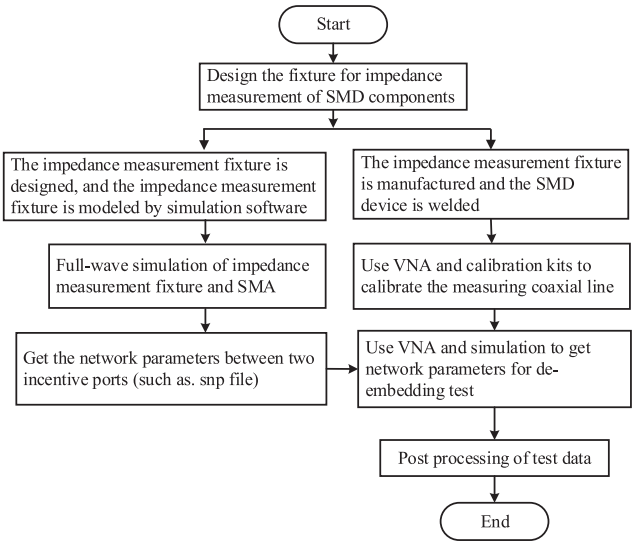

Fig. 1 Impedance parameter extraction steps of SMD electronic components based on full-wave simulation and de-embedding technique.

2) Full-wave simulation is performed on the impedance test PCB to obtain the network parameter files. After the impedance measurement fixture is made, the calibration plane is extended from the coaxial end face to the measurement end face by using the de-embedding technique.

3) Estimate the impedance value and select the appropriate impedance measurement method.

4) Calibration and testing.

5) Post-treatment.

The impedance of the SMD electronic components is obtained by de-embedding and post-processing the measured S parameter files using the VNA.

2.1 Design of the Fixture for Impedance Test of SMD Electronic Components

The impedance measurement methods include radio frequency (RF) I-V method, balanced bridge method and network analysis method. Among them, the single-port reflection method of VNA is a common method to measure the impedance parameters of components. The principle of this method is to measure the impedance parameters through the reflection coefficient S_{11} of DUT measured by the single port of VNA.

In Eq. (1), it can be seen from the equation that when Z_{DUT} is small enough, the magnitude of the reflected signal is close to 1, so that it is difficult to distinguish it from 0 Ω. Therefore, the reflectance impedance measurement method with single port will lead to low accuracy.

$$S_{11} = \frac{Z_{DUT} - Z_1}{Z_{DUT} + Z_1} = \frac{Z_{DUT} - 50}{Z_{DUT} + 50} \tag{1}$$

Usually, when the impedance to be measured is less than 0.1 Ω, the value of S_{11} is close to 99% of 1. The closer S_{11} is to 1, the more difficult it is to measure. So S_{11} greater than

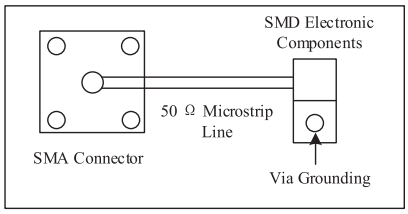

Fig. 2 Schematic diagram of reflective impedance measurement fixture.

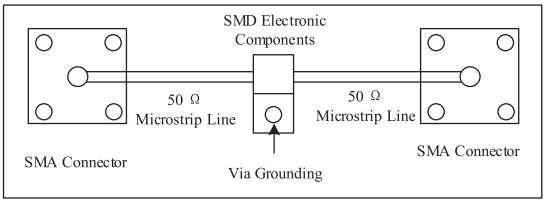

Fig. 3 Schematic diagram of shunt through type impedance measurement fixture.

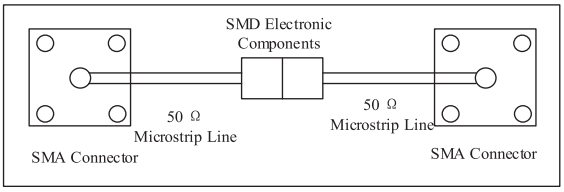

Fig. 4 Schematic diagram of series through type impedance measurement fixture.

0.99 is used as the practical limit for accurate measurement [25].

When the impedance to be measured is less than 0.1 Ω, the shunt straight-through method is used as the measurement method. When the impedance of the component to be tested is greater than 1000 Ω, the series straight-through method is used as the impedance measurement method.

There are three types of impedance measurement fixture for SMD electronic components, including reflection type impedance measurement fixture as shown in Fig. 2, shunt through type impedance measurement fixture as shown in Fig. 3 and series through type impedance measurement fixture as shown in Fig. 4. The characteristic impedance of the micro-strip line on the PCB is 50 Ω, which is consistent with the characteristic impedance of the test instrument VNA and coaxial cable.

The reflective impedance measurement fixture is characterized in that the PCB comprises a micro-strip line with a characteristic impedance of 50 Ω. One end of the micro-strip line is an SMA connector, the other end is a pin pad corresponding to the package SMD element, and the other pin of SMD element pad is grounded.

The shunt through type impedance measurement fixture consists of two equal length micro-strip lines with characteristic impedance of 50 Ω. One end of the two micro-strip lines is connected to one pin pad of SMD element, the other ends of the micro-strip lines are connected to two SMA connectors, and the other pin pad of SMD element is grounded.

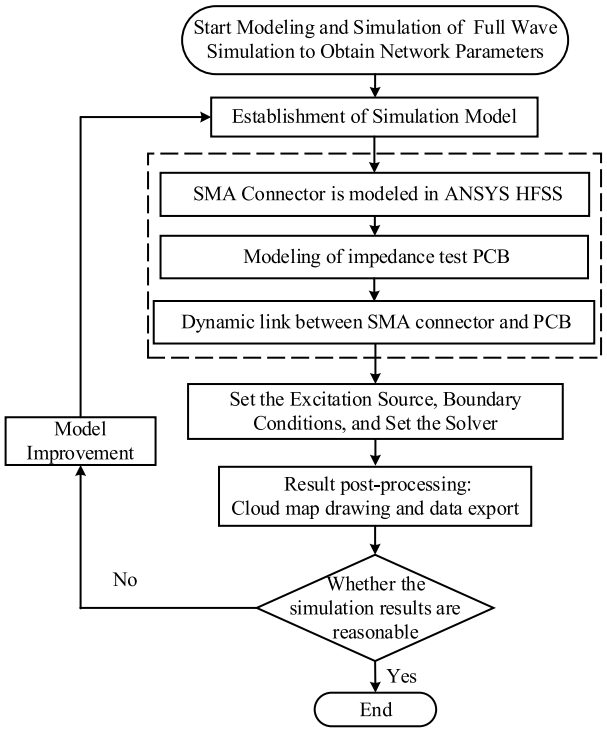

Fig. 5 Simulation flow chart of obtaining network parameters by simulation method.

The series through type impedance measurement fixture includes two equal length micro-strip lines with characteristic impedance of 50 Ω. The two pins of SMD element pad are connected to two SMA connectors through 50 Ω micro-strip wires.

2.2 Full-Wave Simulation to Obtain Network Parameters

Electromagnetic simulation software was used to conduct 3D modeling of the impedance measurement fixture and its connectors, and full-wave simulation was carried out to obtain the network parameters of the fixture. The flow chart of obtaining network parameters through full-wave simulation is shown in Fig. 5, as follows:

1) Establishment of Simulation Model

(1) SMA connector is modeled in ANSYS HFSS.

According to the material type of SMA, select the corresponding material type in the material library after the establishment of SMA model in ANSYS HFSS, and the electromagnetic parameters of the material such as conductivity and permeability can be set according to the actual SMA connector.

(2) Modeling of impedance test fixture

Import the model of the fixture into ANSYS HFSS 3DLayout to complete the modeling. Since the model covers all information of the fixture, such as lamination, material, size, etc., modeling can be easily realized by this method. The modeling of impedance test fixture in this paper adds the direct import of electronic design automation (EDA) tool into HFSS 3Dlayout to realize the consistency of design and

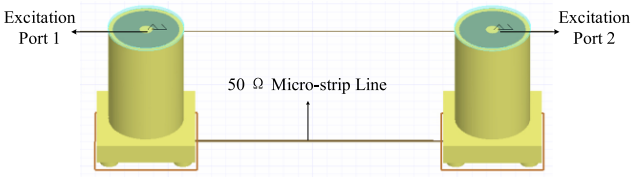

Fig. 6 Full-wave simulation of checking model.

simulation. Because the EDA tool includes the information of stacking and material of impedance test fixture, it effectively improves the consistency between simulation and test.

(3) Dynamic link between SMA connectors and the fixture

Set the excitation port and solver on the connector of SMA, and use the dynamic link method to import it into HFSS 3D Layout.

2) Set the Excitation Source, Boundary Conditions, and Set the Solver

Set the front end of the fixture as the excitation port, and adopt the default boundary condition.

The solver is based on the finite element principle, and the frequency range of the solution is set to 100 kHz~3 GHz.

3) Simulation Result Processing

After the simulation is completed, the S parameter between the two excitation ports can be obtained by the simulation are stored as .snp files which will be used as the necessary files for later de-embedding tests.

2.3 Judge the Accuracy of Simulation Results

In order to verify the correctness of S parameters of fixture network obtained by full-wave simulation, a micro-strip line with characteristic impedance of 50 Ω is designed, and both ends of the micro-strip line are connected with an inner conductor of SMA connector. The S_{21} parameters are compared by full-wave simulation and test. The full-wave simulation is shown in the Fig. 6.

It can be seen from Fig. 7 that the S_{21} parameter error between full-wave simulation and measured is within 0.5 dB from 100 kHz to 2.5 GHz, and within 1.5 dB from 2.5 GHz to 3 GHz. In the frequency band between 2.5 GHz and 3 GHz, the S_{21} parameters gap obtained by simulation and test increases because the fixture substrate material used in the design is FR4, and the dielectric constant during simulation is a fixed value of 4.4. However, the dielectric constant of FR4 substrate material decreases with the increase of frequency. It is recommended to choose Rogers substrate, the dielectric constant is relatively stable and high, low dielectric loss.

The polarization of dielectric appears under the action of external electric field. When the frequency is high enough, the dielectric constant ε of the medium becomes complex due to polarization loss,

$$\varepsilon = \varepsilon' - j\varepsilon'' \tag{2}$$

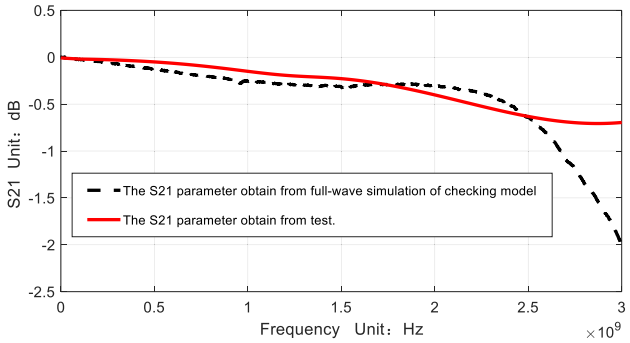

Fig. 7 The S_{21} parameters compared between full-wave simulation and test.

Table 1 Select different impedance test method table.

Impedance Value	Select Impedance Test Type	Notes
1mΩ - 50Ω,	shunt through impedance measurement	If $\|Z\| < 0.1$ Ω, it is small impedance value
0.1 Ω - 1000 Ω	reflective impedance measurement	If $0.1\ \Omega \leqslant \|Z\| \leqslant 1000\ \Omega$, it is medium impedance value
1 Ω -500kΩ	series through impedance measurement	If $\|Z\| > 1000$ Ω, it is large impedance value

Where: $-j\varepsilon''$ means that there is a loss in the medium.

In HFSS 3D Layout, dielectric material FR4 parameters such as relative permittivity ($\varepsilon_r = 4.4$), dielectric loss tangent ($tg\delta = 0.02$) and so on are set according to the actual material.

$$\varepsilon = \varepsilon' - j\varepsilon'' = \varepsilon_r(1 - jtg\delta) = 4.4 \times (1 - 0.02j) \tag{3}$$

In HFSS 3D Layout, the imaginary part of the complex dielectric constant can be obtained according to Eq. (3). Similarly, the conductivity of the metal conductor copper is also set according to the actual material conductivity in the simulation software.

In full-wave simulation, conductor loss and dielectric loss can be obtained by post-processing of the field calculation tool of the simulation software.

2.4 Estimate the Impedance Value and Select the Appropriate Impedance Measurement Method

Estimate the impedance value of the SMD component and select the appropriate test fixture. According to Table 1, select different types of impedance test methods according to the impedance values of different frequency points of SMD components.

The impedance measurement methods listed in Table 1 all use the network analysis method of self-made fixture to extract the impedance of the SMD component. The measurement accuracy of reflection type impedance is related to the reflection coefficient value S_{11} of DUT, and the measurement accuracy of this value is related to the impedance value of DUT. The shunt through measurement method is adopted for DUT with low impedance. For high impedance, series through measurement method is adopted.

1) Impedance test method selection of SMD capacitance

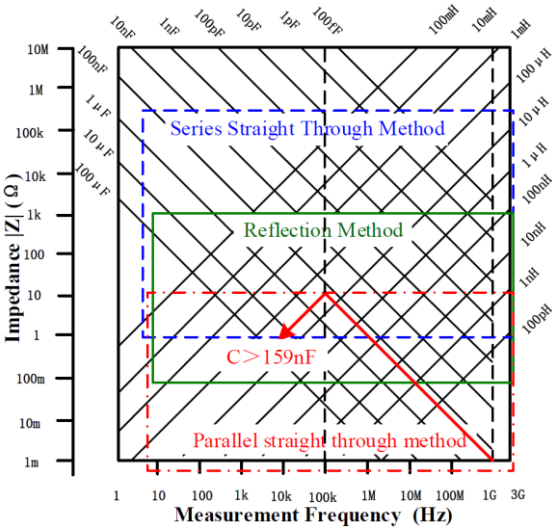

Fig. 8 SMD capacitance impedance test extraction diagram.

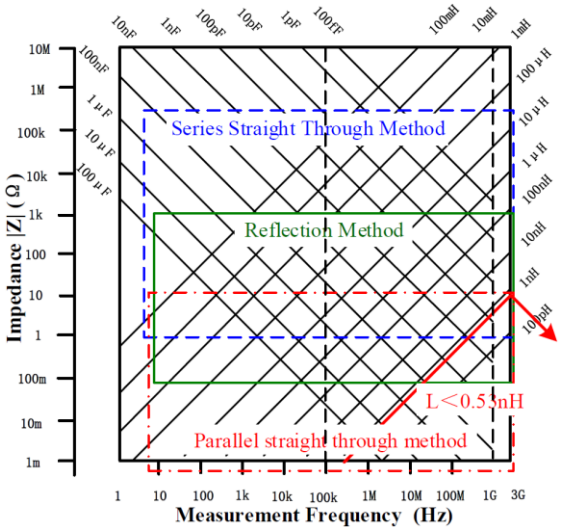

Fig. 9 SMD inductance impedance test extraction diagram.

According to the test frequency of 100 kHz~3 GHz, From Eq. (4) of the ideal capacitive reactance.

$$Z_c = \frac{1}{(\omega C)} \tag{4}$$

As shown in Fig. 8, each diagonal line is the capacitance or inductance with corresponding impedance values at different frequencies in the ideal case.

According to Eq. (4) and Fig. 8, when $|Z_c|_{f=100\,kHz} < 10\,\Omega$, it can get that $C > 159$ nF. In other words that if the value of SMD capacitance is greater than 159 nF, The shunt through method is a suitable method for impedance measurement and extraction when the measurement frequency is between 100 kHz and 3 GHz.

According to Eq. (4) and Fig. 8, if the value of SMD capacitance is less than 159 nF, the series method or reflection method can be a suitable method for impedance measurement and extraction when the measurement frequency is between 100 kHz and 3 GHz.

2) Impedance test method selection of SMD inductance

According to the test frequency of 100 kHz~3 GHz, from Eq. (5) of the ideal capacitive inductance.

$$Z_L = \omega L \tag{5}$$

According to Eq. (5) and Fig. 9, when $|Z_L|_{f=3\,GHz} < 10\,\Omega$, it can get that $L < 0.53$ nH. In other words that if the value of SMD inductance is less than 0.53 nH, The shunt through method is a suitable method for impedance measurement and extraction when the measurement frequency is between 100 kHz and 3 GHz.

2.5 Calibration and Testing

Use VNA and calibration kits to calibrate the coaxial cable and instrument equipment for measurement. After calibration, the calibration plane is at the end face of the coaxial cable connector. If the reflection impedance measurement fixture is selected, it is a single port Open-Short-Through (OST) calibration. If the series through impedance measurement fixture or shunt through impedance measurement fixture is selected, it is a dual port Through-Open -Short -Match (TOSM) calibration.

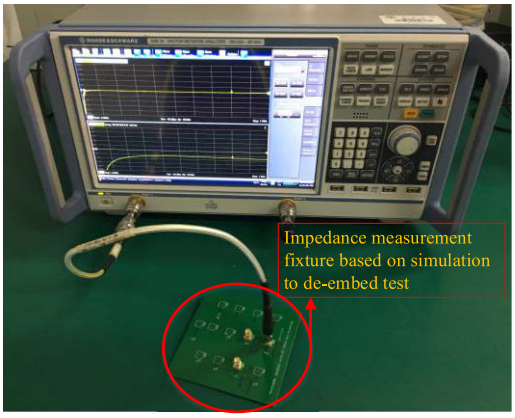

Fig. 10 Test diagram of testing fixture with reflective impedance.

After the calibration of VNA and coaxial cable, use the network parameter file (such as .snp file) obtained by simulation in step 2 to carry out de-embedding test on the impedance measurement fixture with SMD elements, and obtain S-parameter test data as Fig. 10.

If the reflective impedance measurement fixture is selected, select S_{11} parameter. If series through type impedance measurement PCB or shunt through type impedance measurement PCB is selected, select S_{21} parameter.

2.6 Data Processing

The impedance parameters of the SMD element can be obtained by data processing the test data obtained by VNA.

The conversion relationship between impedance and S_{11} of the measured patch element with medium impedance value measured by the reflection measurement method is as follows:

$$Z_{DUT} = \frac{50 \times (1 + S_{11})}{(1 - S_{11})} \tag{6}$$

The conversion relationship between the impedance and S_{21} of the measured patch element with medium to large impedance value measured by the series through method is as follows:

$$Z_{DUT} = \frac{50 \times 2 \times (1 - S_{21})}{S_{21}} \tag{7}$$

The conversion relationship between the impedance and S_{21} of the measured patch element with a small impedance value measured by the shunt through method is as follows:

$$Z_{DUT} = \frac{50 \times S_{21}}{(2 \times (1 - S_{21}))} \tag{8}$$

Equations (6)–(8) are used for processing. Researchers use matlab software to compile programs for testing and obtain S parameter processing, which is then converted into Z parameter. Another method is to use the VNA internal S parameter conversion Z parameter function (this is actually also carried out by the vector network internal data processing).

3. Research Based on "2×Thru" De-Embedding Test

Figure 11 shows the test fixture of SMD electronic components. The characteristics of the fixture include the left and right micro-strip lines and the SMA adapter characteristics. Generally, the instrument is calibrated to the coaxial interface by using the coaxial calibration kits. The calibrated test surface is called the measurement plane, and the plane where the SMD device is placed is called the device plane. However, the characteristics of the SMD device directly measured by using calibration kits also include the fixture characteristics.

The corresponding T parameter matrices are respectively T_{Fix_A}, T_{DUT}, T_{Fix_B}.

According to Fig. 11, the overall characteristics of the measuring fixture and DUT are as follows:

$$T_{Measurement} = T_{Fix\_A} \times T_{DUT} \times T_{Fix\_B} \tag{9}$$

Where:

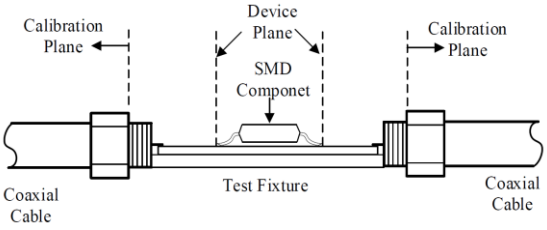

Fig. 11 The test fixture of SMD electronic components [26].

T_{Fix_A} is transmission coefficient from the coaxial cable on the left side of the fixture to SMD components.

T_{DUT} is transmission coefficient of the DUT.

T_{Fix_B} is transmission coefficient from the coaxial cable on the right side of the fixture to SMD components.

If the characteristics of the left and right fixtures are known, then the matrix operation property can be obtained as follows:

$$T_{DUT} = {T_{Fix\_A}}^{-1} \times T_{Measurement} \times {T_{Fix\_B}}^{-1} \tag{10}$$

Therefore, as long as the two-port characteristics of the left and right fixtures are obtained, de-embedding can be accomplished and DUT's characteristic can be obtained.

"2×Thru" is a de-embedding structure composed of directly connected replicas of left fixture and right fixture for a given DUT. "2×Thru" is a de-embedding method that utilizes the "2×Thru" structure to remove the fixture effects when measuring the DUT [27].

$$T_{2\times Thru} = T_{Fix\_A} \times T_{Fix\_B} \tag{11}$$

$$T_{Fix\_B} = {T_{Fix\_A}}^{-1} \times T_{2\times Thru} \tag{12}$$

It can be obtained from Eq. (9) that:

$$T_{Measurement} \times {T_{2\times Thru}}^{-1} \times T_{Fix\_A} = T_{Fix\_A} \times T_{DUT} \tag{13}$$

$$T_{DUT} = {T_{Fix\_A}}^{-1} \times T_{Measurement} \times {T_{2\times Thru}}^{-1} \times T_{Fix\_A} \tag{14}$$

The process of "2×Thru" de-embedding is simple. The basic idea of "2×Thru" de-embedding method is as follows: measure the S parameter of "2×Thru" structure firstly, assuming that the "2×Thru" structure is symmetric, the S parameter of the "1×structure" can be calculated directly from the "2×Thru" measurements. Once the S parameters of the "1×structure" on both sides of the DUT are obtained, the S parameters of the DUT can be easily calculated. The "2×Thru" de-embedding testing method can not only use the VNA but also the microwave probe platform.

Unlike the "2×Thru" method, the "L-2L" method is a method applied to de-embedding transmission lines, which does not require additional auxiliary testing structures. This method only requires two transmission lines with lengths of L and 2L to test the structure and remove parasitic factors from the Pad. This method also considers the DUT as a cascaded network of left pad, transmission line, and right pad. A transmission line with a length of 2L is naturally a cascade of two transmission lines with a length of L [28]–[30].

$$T_{through} = T_{left} \cdot T_{right} = M_{L_1} \cdot \left(M_{L_2}\right)^{-1} \cdot M_{L_1} \tag{15}$$

Where:

L_1 is L, which is the length of the short transmission line.

L_2 is 2L, which is the length of the long transmission line.

T_{left} is the ABCD matrix for the left pad.

T_{right} is the ABCD matrix for the right pad.

M_{L1} is the ABCD matrix for the intrinsic transmission-line structures of length L_1.

M_{L2} is the ABCD matrix for the intrinsic transmission-line structures of length L_2.

3.1 "2 × Thru" De-Embedding Test Steps

"2×Thru" de-embedding test works as follows:

The test fixture and the DUT are designed on the same PCB and the structure of the test fixture is the same as that of the DUT.

1) Measurement "2×Thru" to obtain the test results.

2) Measure the test fixture and DUT and obtain the test results.

3) Run software algorithm to obtain S parameters.

The VNA used in this study uses smart fixtures removal (SFD) algorithm [31], which is developed based on a waveform peeling algorithm application.

3.2 "2 × Thru" De-Embedding Test

The de-embedding test based on "2×Thru" consists of the following steps as shown in the Fig. 12:

1) Design "2×Thru" impedance de-embedding impedance measurement fixture and making board

The following impedance measurement PCB is designed according to the "2×Thru" de-embedding principle, which is capable of testing reflective, series and shunt pass-through SMD electronic components.

As shown in the Fig. 13, the impedance measurement fixture consists of four parts, which are the straight-through test line, the shunt straight-through impedance measurement line, the series straight-through impedance measurement line and the reflection impedance measurement line. It is similar to the test fixture based on the combination of simulation and de-embedding impedance, but the length of the test microstrip line and the DUT of the shunt straight-through type and series straight-through type is equal to the length of the straight-through calibration line, and the DUT is located at the midpoint. The configuration of the reflection type impedance measurement line is the same as that of the shunt straight-through type impedance measurement fixture.

2) Connect VNA to the test cable and perform Thru-Open-Short-Match calibration using the calibration kits to eliminate measurement errors as shown in Fig. 14.

3) The straight-through test line of the "2×Thru" impedance PCB is measured.

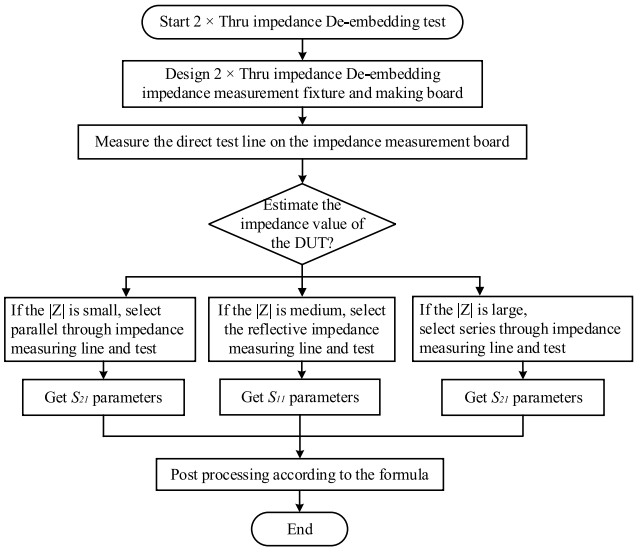

Fig. 12 Work flow diagram of "2×Thru" de-embedding test.

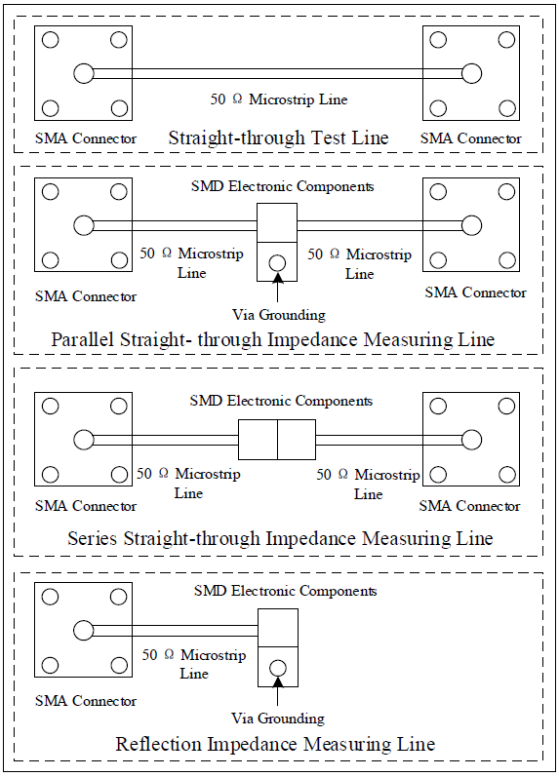

Fig. 13 Based on "2×Thru" de-embedded impedance measurement fixture.

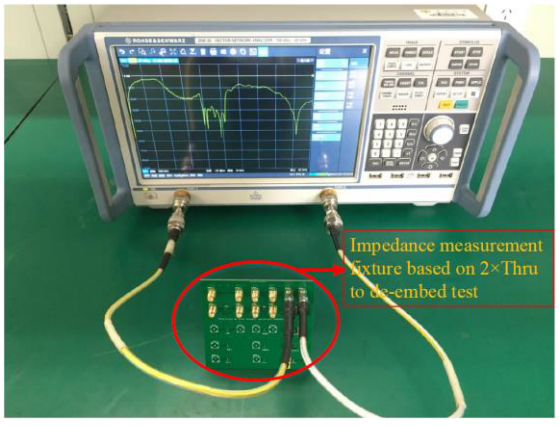

Fig. 14 "2×Thru" de-embedding test.

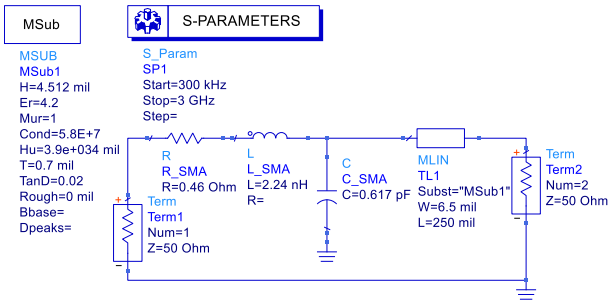

Fig. 15 Obtain the *S* parameter used for de-embedding based on ADS simulation.

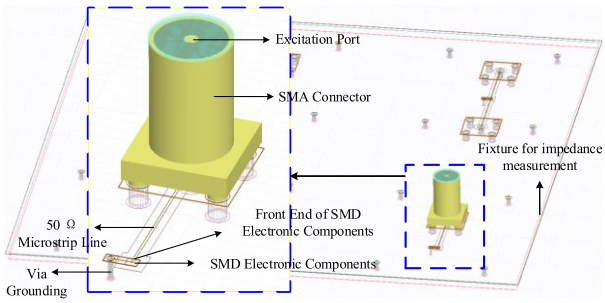

Fig. 16 ANSYS HFSS simulation modeling diagram of reflective type method based on full-wave simulation and de-embedding technique.

4) To estimate the impedance value of the tested SMD electronic components, select different types of impedance measurement methods according to the estimated impedance value in Table 1 in Sect. 2.4.

5) The *S* parameters can be obtained through software algorithm by running the de-embedding test program. The applied reference plane is transferred to the connector to be tested. And acquires the S_{21} parameter or the S_{11} parameter, respectively.

6) After post-processing according to the selected impedance test lines, the impedance values of the embedded SMD electronic components can be obtained using the "2×Thru" method.

4. *S* Parameter Acquisition for De-Embedded Test Based on ADS Simulation

To obtain the *S* parameter of the designed impedance testing fixture using ADS simulation method, it is necessary to de-embed components such as SMA connectors and microstrip lines. Among them, the *S* parameters of microstrip lines can be set in ADS simulation software, and the equivalent circuit of SMA connectors can be obtained by consulting literature [11]. As shown in Fig. 15, ADS simulation is conducted using a microstrip line with a characteristic impedance of 50 Ω and a length of 250 mil as an example. After completing the simulation, the *S* parameters obtained from ADS simulation will be exported for embedding testing.

5. Case: SMD Capacitance Impedance Measurement

The test capacitance value is 22 nF, the package is 0603, the model is GRM188R71E223KA01, and the brand is the parasitic parameter of Murata capacitor.

5.1 Estimate the Impedance Value and Select the Appropriate Measurement Method

According to the impedance value of the Murata capacitor tested, which is the medium impedance value, the reflective impedance measurement fixture is selected as the measurement board according to Sect. 2.4.

5.2 Full-Wave Simulation to Obtain Network Parameters

As shown in Fig. 16 use the simulation software ANSYS HFSS to conduct three-dimensional modeling on the impedance measurement PCB and SMA connector, and conduct full-wave simulation on them. Obtain the network parameter file between the excitation port of the coaxial connector and the front end of the SMD element on the impedance measurement fixture in the built model.

5.3 Calibration and Testing

Using VNA and coaxial calibrator to conduct single port Short-Open-Match calibration on the test cable.

Using the calibrated VNA and coaxial cable as the test instrument and equipment, and use the network file obtained by the simulation in step 2 of Fig. 1 to carry out the de-embedding test on the impedance measurement fixture installed with the SMD element to obtain the *S* parameter test data.

5.4 Data Processing

After processing the test data obtained by VNA de-embedding test, since the reflection impedance measurement Fixture is selected, S_{11} parameter is selected, and Eq. (6) is selected as the parameter for calculating the impedance of the SMD electronic components.

The impedance parameters of the capacitance can be obtained through the measurement from the Fig. 17. It can be seen from it that if the impedance is obtained by directly testing the method of acquiring S_{11} and converting it into the impedance of the component, the resonance frequency of the acquisition element will be lower than the actual impedance resonance frequency of the electronic element. If converted into an equivalent circuit, the inductance will increase. Through simulation and test comparison, it is found that the impedance parameters of the SMD capacitance can be accurately obtained by using the de-embedding test technique.

Taking the impedance value of GRM188R71E223KA01, the official model provided by Murata Capacitor, as a reference, the test results obtained by S-parameters obtained

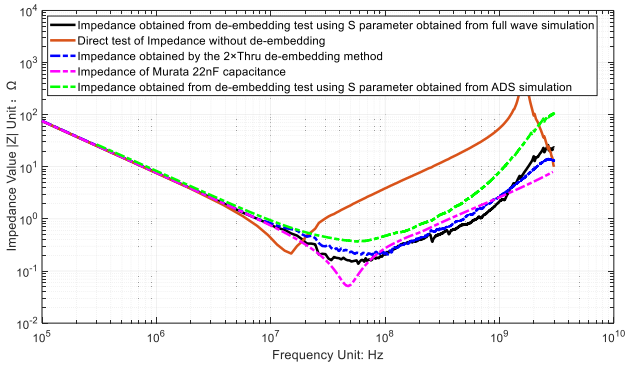

Fig. 17 Comparison diagram of simulation test of Murata capacitance 22 nF.

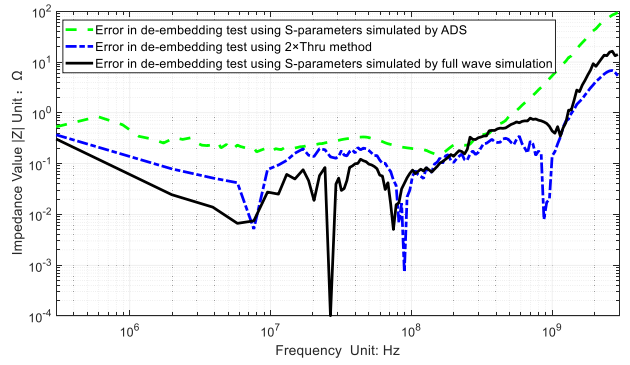

Fig. 18 Comparison of errors obtained from embedding tests using *S* parameters from different sources.

through "2×Thru", ADS simulation and full wave simulation were respectively compared, and the results were shown in Fig. 18.

As can be seen from Fig. 18, the error value of *S* parameter obtained by ADS simulation for de-embedding test in 200 kHz~3 GHz is higher than the other two. The *S* parameter was obtained by full wave simulation for the de-embedding test, and the error was smaller than that by using the "2×Thru" method when the frequency range was below 80 MHz. This shows that the method of obtaining *S* parameters based on full wave simulation proposed in this paper has higher accuracy than that of obtaining *S* parameters based on ADS simulation for de-embedding test.

6. Conclusion

The SMD electronic components are non-coaxial devices, and the structure and material information are unknown. The impedance parameters cannot be obtained by direct measurement, so it is necessary to design the impedance test fixture. The design of impedance test fixture for test extraction should consider the error caused by non-coaxial and measuring fixture.

An important contribution of this paper is to solve the difficult problem of *S* parameter acquisition in de-embedding test, and propose a method of full wave simulation to obtain *S* parameter used in de-embedding test, and use de-embedding technology to extract impedance from the electronic components of the patch. The *S* parameter obtained by this method is close to the actual test fixture, and the result is more accurate. The target frequency range for the methodology is 100 kHz~3 GHz. The *S* parameter used in the de-embedding test is obtained outside the VNA through full-wave simulation, while the *S* parameter is obtained by hardware testing and software algorithms in the VNA based on the "2×Thru" de-embedding test.

Based on the de-embedding test technique, the impedance of SMD electronic components of 22nF was tested and extracted, the *S* parameters for de-embedding were obtained using methods based on full wave simulation, "2×Thru", and ADS simulation. The results indicate that obtaining the *S* parameter of the testing fixture based on full wave simulation and conducting de-embedding testing compared to ADS simulation can accurately extract the impedance parameters of SMD electronic components. The research of impedance parameter extraction method based on full-wave simulation and de-embedding technique has important reference value for the analysis of EMI coupling mechanism of PCB.

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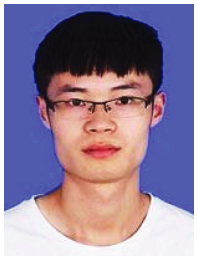
Yang Xiao received the B.S. degree and the M.S. degrees in mechatronic engineering from Hefei University of Technology, Hefei, China. He is currently working toward the Ph.D. degree in Southeast University, Nanjing, China. His current research interests include the electromagnetic compatibility.

Zhongyuan Zhou received the M.S. and Ph.D. degrees in mechatronic engineering from Southeast University, Nanjing, China, in 1998 and 2008, respectively. Currently, he is Professor of mechatronic engineering teaching and conducting research in electromagnetic compatibility.



Mingjie Sheng received the B.S. degree in mechatronic engineering from Nanjing University of Science and Technology, Nanjing, China in 2016. And he received the Ph.D. degrees in mechatronic engineering from Southeast University, Nanjing, China, in 2023. His research interests include EMC/EMI analysis.

Qi Zhou received the B.S. degree in mechatronic engineering in Southeast University, Nanjing, China. And he received the Ph.D. degrees in mechatronic engineering from Southeast University, Nanjing, China, in 2023. His research interests include EMC/EMI analysis.