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FOREWORD

Special Section on Analog Circuit Techniques and Related Topics

All amount of data traffic in the world is continuously increasing, and network infrastructures which are baselines of data traffic are also progressing. For example, 6G is developing as a future wireless network realizing high speed, low latency, multi connectivity, and so on. Data rate of wireline networks such as PCI Express is also increasing continuously. To realize the future network infrastructures, analog circuit techniques are one key techniques. Basically, digital-circuit performance is almost decided by selections of semiconductor process, however, analog-circuit performance is changed by its design and analog-circuit design techniques are still interesting research area.

This special section includes two invited papers, three regular papers and two letters which discuss interesting technical topics related to analog circuit techniques. The regular papers and letters covers circuit and system design techniques for wireless and wireline transceivers. In addition to these fine papers, this special section has two excellent invited papers. The first invited paper by Prof. Haruo Kobayashi reviews various design techniques for analog and mixed-signal circuits and systems. It is an epic work and a compilation of his long research career. The second invited paper by Dr. Guangwei Cong presents optical neural networks, optical analog computing techniques using silicon photonics technologies are applied to the neural networks.

On behalf of the editorial committee of this special section, I would like to express my sincere appreciation to all the authors who submitted manuscripts to this special section, all the reviewers, and the editorial committee members listed below for their technical and editorial contributions. Finally, I would like to express my special thanks to Prof. Hiroki Sato, Dr. Rui Ito, and Dr. Asuka Maki for their hard work as secretary and liaison.

Ryuichi Fujimoto, Guest Editor-in-Chief

Ryuichi Fujimoto *(Senior Member)* received his B.E., M.E., and Dr. Eng. Degrees from Waseda University, Tokyo, Japan, in 1988, 1990, and 2003, respectively. He joined the Mobile Communication Laboratory, Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 1991. Since then, he has been engaged in the research and development of analog integrated circuits and device models for wireless communication systems. In 2005, he was transferred to Wireless & Multimedia LSI Development Department, Toshiba Corp. Semiconductor Company. From 2009 to 2011, he was on loan to Semiconductor Technology Academic Research Center (STARC). Currently, he is with System Technology Research & Development Center, Kioxia Corporation. Dr. Fujimoto was an Associate Editor of IEICE Transactions on Electronics from 2001 to 2004, IEICE Electronics Express (ELEX) from 2003 to 2008, and IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences from 2005 to 2009. He was the secretary of the Japan Chapter of IEEE Circuits and Systems Society from 2008 to 2009 and the chair of Japan Chapter of IEEE Solid-State Circuit Society from 2019 to 2020. He is an organizing committee co-chair of A-SSCC 2024. He is a member of the IEEE, IEEJ, JIEP and JAAS.